REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Added two new packages, case outline letters Z and U. Adding case outline U, figure 1. Adding terminal connection U and Z in figure 2. Editorial changes throughout document.	93-10-25	Monica L. Poelking

REV																			
SHEET																			
REV	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A			
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30			

REV STATUS OF SHEETS															
REV	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY: Phu H. Nguyen

CHECKED BY: Tim H. Noh

APPROVED BY: Monica L. Poelking

DRAWING APPROVAL DATE: 92-04-10

REVISION LEVEL: A

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, DIGITAL, HCMOS MULTIFUNCTION PERIPHERAL, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	67268	5962-90864

SHEET 1 OF 30

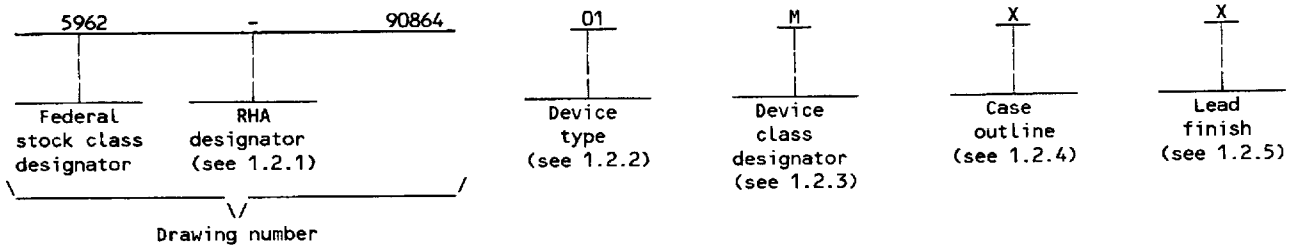
DESC FORM 193
JUL 91

5962-E359-93

1. SCOPE

1.1 Scope. This drawing forms a part of a one part - one part number documentation system (see 6.6 herein). Two product assurance classes consisting of military high reliability (device classes B, Q, and M) and space application (device classes S and V), and a choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). Device class M microcircuits represent non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices". When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:



1.2.1 RHA designator. Device classes M, B, and S RHA marked devices shall meet the MIL-M-38510 specified RHA levels and shall be marked with the appropriate RHA designator. Device classes Q and V RHA marked devices shall meet the MIL-I-38535 specified RHA levels and shall be marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Frequency	Circuit function
01	68C901B-4	4.0 MHz	HCMOS multifunction peripheral
02	68C901B-5	5.0 MHz	HCMOS multifunction peripheral
03	68C901B-8	8.0 MHZ	HCMOS multifunction peripheral

1.2.3 Device class designator. The device class designator shall be a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883
B or S	Certification and qualification to MIL-M-38510
Q or V	Certification and qualification to MIL-I-38535

1.2.4 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	GDIP1-T48 or CDIP2-T48	48	Dual-in-line
Y	CQCC1-N52	52	Leadless chip carrier
Z	CMGA15-P68	68	Pin grid array 1/
U	See figure 1	52	Leaded chip carrier

1.2.5 Lead finish. The lead finish shall be as specified in MIL-M-38510 for classes M, B, and S or MIL-I-38535 for classes Q and V. Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference.

1/ Inactive for new design.

1.3 Absolute maximum ratings. 1/

Supply voltage range, referenced to ground (V_{CC})	-0.3 V dc to +7.0 V dc
Input voltage	-0.3 V dc to +7.0 V dc
Storage temperature range	-55°C to 150°C
Maximum power dissipation (P_D)	55 mW
Lead temperature (soldering, 10 seconds)	+270°C
Maximum operating junction temperature (T_J)	+170°C
Thermal resistance, junction-to-case (Θ_{JC}):	
Cases X, Y and Z	See MIL-STD-1835
Case U	10°C/W

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	4.5 V dc minimum to 5.5 V dc maximum
High level input voltage range (V_{IH})	2.0 V dc to V_{CC}
Low level input voltage range (V_{IL})	-0.3 V dc to 0.8 V dc
Frequency of operation:	
Device type 01	1.0 MHz to 4.0 MHz
Device type 02	1.0 MHz to 5.0 MHz
Device type 03	1.0 MHz to 8.0 MHz
Case operating temperature range (T_C)	-55°C to +125°C

1.5 Digital logic testing for device classes Q and V.

Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012)	XX percent 2/

2. APPLICABLE DOCUMENTS

2.1 Government specifications, standards, bulletin, and handbook. Unless otherwise specified, the following specifications, standards, bulletin, and handbook of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATIONS

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.
MIL-I-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

MILITARY

MIL-STD-480 - Configuration Control-Engineering Changes, Deviations and Waivers.
MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-1835 - Microcircuit Case Outlines.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ Values will be added when they become available.

HANDBOOK

MILITARY

MIL-HDBK-780 - Standardized Military Drawings.

(Copies of the specifications, standards, bulletin, and handbook required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device class M shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein. The individual item requirements for device classes B and S shall be in accordance with MIL-M-38510 and as specified herein. For device classes B and S, a full electrical characterization table for each device type shall be included in this SMD. The individual item requirements for device classes Q and V shall be in accordance with MIL-I-38535, the device manufacturer's Quality Management (QM) plan, and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 for device classes M, B, and S and MIL-I-38535 for device classes Q and V and herein.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Block diagram. The block diagram shall be as specified on figure 3.

3.2.4 Output load circuits and waveforms. The output load circuits and waveforms shall be as specified on figure 4.

3.2.5 Radiation exposure circuit. The radiation exposure circuit shall be as specified when available.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. Marking for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein). In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103. Marking for device classes B and S shall be in accordance with MIL-M-38510. Marking for device classes Q and V shall be in accordance with MIL-I-38535.

3.5.1 Certification/compliance mark. The compliance mark for device class M shall be a "C" as required in MIL-STD-883 (see 3.1 herein). The certification mark for device classes B and S shall be a "J" or "JAN" as required in MIL-M-38510. The certification mark for device classes Q and V shall be a "QML" as required in MIL-I-38535.

3.6 Certificate of compliance. For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.7.3 herein). For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.7.2 herein). The certificate of compliance submitted to DESC-EC prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device class M, the requirements of MIL-STD-883 (see 3.1 herein), or for device classes Q and V, the requirements of MIL-I-38535 and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required for device class M in MIL-STD-883 (see 3.1 herein) or device classes B and S in MIL-M-38510 or for device classes Q and V in MIL-I-38535 shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DESC-EC of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-480.

3.9 Verification and review for device class M. For device class M, DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device classes M, B, and S. Device classes M, B, and S devices covered by this drawing shall be in microcircuit group number 105 (see MIL-M-38510, appendix E).

3.11 Serialization for device class S. All device class S devices shall be serialized in accordance with MIL-M-38510.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device class M, sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein). For device classes B and S, sampling and inspection procedures shall be in accordance with MIL-M-38510 and method 5005 of MIL-STD-883, except as modified herein. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-I-38535 and the device manufacturer's QM plan.

4.2 Screening. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. For device classes B and S, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to qualification and quality conformance inspection. For device classes Q and V, screening shall be in accordance with MIL-I-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes M, B, and S.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. For device class M, the test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. For device classes B and S, the test circuit shall be submitted to the qualifying activity. For device classes M, B, and S, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-I-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in appendix B of MIL-I-38535.

4.3 Qualification inspection.

4.3.1 Qualification inspection for device classes B and S. Qualification inspection for device classes B and S shall be in accordance with MIL-M-38510. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, and D inspections (see 4.4.1 through 4.4.5).

4.3.2 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-I-38535. Inspections to be performed shall be those specified in MIL-I-38535 and herein for groups A, B, C, and D inspections (see 4.4.1 through 4.4.5).

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ V_{CC} = 5.0 V ±10% 1/ unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Low level input voltage for all inputs 2/	V_{IL}	V_{CC} = 5.5 V	1, 2, 3	All	-0.3	0.8	V
High level input voltage for all inputs (except XTAL1, XTAL2, CLK)	V_{IH1}	V_{CC} = 5.5 V			2.0	V_{CC}+.3	V
High level input voltage for (XTAL1, XTAL2, CLK)	V_{IH2}	V_{CC} = 5.5 V			V_{CC}-1.5	V_{CC}+.3	V
Low level output voltage (except DTACK)	V_{OL}	V_{CC} = 4.5 V, I_{OL} = 2.0 mA V_{IN} = $V_{IH\ min}$, $V_{IL\ max}$				0.5	V
High level output voltage (except DTACK)	V_{OH}	V_{CC} = 4.5 V, I_{OH} = -120 µA V_{IN} = $V_{IH\ min}$, $V_{IL\ max}$			2.4		V
Supply current	I_{CC}	Outputs open V_{CC} = 5.5 V				10	mA
Input leakage current	I_{IN}	V_{IN} = 0 V to 5.5 V			-10	10	µA
Three-state input current in float	I_{LOH}	V_{OUT} = 2.4 V to V_{CC}				10	µA
	I_{LOL}	V_{OUT} = 0.5 V				-10	µA
$\overline{\text{DTACK}}$ output source current	I_{OH}	V_{OUT} = 2.4 V, V_{CC} = 5.5 V				-400	µA
$\overline{\text{DTACK}}$ output sink current	I_{OL}	V_{OUT} = 0.5 V, V_{CC} = 5.5 V			5.3		mA
Input capacitance	C_{IN}	Reverse voltage = 0 V, f = 1.0 MHz, T_A = +25°C see 4.4.1b	4			10	pF
Output capacitance	C_{OUT}					10	pF
Functional test		see 4.4.1c V_{CC} = 4.5 V, 5.5 V	7, 8				

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ V_{CC} = 5.0 V ±10% 1/ unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
$\overline{CS}$, $\overline{DS}$ width high 3/	t_1	See figure 4 V_{CC} = 4.5 V and 5.5 V	9, 10, 11	01	50		ns
				02	35		
				03	25		
R/$\overline{W}$, A1-A5 valid to falling $\overline{CS}$	t_2			01	30		
				02	25		
				03	20		
Data valid prior to $\overline{DS}$ high	t_3			01	250		
				02	200		
				03	120		
$\overline{CS}$, $\overline{IACK}$ valid prior to falling CLK 4/	t_4			All	50		
CLK low to $\overline{DTACK}$ low	t_5			01		220	
				02		180	
				03		90	
$\overline{CS}$, $\overline{DS}$, or $\overline{IACK}$ high to $\overline{DTACK}$ high	t_6			01		60	
				02		55	
				03		50	
$\overline{CS}$, $\overline{DS}$, or $\overline{IACK}$ high to $\overline{DTACK}$ high impedance state 5/	t_7			All		100	
$\overline{CS}$, $\overline{DS}$, or $\overline{IACK}$ high to data invalid (write)	t_8			All	0		
$\overline{CS}$, $\overline{DS}$, or $\overline{IACK}$ high to data invalid (read)	t_{8A}			All	0		
$\overline{CS}$, $\overline{DS}$, or $\overline{IACK}$ high to data three-state 5/	t_9			All		50	
$\overline{CS}$, $\overline{DS}$, or $\overline{IACK}$ high to R/W, A1-A15 invalid	t_{10}			All	0		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ V_{CC} = 5.0 V ±10% 1/ unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Data valid from $\overline{CS}$ low 3/ 4/	t_{11}	See figure 4 V_{CC} = 4.5 V and 5.5 V	9, 10, 11	01		310	ns
				02		260	
				03		180	
Read data valid to $\overline{DTACK}$ low valid	t_{12}			All	10		
$\overline{DTACK}$ low to $\overline{DS}$, $\overline{CS}$, or $\overline{IACK}$ high	t_{13}			All	10		
$\overline{IEI}$ low to falling CLK	t_{14}			All	50		
$\overline{IEO}$ valid from CLK low 6/	t_{15}			01, 02		180	
				03		120	
Data valid from CLK low	t_{16}			01, 02		300	
				03		180	
$\overline{IEO}$ invalid from $\overline{IACK}$ high	t_{17}			01, 02		150	
				03		100	
$\overline{DTACK}$ low from CLK high	t_{18}			01		180	
				02		165	
				03		100	
$\overline{IEO}$ valid from $\overline{IEI}$ low	t_{19}			All		100	
Data valid from $\overline{IEI}$ low	t_{20}			01, 02		220	
				03		140	
CLK cycle time 5/	t_{21}			01	250	1000	
				02	200	1000	
				03	125	1000	
CLK width low	t_{22}			01	110		
				02	90		
				03	55		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$, V_{CC} = 5.0 V ±10% 1/ unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
CLK width high	t_{23}	See figure 4, V_{CC} = 4.5 V and 5.5 V	9, 10, 11	01	110		ns
				02	90		
				03	55		
$\overline{CS}$, $\overline{IACK}$ inactive to rising CLK 7/	t_{24}			01	100		
				02	80		
				03	50		
I/O minimum active pulse width	t_{25}			All	100		
$\overline{IACK}$ width high	t_{26}			All		$2\ t_{CLK}$	
I/O data valid from CLK↓ following $\overline{CS}$↑ or $\overline{DS}$↑	t_{27}			01		450	
				02		400	
				03		300	
Receiver ready delay from rising RC	t_{28}			01, 02		600	
				03		200	
Transmitter ready delay from rising RC	t_{29}			01, 02		600	
				03		200	
Timer output low from rising edge of $\overline{CS}$, $\overline{DS}$ 8/	t_{30}			01, 02		450	
				03		200	
Timer output valid from internal time-out 4/ 5/ 8/	t_{31}			All		$2\ t_{CLK} + 300$	
Timer CLK low time	t_{32}			01	110		
				02	90		
				03	55		
Timer CLK high time	t_{33}			01	110		
				02	90		
				03	55		
Timer CLK cycle time 5/	t_{34}			01	250	1000	
				02	200	1000	
				03	125	1000	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ V_{CC} = 5.0 V ±10% 1/ unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
$\overline{\text{RESET}}$ low time	t_{35}	See figure 4 V_{CC} = 4.5 V and 5.5 V	9, 10, 11	01	2.0		µs
				02	1.6		
				03	1.0		
Delay to falling $\overline{\text{IRQ}}$ from external interrupt, active transmitter	t_{36}			01, 02		380	ns
				03		250	
Transmitter interrupt delay falling TC	t_{37}			01, 02		550	
				03		300	
Transmitter underrun error or end of break interrupt delay from rising edge of TC	t_{37A}			01, 02		550	
				03		300	
Receiver buffer full interrupt transmit delay from rising RC	t_{38}			01, 02		800	
				03		400	
Receive error interrupt transmit delay from falling edge of RC	t_{39}			All		800	
Serial in setup time of rising edge of RC (divide by one only)	t_{40}			01	80		
				02	70		
				03	50		
Data hold time from rising edge of RC (divide by one only)	t_{41}			01	350		
				02	325		
				03	100		
Serial output data valid from falling edge of TC	t_{42}			01		440	
				02		420	
				03		200	
Transmitter CLK low time	t_{43}			01	500		
				02	450		
				03	250		
Transmitter CLK high time	t_{44}			01	500		
				02	450		
				03	250		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ V_{CC} = 5.0 V ±10% 1/ unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Transmitter CLK cycle time	t_{45}	See figure 4 V_{CC} = 4.5 V and 5.5 V	9, 10, 11	01	1000		ns
				02	900		
				03	500		
Receiver CLK low time	t_{46}			01	500		
				02	450		
				03	250		
Receiver CLK high time	t_{47}			01	500		
				02	450		
				03	250		
Receiver CLK cycle time 5/	t_{48}			01	1000		
				02	900		
				03	500		
$\overline{CS}$, $\overline{IACK}$, $\overline{DS}$ width low	t_{49}			All		80 t_{CLK}	
Serial output data valid from falling edge TC (+16)	t_{50}			01		490	
				02		370	
				03		240	
Cycle time	t_{51}			All	1000		
Pulse width, E high	t_{52}				430		
Pulse width, E low	t_{53}				450		
Address R/W setup time before E	t_{54}				80		
$\overline{CS}$ setup time before E	t_{55}				80		
Address hold time	t_{56}				10		
$\overline{CS}$ hold time	t_{57}				10		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ V_{CC} = 5.0 V ±10% 1/ unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Output data delay (read)	t_{58}	See figure 4 V_{CC} = 4.5 V and 5.5 V	9, 10, 11	All		250	ns
Data hold time	t_{59}				0	100	
Input data setup time (write)	t_{60}				280		
Data hold time (write)	t_{61}				20		
Cycle time	t_{62}				800		
Pulse width $\overline{DS}$ low or R/$\overline{W}$ high	t_{63}				350		
Pulse width $\overline{DS}$ low or R/$\overline{W}$ low	t_{64}				340		
Pulse width $\overline{AS}$, ALE high	t_{65}				100		
Delay $\overline{AS}$ fall to $\overline{DS}$ rise or ALE fall to R/$\overline{W}$ fall	t_{66}				30		
Delay $\overline{DS}$ or R/$\overline{W}$ rise to $\overline{AS}$, ALE	t_{67}				30		
R/$\overline{W}$ setup time to $\overline{DS}$	t_{68}				100		
R/$\overline{W}$ hold time to $\overline{DS}$	t_{69}				10		
Address setup time $\overline{AS}$, ALE	t_{70}				20		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ V_{CC} = 5.0 V ±10% 1/ unless otherwise specified	Group A subgroups	Device types	Limits		Unit
					Min	Max	
Address setup to $\overline{AS}$, ALE	t_{71}	See figure 4 V_{CC} = 4.5 V and 5.5 V	9, 10, 11	All	20		ns
Data setup time to $\overline{DS}$ or R/$\overline{W}$ (write)	t_{72}				280		
Delay data to $\overline{DS}$ or R/$\overline{W}$ (read)	t_{73}					250	
Data hold time to $\overline{DS}$ or R/$\overline{W}$ (write)	t_{74}				20		
Data hold time to $\overline{DS}$ or R/$\overline{W}$ (read)	t_{75}					100	
$\overline{CE}$ setup time to $\overline{AS}$, ALE fall	t_{76}				20		
$\overline{CE}$ hold time to $\overline{DS}$, or R/$\overline{W}$	t_{77}				20		
CLK rise time	t_{78}					10	
CLK fall time	t_{79}					10	

1/ All testing must be performed under the worst case condtition unless otherwise specified.

2/ For clock inputs V_{IL} = 0.5 V maximum.

3/ Although $\overline{CS}$ and $\overline{DTACK}$ are synchronized with the clock, the data out during a read cycle is asynchronous to the clock, recycling only on $\overline{CS}$ for timing.

4/ If the setup time is not met, $\overline{CS}$ or $\overline{IACK}$ will not be recognized until the next falling CLK.

5/ t_7, t_9, t_{21}, t_{31}, t_{34}, t_{45}, and t_{48} are provided for information purposes only, not for inspection purposes.

6/ $\overline{IEO}$ only goes low if no acknowledgeable interrupt is pending. If $\overline{IEO}$ goes low, $\overline{DTACK}$ and the data bus remain three-stated.

7/ If the setup time is met (for consecutive cycles), the minimum hold-off time of one clock cycle will be obtained. If not met, the hold-off will be two clock cycles.

8/ t_{CLK} refers to the clock applied to the MFP CLK input pin.

Case U

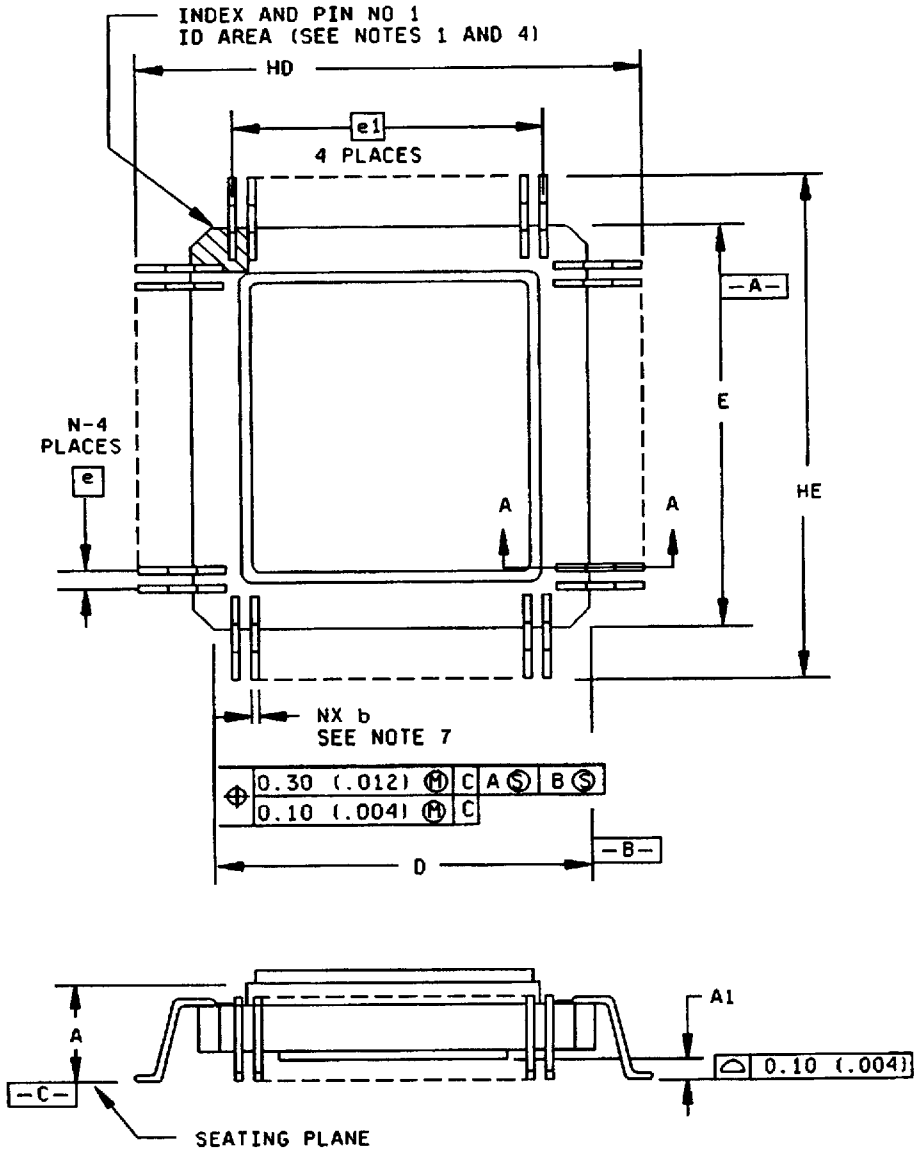


FIGURE 1. Case outline.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-90864
		REVISION LEVEL A	SHEET 14

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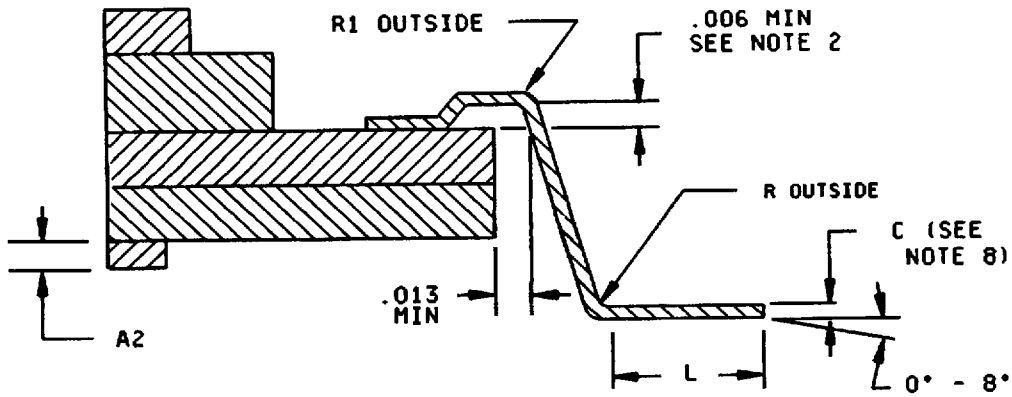
Case U



Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A		3.18		.125
A1	.46	.89	.018	.035
b	.33	.76	.014	.030
c	.13	.25	.005	.010
D/E	23.74	24.38	.935	.960
e	1.27 BCS		.050 BCS	
e1	15.24 BCS		.600 BCS	
HD/HE	28.78	29.13	1.133	1.147
L	.61	1.01	.024	.040
N	52		52	
R	.28	.86	.011	.034
R1	.23		.009	

NOTES:
1. A terminal 1 identification mark shall be located at the index corner in the shaded area shown. Terminal 1 is located immediately adjacent to and counterclockwise from the index corner. Terminal numbers increase in a counterclockwise direction when viewed as shown.
2. Generic lead attach dogleg depiction.
3. Dimension N: number of terminals.
4. Corner shapes (square, notch, radius, etc.)
5. The preferred unit of measurement is millimeters. However, this item was designed using inch-pound units of measurements. In case of problems involving conflicts between the metric and inch-pound units, the inch-pound units shall rule.
6. Datums X and Y to be determined where center leads exit the body.
7. Dimensions b and c include lead finish.

FIGURE 1. Case outline - Continued.

Terminal number	Terminal symbol		
	Case outlines		
	X	Y	U
1	$\overline{R/W}$	NC	D6
2	A1	R/W	D7
3	A2	A1	IACK
4	A3	A2	DTACK
5	A4	A3	DS
6	A5	A4	CS
7	TC	A5	NC
8	SO	TC	R/W
9	SI	SO	A1
10	RC	SI	A2
11	V_{CC}	RC	A3
12	MPX	V_{CC}	A4
13	TAO	MPX	A5
14	TBO	NC	TC
15	TCO	TAO	SO
16	TDO	TBO	SI
17	XTAL1	TCO	RC
18	XTAL2	TDO	V_{CC}
19	TAI	XTAL1	MPX
20	TBI	XTAL2	NC
21	RESET	NC	TAO
22	I0	TAI	TBO
23	I1	TBI	TCO
24	I2	RESET	TDO
25	I3	I0	XTAL1
26	I4	I1	XTAL2

Terminal number	Terminal symbol		
	Case outlines		
	X	Y	U
27	I5	I2	NC
28	I6	I3	TAI
29	I7	I4	TBI
30	IR	I5	RESET
31	RR	I6	I0
32	IRQ	I7	I1
33	IEO	NC	I2
34	IEI	TR	I3
35	CLK	RR	I4
36	GND	IRQ	I5
37	D0	IEO	I6
38	D1	IEI	I7
39	D2	CLK	NC
40	D3	GND	TR
41	D4	D0	RR
42	D5	D1	IRQ
43	D6	D2	IEO
44	D7	D3	IEI
45	IACK	D4	CLK
46	DTACK	D5	GND
47	DS	D6	D0
48	CS	D7	D1
49	---	IACK	D2
50	---	DTACK	D3
51	---	DS	D4
52	---	CS	D5

NC = No connection.

FIGURE 2. Terminal connections.

Terminal number	Terminal symbol
	Case outline Z
A2	A5
A3	A4
A4	A2
A5	NC
A6	CS
A7	DTACK
A8	D7
A9	D5
A10	TC
B1	NC
B2	A3
B3	A4
B4	A1
B5	R/W
B6	NC
B7	DS
B8	IACK
B9	D6
B10	NC
B11	NC
C1	SI
C2	SO
C10	D4
C11	NC
D1	NC
D2	RC
D10	D2
D11	D3
E1	NC
E2	VCC
E10	DO
E11	D1
F1	TAO
F2	MPX

Terminal number	Terminal symbol
	Case outline Z
F10	VSS
F11	NC
G1	TCO
G2	TBO
G10	IEI
G11	CLK
H1	XTAL1
H2	TDO
H10	IRQ
H11	IEO
J1	XTAL2
J2	NC
J10	TR
J11	RR
K1	NC
K2	NC
K3	TAI
K4	RESET
K5	I1
K6	NC
K7	I3
K8	I5
K9	I7
K10	NC
K11	NC
L2	NC
L3	TBI
L4	IO
L5	I2
L6	NC
L7	I4
L8	I6
L9	NC
L10	NC

NC = No connection

FIGURE 2. Terminal connections - Continued.

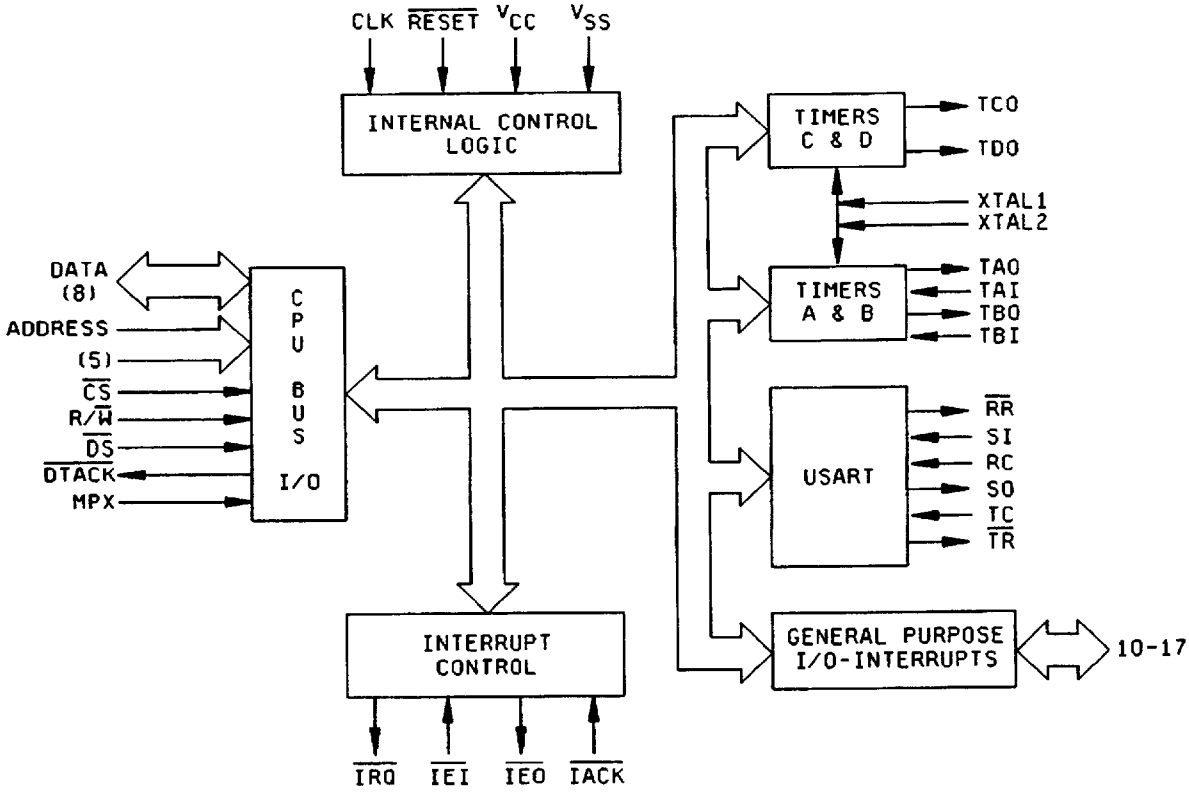
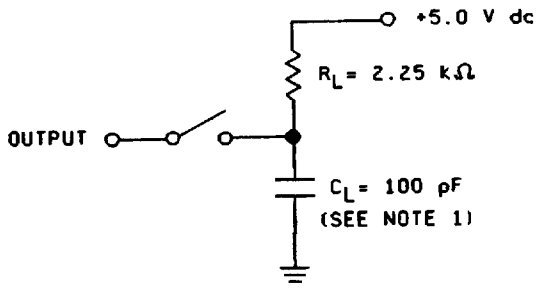
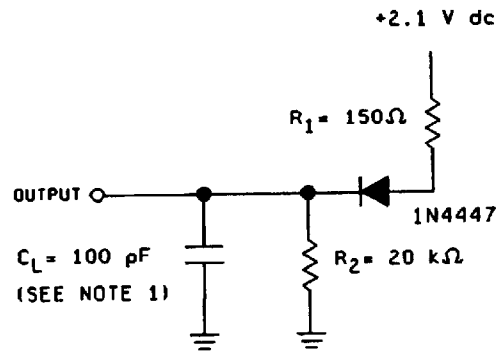


FIGURE 3. Block diagram.

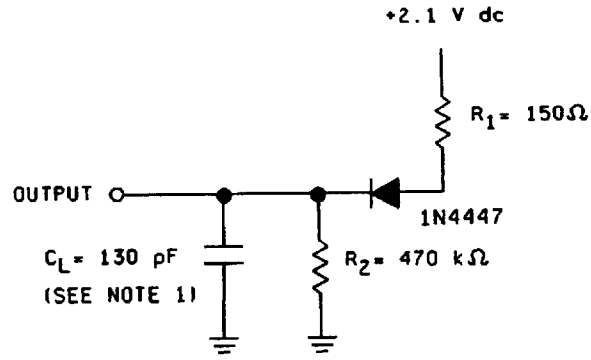
OUTPUT LOAD CIRCUIT FOR $\overline{IRQ}$



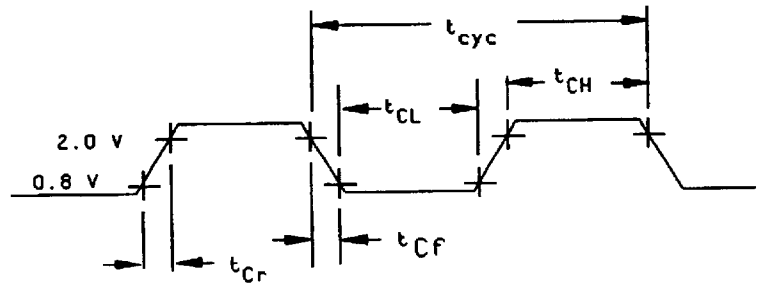
OUTPUT LOAD CIRCUIT FOR ALL OUTPUTS EXCEPT $\overline{DTACK}$



OUTPUT LOAD CIRCUIT FOR $\overline{DTACK}$



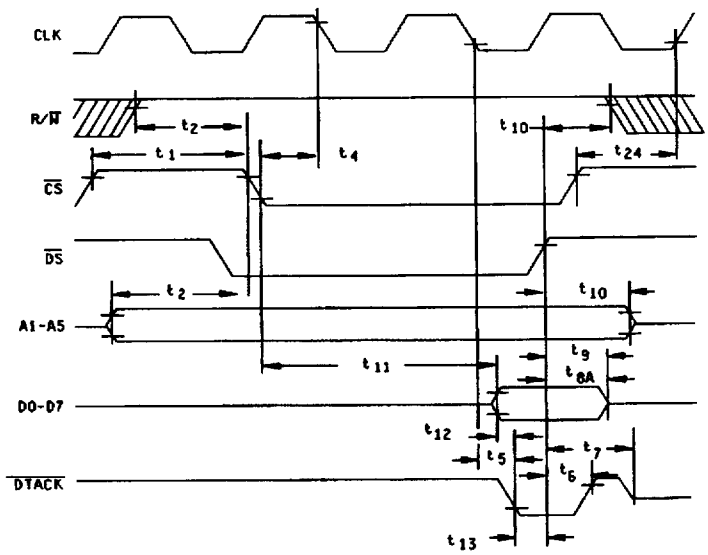
CLOCK INPUT TIMING DIAGRAM



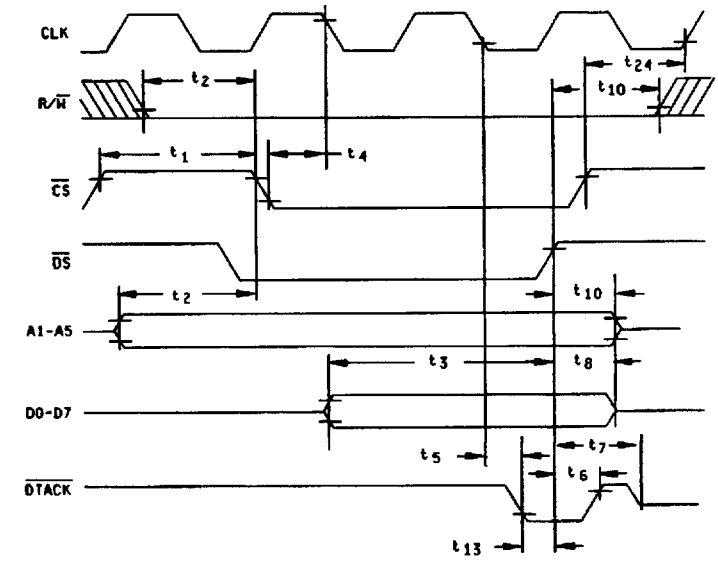
See notes at end of figure.

FIGURE 4. Output load circuits and waveforms.

READ CYCLE TIMING



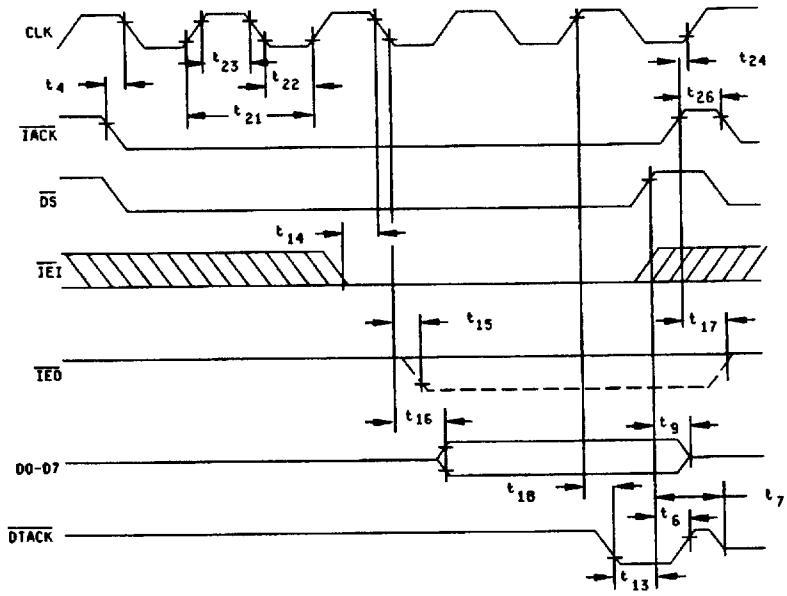
WRITE CYCLE TIMING
(SEE NOTE 2)



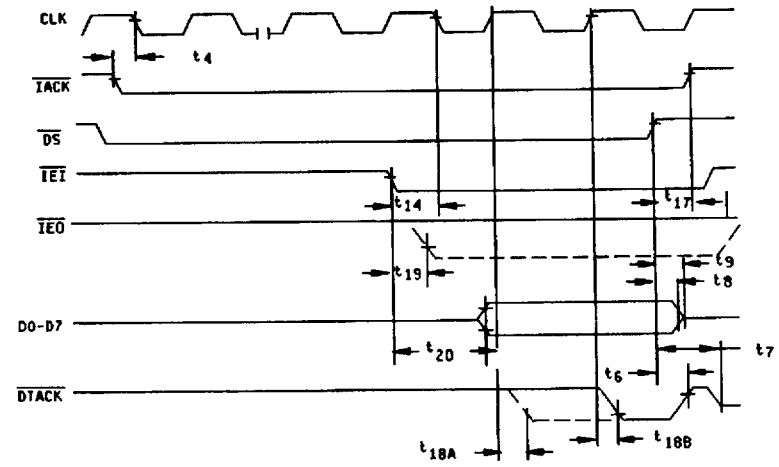
See notes at end of figure.

FIGURE 4. Output load circuits and waveforms - Continued.

INTERRUPT ACKNOWLEDGE CYCLE ($\overline{IEI}$ LOW
(SEE NOTE 3)

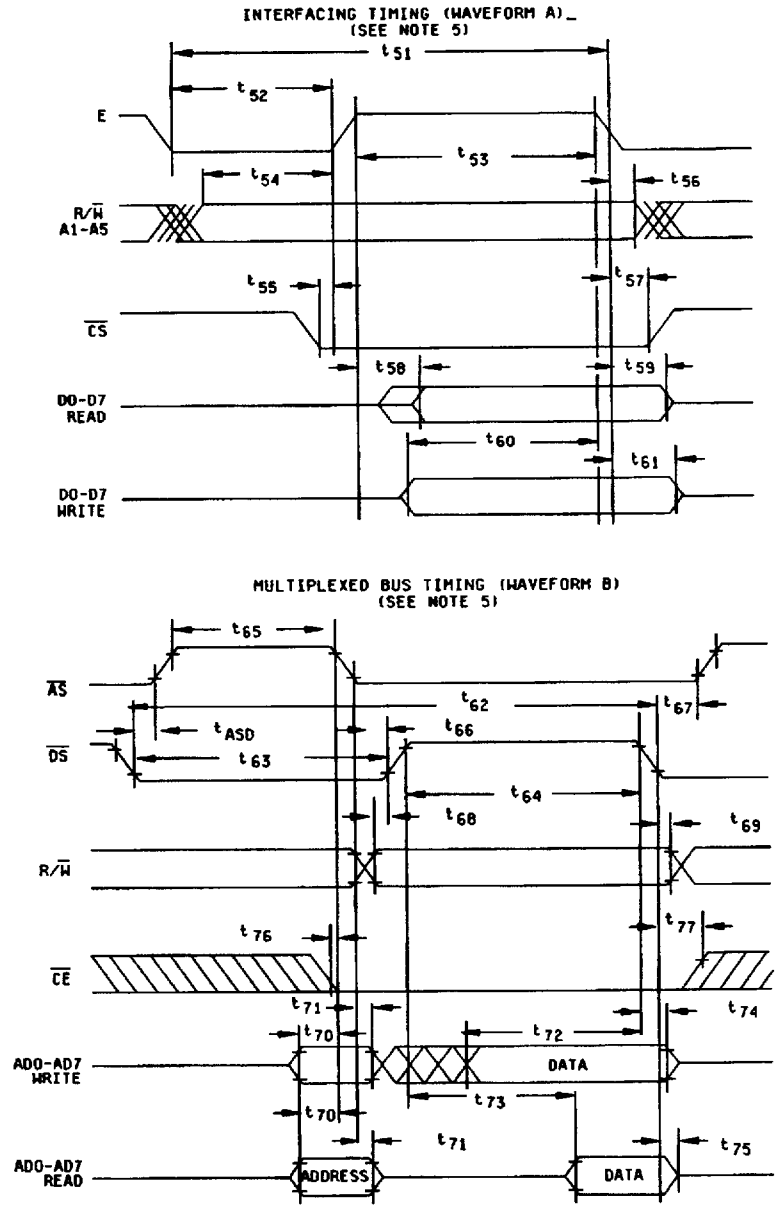


INTERRUPT ACKNOWLEDGE CYCLE ($\overline{IEI}$ HIGH).
(SEE NOTE 4)



See notes at end of figure.

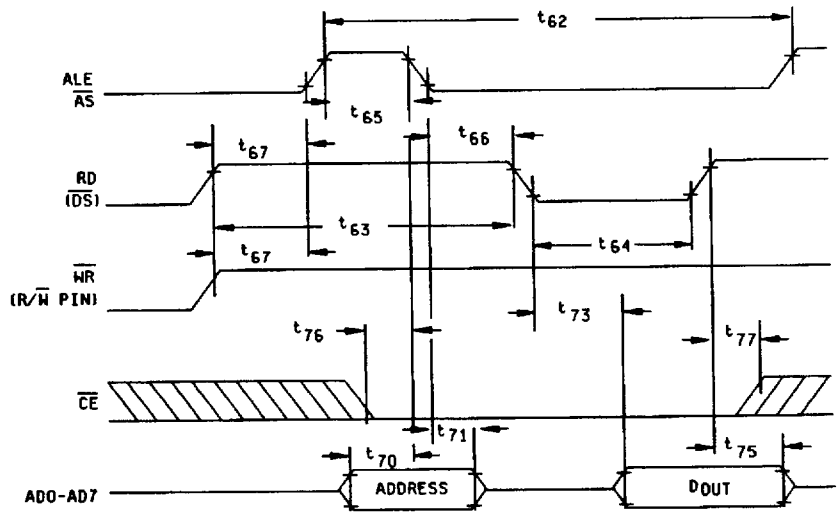
FIGURE 4. Output load circuits and waveforms - Continued.



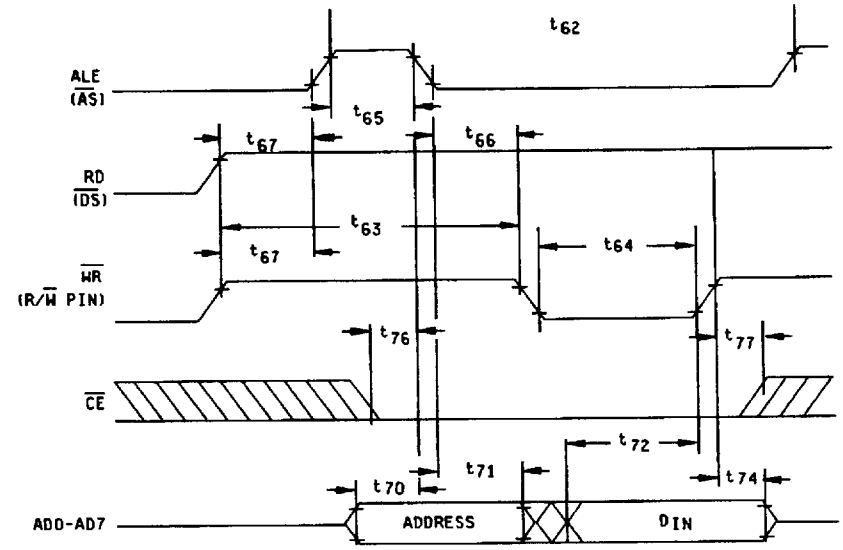
See notes at end of figure.

FIGURE 4. Output load circuits and waveforms - Continued.

MULTIPLEXED BUS TIMING - READ TIMING (WAVEFORM C)
(SEE NOTE 5)

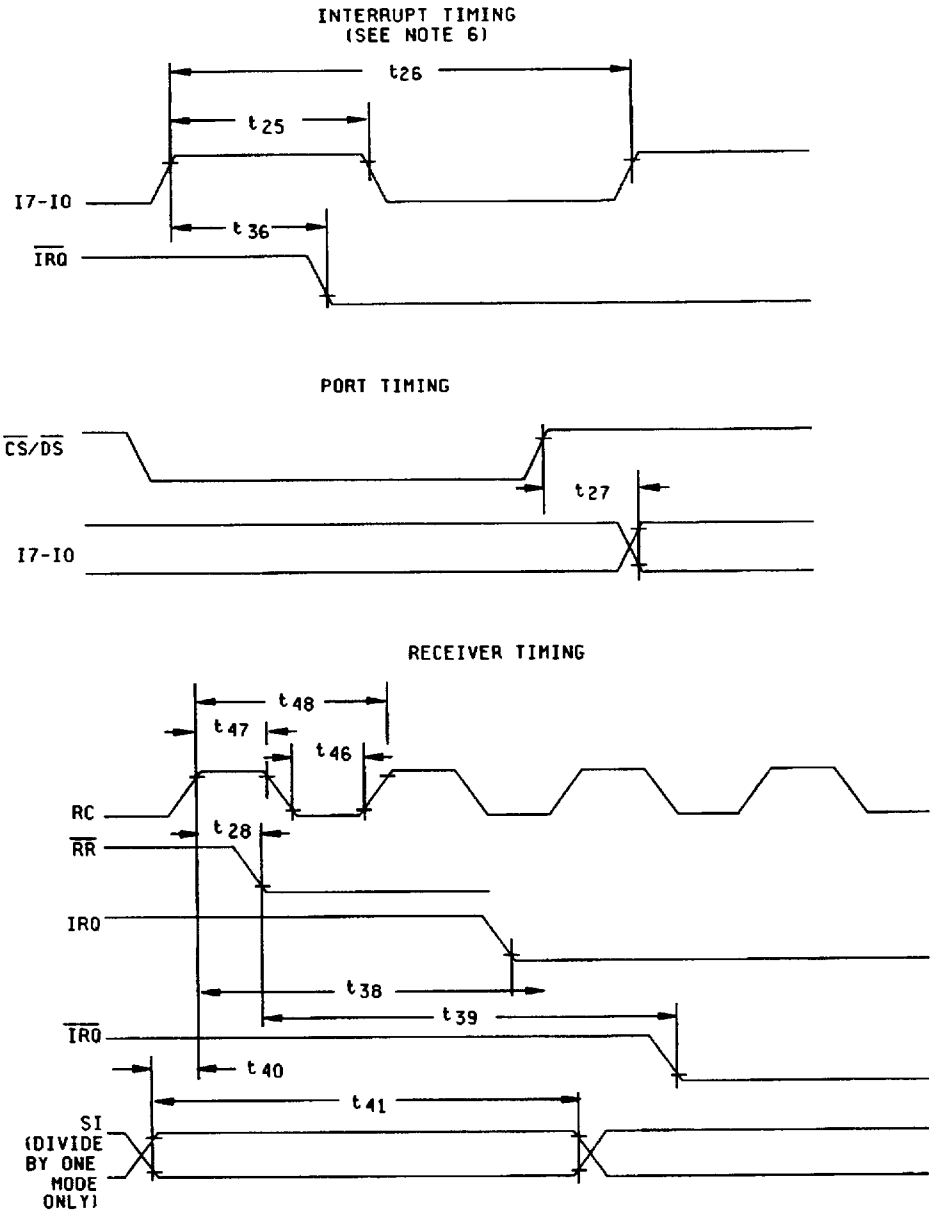


MULTIPLEXED BUS TIMING - WRITE TIMING (WAVEFORM C)
(SEE NOTE 5)



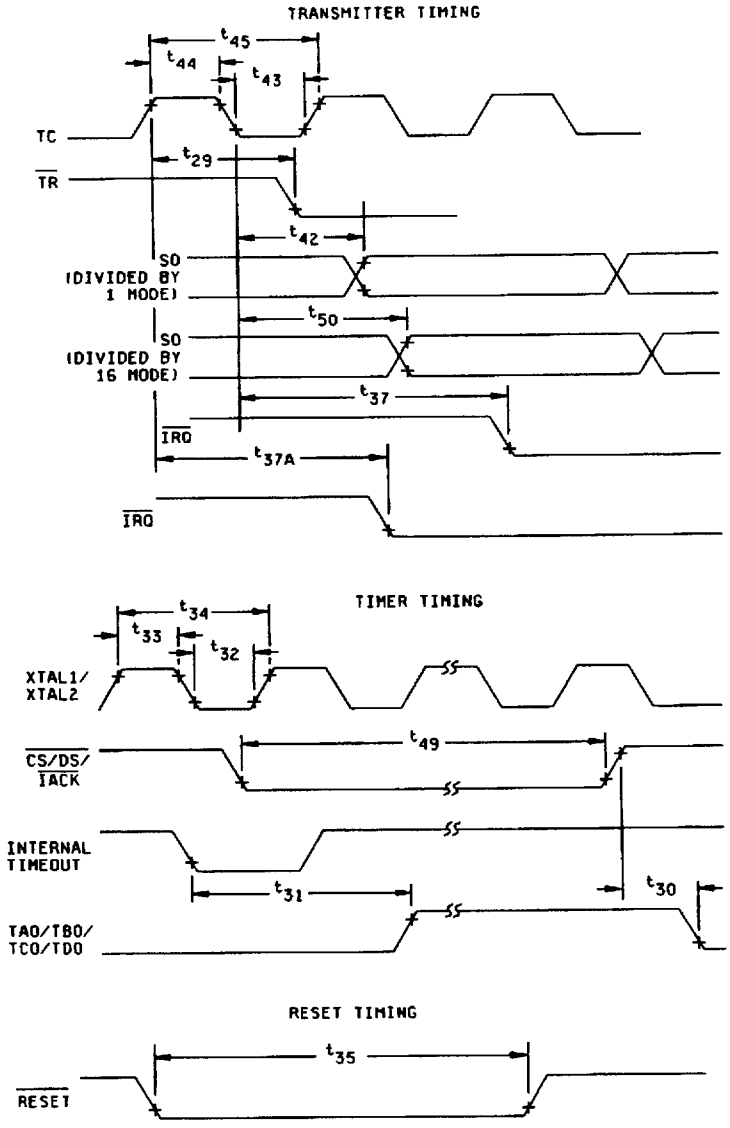
See notes at end of figure.

FIGURE 4. Output load circuits and waveforms - Continued.



See notes at end of figure.

FIGURE 4. Output load circuits and waveforms - Continued.



NOTES:

1/ C_L = load capacitance and includes scope and jig capacitance.

2/ CS and IACK must be a function of DS.

3/ IEO only goes low if no acknowledgeable interrupt is pending. If IEO goes low, DTACK and the data bus remain in the high impedance state.

4/ DTACK will go low at A if specification number 14 is met. Otherwise, DTACK will go low at 8.

5/ See notes in 6.5.2

6/ Active edge is assumed to be the rising edge.

FIGURE 4. Output load circuits and waveforms - Continued.

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)			Subgroups (in accordance with MIL-I-38535, table III)	
	Device class M	Device class B	Device class S	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1,7,9	1,7,9	1,7,9	1,7,9	1,7,9
Final electrical parameters (see 4.2)	1,2,3,7,8,9 10,11 1/	1,2,3,7,8,9 10,11 1/	1,2,3,7,8,9 10,11 2/	1,2,3,7,8,9 10,11 1/	1,2,3,7,8,9 10,11 2/
Group A test requirements (see 4.4)	1,2,3,4,7,8 9,10,11	1,2,3,4,7,8 9,10,11	1,2,3,4,7,8 9,10,11	1,2,3,4,7,8 9,10,11	1,2,3,4,7,8 9,10,11
Group B end point electrical parameters (see 4.4)			2,8a,10		
Group C end point electrical parameters (see 4.4)	2,8a,10	2,8a,10		2,8a,10	2,8a,10
Group D end point electrical parameters (see 4.4)	2,8a,10	2,8a,10	2,8a,10	2,8a,10	2,8a,10
Group E end point electrical parameters (see 4.4)	1,7,9	1,7,9	1,7,9	1,7,9	1,7,9

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1 and 7.

4.4 Conformance inspection. Quality conformance inspection for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein) and as specified herein. Quality conformance inspection for device classes B and S shall be in accordance with MIL-M-38510 and as specified herein. Inspections to be performed for device classes M, B, and S shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5). Technology conformance inspection for classes Q and V shall be in accordance with MIL-I-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-I-38535 permits alternate in-line control testing.

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for initial qualification and after any process or design changes which may affect input or output capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency of 1 MHz. Sample size is 15 devices with no failures, and with all input and output terminals tested.

c. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the functionality of the device. For device classes B and S, subgroups 7 and 8 tests shall be sufficient to verify the functionality of the device as approved by the qualifying activity. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).

4.4.2 Group B inspection. The group B inspection end-point electrical parameters shall be as specified in table II herein. For device class S steady-state life tests, the test circuit shall be submitted to the qualifying activity.

4.4.3 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.3.1 Additional criteria for device classes M and B. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A, B, C, or D. For device class M, the test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. For device class B, the test circuit shall be submitted to the qualifying activity. For device classes M and B, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.3.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-I-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

4.4.4 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.5 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes B, S, Q, and V shall be M, D, R, and H and for device class M shall be M and D.

a. End-point electrical parameters shall be as specified in table II herein.

b. For device classes M, B, and S, the devices shall be subjected to radiation hardness assured tests as specified in MIL-M-38510 for the RHA level being tested. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-I-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510 for device classes M, B, and S and MIL-I-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device classes B and Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).

6.3 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and which SMD's are applicable to that system. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DESC-EC, telephone (513) 296-6047.

6.4 Comments. Comments on this drawing should be directed to DESC-EC, Dayton, Ohio 45444, or telephone (513) 296-5377.

6.5 Symbols, definitions, and functional descriptions.

6.5.1 Pin Descriptions

Pin name	Descriptions
$\overline{CS}$	Chip Select (input, active low). $\overline{CS}$ is used to select the device for accesses to the internal registers. CS and IACK must not be asserted at the same time.
$\overline{DS}$	Data Strobe (input, active low). $\overline{DS}$ is used as part of the chip select and interrupt acknowledge functions.
R/$\overline{W}$	Read/Write (input). R/$\overline{W}$ is the signal from the bus master indicating whether the current bus cycle is a Read (high) or Write (low) cycle.
$\overline{DTACK}$	Data Transfer Acknowledge (output, active low, tri-stateable). $\overline{DTACK}$ is used to signal the bus master that the data is ready, or that data has been accepted by the device.
A1-A5	Address Bus (input). The address bus is used to address one of the internal registers during a read or write cycle.
D0-D7	Data Bus (bi-directions, tri-stateable). The data bus is used to receive data from or transmit data to one of the internal registers during a read or write cycle. It is also used to pass a vector during an interrupt acknowledge cycle.
CLK	Clock (input). This input is used to provide the internal timing for the device.
$\overline{RESET}$	Device reset (input, active low). Reset disables the USART receiver and transmitter, stops all timers and forces the time outputs low, disables all interrupt channels and clears any pending interrupts. The General Purpose Interrupt I/O lines will be placed in the tri-stated input mode. All internal registers (except the timer, USART data registers, and transmit status register) will be cleared.

Pin name	Descriptions
$\overline{IRQ}$	Interrupt Request (output, active low, open drain) $\overline{IRQ}$ is asserted when the device is requesting an interrupt. IRQ is negated during an interrupt acknowledge cycle or by clearing the pending interrupt(s) through software.
$\overline{IACK}$	Interrupt Acknowledge (input, active low). $\overline{IACK}$ is used to signal the device that the CPU is acknowledge an interrupt. CS and IACK must not be asserted at the same time.
$\overline{IEI}$	Interrupt Enable in (input, active low). $\overline{IEI}$ is used to signal the device that no higher priority device is requesting interrupt service.
$\overline{IEO}$	Interrupt Enable Out (output, active low). $\overline{IEO}$ is used to signal lower priority peripherals that neither the device nor another higher priority peripheral is requesting interrupt service.
IO-I7	General Purpose Interrupt I. O. lines. These lines may be used as interrupt inputs and/or I/O lines. When used as interrupt inputs, their active edge is programmable. A data direction register is used to define which lines are to be Hi-Z inputs and which lines are to be push-pull TTL compatible outputs.
SO	Serial Output. This is the output of the USART transmitter. This output is configured by the TSR register.
SI	Serial Input. This is the input to the USART receiver.
RC	Receiver Clock. This input controls the serial bit rate of the USART receiver.
TC	Transmitter Clock. This input controls the serial bit rate of the USART transmitter.
$\overline{RR}$	Receiver Ready (output, active low). DMA output for the receiver, which reflects the same status of Buffer Full in port number 16.
$\overline{TR}$	Transmitter Ready (output, active low). DMA output for transmitter, which reflects the status of Buffer Full in port number 16.
TAO,TBO	Timer Outputs. Each of the four times has an output which can produce a square wave. The TCO, TDO output will change states each timer cycle; thus one full period of the timer out signal is equal to two time cycles. TAO and TBO can be reset (logic "0") by a write to TACR and TBCR respectively.
XTAL1, XTAL2	Time Clock Inputs. A crystal can be connected between XTAL1 and XTAL2, or XTAL1 can be driven with EXTERNAL clock. When driving XTAL1 with EXTERNAL clock, XTAL2 must be allowed to float. When using a crystal, external capacitors are required. All chip accesses are independent of the timer clock.
TAI, TBI	Timer A, B Inputs. Used when running the timers in the event count or the pulse width measurements mode. The interrupt channels associated with 14 and 13 are used for TAI and TBI respectively. Thus, when running a timer in the pulse width measurement mode, 14 or 13 can be used for I/O only.
MPX	This signal selected the data bus mode: MPX = 0 : nonmultiplex mode MPX = 1 : multiplex mode The register select lines RS1-RS55 and the data bus D0-D7 are multiplexed. An address strobe must be connected to the CLK pin.

6.5.2 Definitions

Waveform name	Waveform type
Waveform A	6800 Interface timing
Waveform B	Motorola Bus timing
Waveform C	Intel Bus timing

6.6 One part - one part number system. The one part - one part number system described below has been developed to allow for transitions between identical generic devices covered by the four major microcircuit requirements documents (MIL-M-38510, MIL-H-38534, MIL-I-38535, and 1.2.1 of MIL-STD-883) without the necessity for the generation of unique PIN's. The four military requirements documents represent different class levels, and previously when a device manufacturer upgraded military product from one class level to another, the benefits of the upgraded product were unavailable to the Original Equipment Manufacturer (OEM), that was contractually locked into the original unique PIN. By establishing a one part number system covering all four documents, the OEM can acquire to the highest class level available for a given generic device to meet system needs without modifying the original contract parts selection criteria.

Military documentation format	Example PIN under new system	Manufacturing source listing	Document listing
New MIL-M-38510 Military Detail Specifications (in the SMD format)	5962-XXXXXZZ(B or S)YY	QPL-38510 (Part 1 or 2)	MIL-BUL-103
New MIL-H-38534 Standardized Military Drawings	5962-XXXXXZZ(H or K)YY	QML-38534	MIL-BUL-103
New MIL-I-38535 Standardized Military Drawings	5962-XXXXXZZ(Q or V)YY	QML-38535	MIL-BUL-103
New 1.2.1 of MIL-STD-883 Standardized Military Drawings	5962-XXXXXZZ(M)YY	MIL-BUL-103	MIL-BUL-103

6.7 Sources of supply.

6.7.1 Sources of supply for device classes B and S. Sources of supply for device classes B and S are listed in QPL-38510.

6.7.2 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DESC-EC and have agreed to this drawing.

6.7.3 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-EC.