REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																			
SHEET																			
REV																			
SHEET																			
REV																			
SHEET	15	16	17	18	19														

REV STATUS OF SHEETS	REV														
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY Thomas M. Hess

CHECKED BY Thomas M. Hess

APPROVED BY Monica L. Poelking

DRAWING APPROVAL DATE
93-05-21

REVISION LEVEL

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, DIGITAL, CMOS, MANCHESTER ENCODER-DECODER, MONOLITHIC SILICON

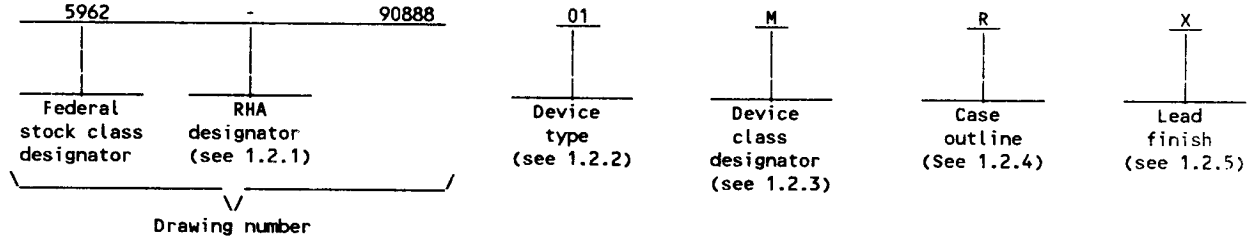
SIZE	CAGE CODE	5962-90888
A	67268	

SHEET 1 OF 19

1. SCOPE

1.1 Scope. This drawing forms a part of a one part - one part number documentation system (see 6.6 herein). Two product assurance classes consisting of military high reliability (device classes B, Q, and M) and space application (device classes S and V), and a choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). Device class M microcircuits represent non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices". When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:



1.2.1 RHA designator. Device classes M, B, and S RHA marked devices shall meet the MIL-M-38510 specified RHA levels and shall be marked with the appropriate RHA designator. Device classes Q and V RHA marked devices shall meet the MIL-I-38535 specified RHA levels and shall be marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	6409	Manchester encoder-decoder

1.2.3 Device class designator. The device class designator shall be a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883
B or S	Certification and qualification to MIL-M-38510
Q or V	Certification and qualification to MIL-I-38535

1.2.4 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
R	GDIP1-T20 or CDIP2-T20	20	Dual-in-line package
2	CQCC1-N20	20	Square leadless chip carrier

1.2.5 Lead finish. The lead finish shall be as specified in MIL-M-38510 for classes M, B, and S or MIL-I-38535 for classes Q and V. Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference.

1.3 Absolute maximum ratings. 1/

Supply voltage . . . . . +7.0 V
Input, Output or I/O voltage range applied . . . . . GND - 0.5 V to V_{CC} + 0.5 V
Storage temperature range . . . . . -65°C to +150°C
Junction temperature . . . . . +175°C
Lead temperature (soldering 10 sec) . . . . . +300°C
Power dissipation
  Case R . . . . . 602 mW
  Case 2 . . . . . 595 mW
Thermal resistance, Junction-to-case . . . . . See MIL-STD-1835

1.4 Recommended operating conditions.

Operating temperature range . . . . . -55°C to +125°C
Supply voltage range . . . . . 4.5 V $\leq V_{CC} \leq$ 5.5 V
Input rise and fall times . . . . . 50 ns max

1.5 Digital logic testing for device classes Q and V.

Fault coverage measurement of manufacturing
  logic tests (MIL-STD-883, test method 5012) . . . . . 2/ percent

2. APPLICABLE DOCUMENTS

2.1 Government specifications, standards, bulletin, and handbook. Unless otherwise specified, the following specifications, standards, bulletin, and handbook of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATIONS

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.
MIL-I-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

MILITARY

MIL-STD-480 - Configuration Control-Engineering Changes, Deviations and Waivers.
MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-1835 - Microcircuit Case Outlines.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

HANDBOOK

MILITARY

MIL-HDBK-780 - Standardized Military Drawings.

(Copies of the specifications, standards, bulletin, and handbook required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ Values will be added when they become available.

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device class M shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein. The individual item requirements for device classes B and S shall be in accordance with MIL-M-38510 and as specified herein. For device classes B and S, a full electrical characterization table for each device type shall be included in this SMD. The individual item requirements for device classes Q and V shall be in accordance with MIL-I-38535, the device manufacturer's Quality Management (QM) plan, and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 for device classes M, B, and S and MIL-I-38535 for device classes Q and V and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Block diagram. The block diagram shall be as specified on figure 2.

3.2.4 Radiation exposure circuit. The radiation exposure circuit shall be specified when available.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. Marking for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein). In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103. Marking for device classes B and S shall be in accordance with MIL-M-38510. Marking for device classes Q and V shall be in accordance with MIL-I-38535.

3.5.1 Certification/compliance mark. The compliance mark for device class M shall be a "C" as required in MIL-STD-883 (see 3.1 herein). The certification mark for device classes B and S shall be a "J" or "JAN" as required in MIL-M-38510. The certification mark for device classes Q and V shall be a "QML" as required in MIL-I-38535.

3.6 Certificate of compliance. For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.7.3 herein). For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.7.2 herein). The certificate of compliance submitted to DESC-EC prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device class M, the requirements of MIL-STD-883 (see 3.1 herein), or for device classes Q and V, the requirements of MIL-I-38535 and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required for device class M in MIL-STD-883 (see 3.1 herein) or device classes B and S in MIL-M-38510 or for device classes Q and V in MIL-I-38535 shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DESC-EC of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-480.

3.9 Verification and review for device class M. For device class M, DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device classes M, B, and S. Device classes M, B, and S devices covered by this drawing shall be in microcircuit group number 105 (see MIL-M-38510, appendix E).

3.11 Serialization for device class S. All device class S devices shall be serialized in accordance with MIL-M-38510.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Input high voltage	V_{IH}	V_{CC} = 4.5 V	1, 2, 3	All	.7 V_{CC}		V
Input low voltage	V_{IL}	V_{CC} = 4.5 V	1, 2, 3	All		.2 V_{CC}	V
Input high voltage $\overline{\text{Reset}}$	V_{IHR}	V_{CC} = 5.5 V	1, 2, 3	All	V_{CC} -0.5		V
Input low voltage $\overline{\text{Reset}}$	V_{ILR}	V_{CC} = 4.5 V	1, 2, 3	All		GND +0.5	V
Input high voltage Clock	V_{IHC}	V_{CC} = 5.5 V	1, 2, 3	All	V_{CC} -0.5		V
Input low voltage Clock	V_{ILC}	V_{CC} = 4.5 V	1, 2, 3	All		GND +0.5	V
Input leakage current (except I_X)	I_I	V_{IN} = V_{CC} or GND V_{CC} = 5.5 V	1, 2, 3	All	-1.0	1.0	µA
Input leakage current (I_X)	I_I	V_{IN} = V_{CC} or GND V_{CC} = 5.5 V	1, 2, 3	All	-20	20	µA
I/O leakage current	I_O	V_{OUT} = V_{CC} or GND V_{CC} = 5.5 V	1, 2, 3	All	-10	10	µA
Output high voltage (All except O_X)	V_{OH}	I_{OH} = -2.0 mA V_{CC} = 4.5 V 2/	1, 2, 3	All	V_{CC} -0.4		V
Output low voltage (All except O_X)	V_{OL}	I_{OH} = 2.0 mA V_{CC} = 4.5 V 2/	1, 2, 3	All		0.4	V
Standby power supply current	I_{CCSB}	V_{OUT} = V_{CC} or GND V_{CC} = 5.5 V Outputs open	1, 2, 3	All		100	µA
Operating power supply current	I_{CCOP}	f = 16 MHz V_{IN} = V_{CC} or GD V_{CC} = 5.5 V, C_L = 50 pF	1, 2, 3	All		18	mA

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Input capacitance	C_{IN}	V_{CC} = Open f = 1 MHz See 4.4.1.c T_A = +25° C	4	All		10	pF
I/O capacitance	$C_{I/O}$		4	All		12	pF
Functional test		V_{CC} = 4.5 V See 4.4.1.b	7, 8	All			
Output rise time (all except clock)	t_r	From 1.0 to 3.5 V C_L = 50 pF 3/	9, 10, 11	All		50	ns
Output fall time (all except clock)	t_f	From 3.5 to 1.0 V C_L = 50 pF 3/	9, 10, 11	All		50	ns
Clock output rise time	t_r	From 1.0 to 3.5 V C_L = 20 pF 3/	9, 10, 11	All		11	ns
Clock output fall time	t_f	From 3.5 to 1.0 V C_L = 20 pF 3/	9, 10, 11	All		11	ns
ECLK to $\overline{BZO}$, $\overline{BOO}$	t_{CE3}	See figure 3 4/ 3/ V_{CC} = 4.5 V	9, 10, 11	All	0.5	1.0	DBP
$\overline{CTS}$ low to $\overline{BZO}$ $\overline{BOO}$ enables	t_{CE4}	See figure 3 4/ 3/ V_{CC} = 4.5 V	9, 10, 11	All	0.5	1.5	DBP
$\overline{CTS}$ low to ECLK enabled	t_{CE5}	See figure 3 4/ 3/ V_{CC} = 4.5 V	9, 10, 11	All	10.5	11.5	DBP
$\overline{CTS}$ high to ECLK disabled	t_{CE6}	See figure 3 4/ 3/ V_{CC} = 4.5 V	9, 10, 11	All		1.0	DBP
$\overline{CTS}$ high to $\overline{BZO}$ $\overline{BOO}$ disabled	t_{CE7}	See figure 3 4/ 3/ V_{CC} = 4.5 V	9, 10, 11	All	1.5	2.5	DBP
UDI to SDO, $\overline{NVM}$	t_{CD1}	See figure 3 4/ 3/ V_{CC} = 4.5 V	9, 10, 11	All	2.5	3.0	DBP

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
$\overline{RST}$ low to DCLK, SDO, NVM low	t_{CD3}	See figure 3 4/ 3/ V_{CC} = 4.5 V	9, 10, 11	All	0.5	1.5	DBP
$\overline{RST}$ high to DCLK, enabled	t_{CD4}	See figure 3 4/ 3/ V_{CC} = 4.5 V	9, 10, 11	All	0.5	1.5	DBP
UDI to $\overline{BZO}$, $\overline{BOO}$	t_{R1}	See figure 3 4/ 3/ V_{CC} = 4.5 V	9, 10, 11	All	0.5	1.0	DBP
UDI to SDO, $\overline{NVM}$	t_{R3}	See figure 3 4/ 3/ V_{CC} = 4.5 V	9, 10, 11	All	2.5	3.0	DBP
Clock frequency	f_C	See figure 3 4/ 5/ V_{CC} = 4.5 V	9, 10, 11	All		16	MHz
Clock period	t_C	See figure 3 4/ 5/ V_{CC} = 4.5 V	9, 10, 11	All	$1/f_C$		s
Bipolar pulse width	t_1	See figure 3 4/ 5/ V_{CC} = 4.5 V	9, 10, 11	All	t_C+10		ns
One-zero overlap	t_3	See figure 3 4/ 5/ V_{CC} = 4.5 V	9, 10, 11	All		t_C-10	ns
Clock high time	t_{CH}	See figure 3 4/ 5/ V_{CC} = 4.5 V f = 16 MHz	9, 10, 11	All	20		ns
Clock low time	t_{CL}	See figure 3 4/ 5/ V_{CC} = 4.5 V f = 16 MHz	9, 10, 11	All	20		ns
Serial data setup time	t_{CE1}	See figure 3 4/ 5/ V_{CC} = 4.5 V	9, 10, 11	All	120		ns
Serial data hold time	t_{CE2}	See figure 3 4/ 5/ V_{CC} = 4.5 V	9, 10, 11	All	0		ns
DCLK to SDO, $\overline{NVM}$	t_{CD2}	See figure 3 4/ 5/ V_{CC} = 4.5 V	9, 10, 11	All		40	ns

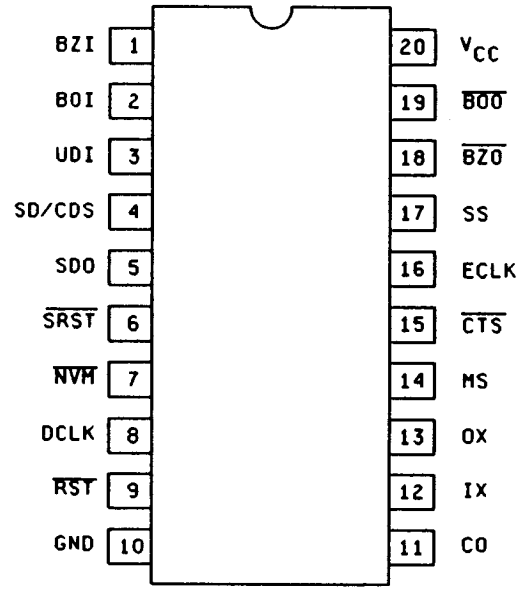
See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
ECLK to $\overline{BZO}$	t_{R2}	See figure 3 4/ 5/ V_{CC} = 4.5 V	9, 10, 11	All		40	ns

1/ Unless otherwise specified, all testing to be performed using worst-case test conditions.
2/ Interchanging of force and sense conditions is permitted.
3/ Guaranteed but not tested.
4/ Data Bit Period (DBP), clock rate = 16x, one DBP = 16 clock cycles; clock rate = 32x, one DBP = 32 clock cycles.
5/ Unless otherwise specified tested at f = 4.0 MHz, V_{IH} = 70% V_{CC}, V_{IL} = 20% V_{CC}, speed select = 16x, $V_{OH} \ge V_{CC}/2$, $V_{OL} \le V_{CC}/2$, V_{CC} = 4.5 V and 5.5 V, input rise and fall times driven at 1 ns/V.

Case R



Case 2

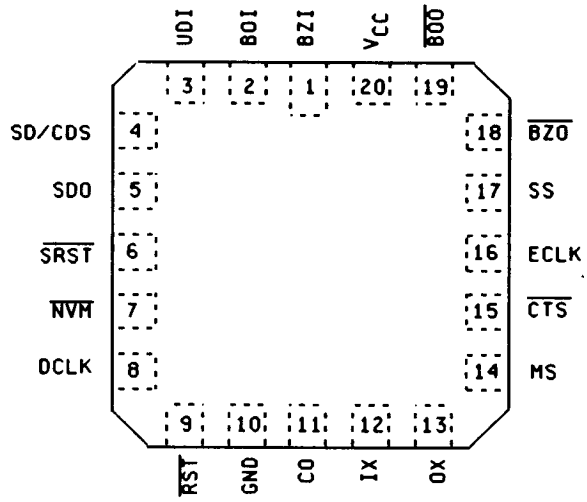


FIGURE 1. Terminal connections.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-90888
		REVISION LEVEL	SHEET 9

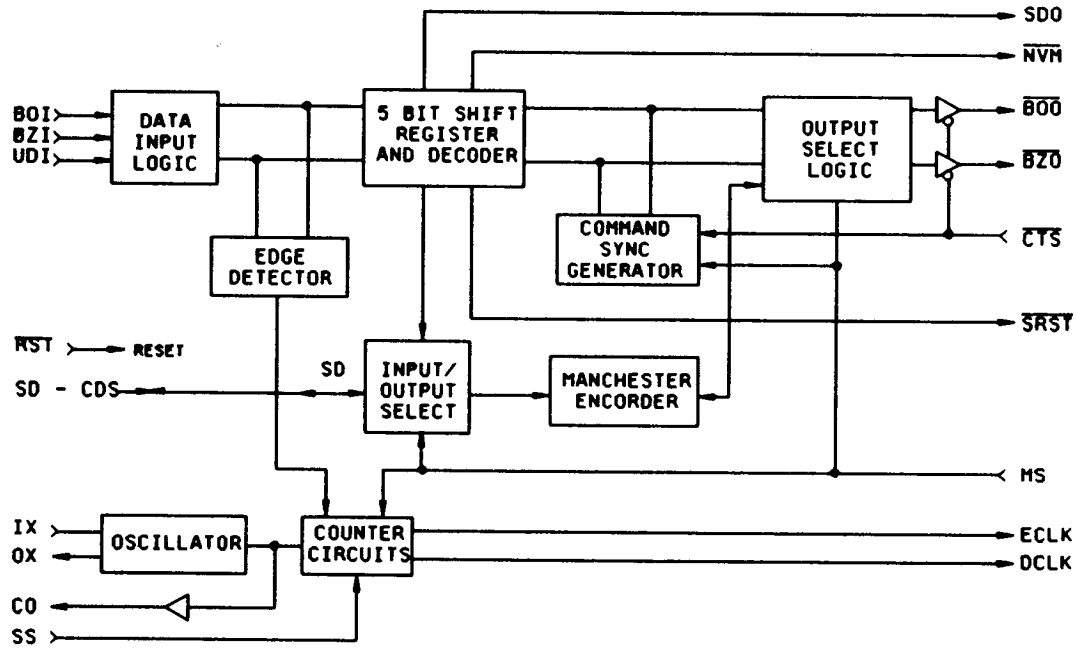
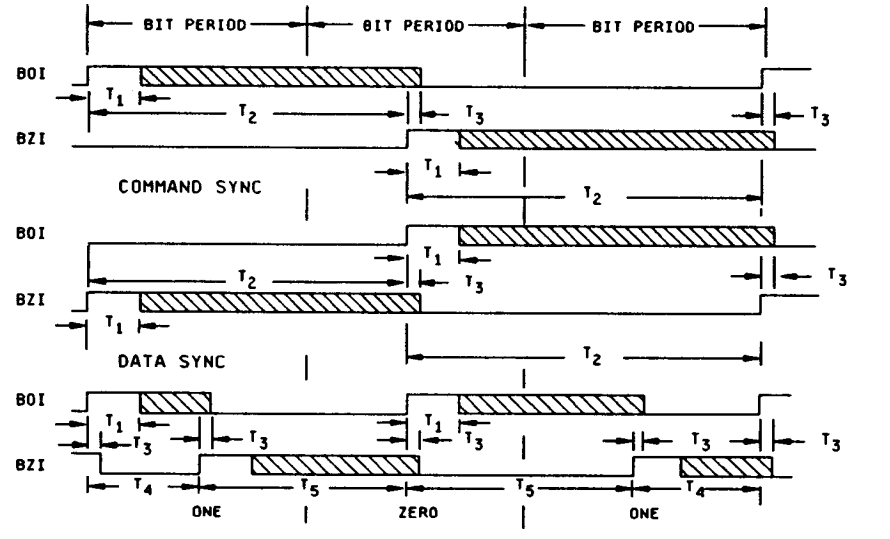
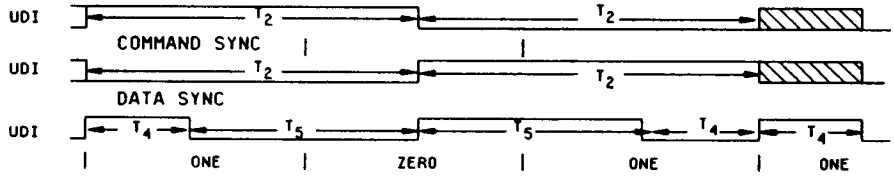


FIGURE 2. Block diagram.

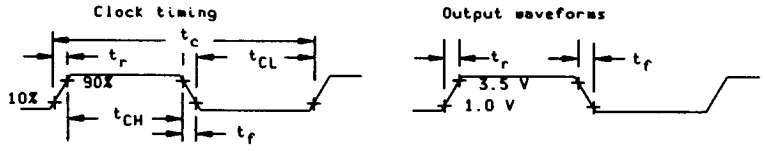
STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-90888
		REVISION LEVEL	SHEET 10



NOTE: UDI = 0, for next diagrams.



NOTE: BOI = 0 AND BZI = 1 for next diagrams.



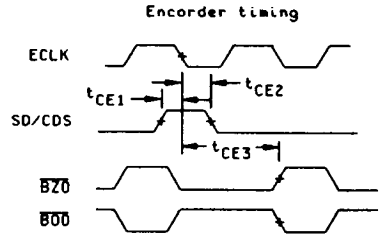
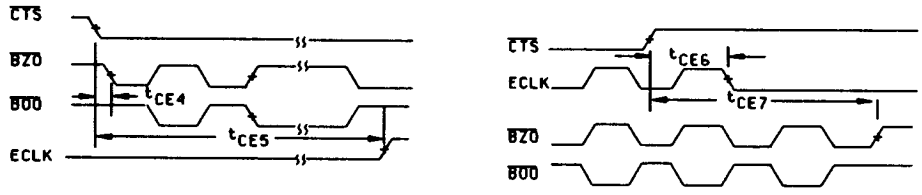
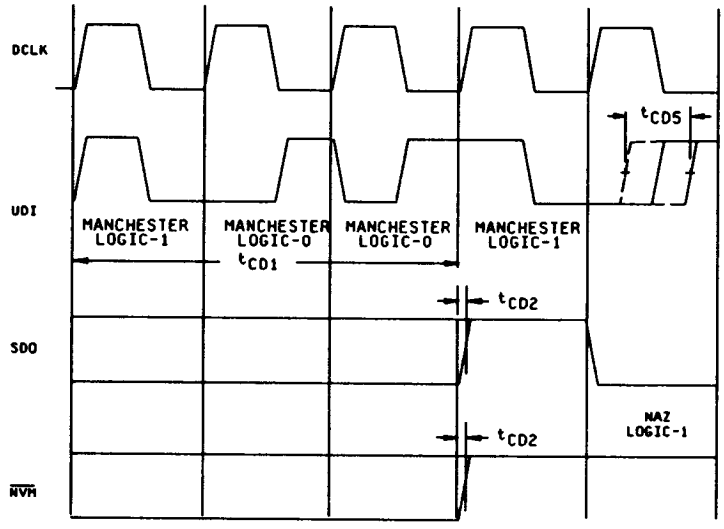


FIGURE 3. Timing waveforms.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-90888
		REVISION LEVEL	SHEET 11

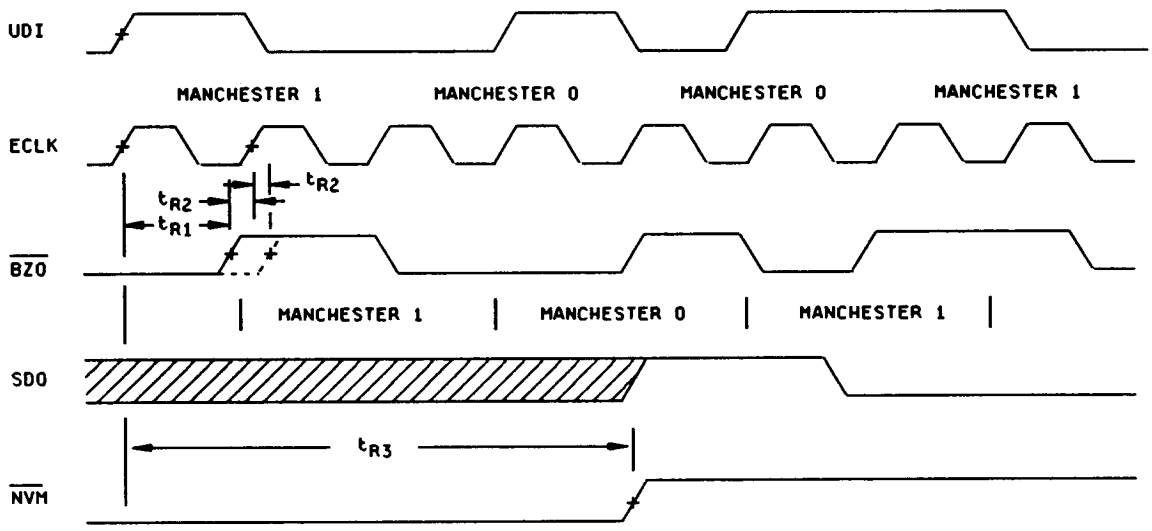


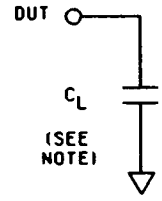
Decoder timing



NOTE: Manchester data in is not synchronous with decoder clock. Decoder clock is synchronous with decoded NAZ out of SDO.

FIGURE 3. Timing waveforms - Continued.





NOTE: Includes stray and jig capacitance, C_L = 50 pF

FIGURE 3. Timing waveforms - Continued.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device class M, sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein). For device classes B and S, sampling and inspection procedures shall be in accordance with MIL-M-38510 and method 5005 of MIL-STD-883, except as modified herein. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-I-38535 and the device manufacturer's QM plan.

4.2 Screening. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. For device classes B and S, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to qualification and quality conformance inspection. For device classes Q and V, screening shall be in accordance with MIL-I-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes M, B, and S.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C or D. For device class M, the test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. For device classes B and S, the test circuit shall be submitted to the qualifying activity. For device classes M, B, and S, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-I-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in appendix B of MIL-I-38535.

4.3 Qualification inspection.

4.3.1 Qualification inspection for device classes B and S. Qualification inspection for device classes B and S shall be in accordance with MIL-M-38510. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5).

4.3.2 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-I-38535. Inspections to be performed shall be those specified in MIL-I-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5).

4.4 Conformance inspection. Quality conformance inspection for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein) and as specified herein. Quality conformance inspection for device classes B and S shall be in accordance with MIL-M-38510 and as specified herein. Inspections to be performed for device classes M, B, and S shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5). Technology conformance inspection for classes Q and V shall be in accordance with MIL-I-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-I-38535 permits alternate in-line control testing.

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table. For device classes B and S, subgroups 7 and 8 tests shall be sufficient to verify the truth table as approved by the qualifying activity. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).

c. Subgroups 4(C_{IN} and $C_{I/O}$) shall be measured only for the initial test and after process or design changes which may affect capacitance. A minimum sample size of five devices with zero defects shall be required.

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)			Subgroups (in accordance with MIL-I-38535, table III)	
	Device class M	Device class B	Device class S	Device class Q	Device class V
Interim electrical parameters (see 4.2)			1, 7, 9		1, 7, 9
Final electrical parameters (see 4.2)	1, 2, 3, 7 1/ 8,9,10,11	1, 2, 3 7 1/ 8,9,10,11	1, 2, 3 7 2/ 8,9,10,11	1, 2, 3 7 1/ 8,9,10,11	1, 2, 3 7 2/ 8,9,10,11
Group A test requirements (see 4.4)	1,2,3,4 7, 8 9,10,11	1,2,3,4 7, 8 9,10,11	1,2,3,4 7, 8 9,10,11	1,2,3,4 7, 8 9,10,11	1,2,3,4 7, 8 9,10,11
Group B end-point electrical parameters (see 4.4)			1, 7, 9		
Group C end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9	1, 7, 9	1, 7, 9	1, 7, 9
Group D end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9	1, 7, 9	1, 7, 9	1, 7, 9
Group E end-point electrical parameters (see 4.4)	---	---	---	---	---

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1 and 7.

4.4.2 Group B inspection. The group B inspection end-point electrical parameters shall be as specified in table II herein. For device class S steady-state life tests, the test circuit shall be submitted to the qualifying activity.

4.4.3 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.3.1 Additional criteria for device classes M and B. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A, B, C, or D. For device class M, the test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. For device class B, the test circuit shall be submitted to the qualifying activity. For device classes M and B, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.3.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-I-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

4.4.4 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.5 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes B, S, Q, and V shall be M, D, R, and H and for device class M shall be M and D.

a. End-point electrical parameters shall be as specified in table II herein.

b. For device classes M, B, and S, the devices shall be subjected to radiation hardness assured tests as specified in MIL-M-38510 for the RHA level being tested. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-I-38535 for the RHA environment and level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510 for device classes M, B, and S and MIL-I-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device classes B and Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).

6.3 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and which SMD's are applicable to that system. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DESC-EC, telephone (513) 296-6047.

6.4 Comments. Comments on this drawing should be directed to DESC-EC, Dayton, Ohio 45444, or telephone (513) 296-5377.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-M-38510 and MIL-STD-1331 and Table III.

Table III. Pin descriptions

Symbol	Name	Description
BZI	Bipolar Zero Input	Used in conjunction with pin 2, bipolar one input (BOI), to input Manchester encoder data to the decoder. BZI and BOI are logical complements. When using pin 3, unipolar data input (UDI) for data input, BZI must be held high.
BOI	Bipolar One Input	Used in conjunction with pin 1, Bipolar Zero Input (BZI) to input Manchester encoded data to the decoder, BOI and BZI are logical complements. When using pin 3, Unipolar Data Inputs (UDI) for data input, BOI must be held low.
UDI	Unipolar Data Input	An alternate to bipolar input (BZI,BOI), Unipolar Data Input (UDI) is used to input Manchester encoded data to the decoder. When using pin 1, (BZI) and pin 2 (BOI) for data input, UDI must be held low.
SD/CDS	Serial Data/Command Data Sync	In the converter mode, SD/CDS is an input used to receive serial NRZ data. NRZ data is accepted synchronously on the falling edge of encoder clock output (ECLK). In the repeater mode, SD/CDS is an output indicating the status of last valid sync pattern received. A high indicates a command sync and a low indicates a data sync pattern.
SDO	Serial Data Out	The decoded serial NRZ data is transmitted out synchronously with the decoder clock (DCLK). SDO is forced low when RST is low.
$\overline{\text{SRST}}$	Serial Reset	In the converter mode, $\overline{\text{SRST}}$ follows $\overline{\text{RST}}$. In the repeater mode when $\overline{\text{RST}}$ goes low, SRST goes low and remains low after RS goes high. SRST goes high only when RST is high, The reset bit is zero and a valid synchronization sequence is received.
$\overline{\text{NVM}}$	Nonvalid Manchester	A low on $\overline{\text{NVM}}$ indicates that the decoder has received invalid Manchester data and present data on Serial Data Out (SDO) is invalid. A high indicates that the sync pulse and data were valid and SDO is valid. NVM is set low by a low on RST and remains low after RST goes high until valid sync pulse followed by two valid Manchester bits is received.
$\overline{\text{RST}}$	Reset	In the converter mode, a low on $\overline{\text{RST}}$ forces SDO, DCLK, $\overline{\text{NVM}}$ and $\overline{\text{SRST}}$ low. A high on $\overline{\text{RST}}$ enables SDO and DCLK , and forces SRST high. NVM remains low after RST goes high until a valid sync pulse followed by two Manchester bits are received, after which it goes high. In the repeater mode, $\overline{\text{RST}}$ has the same effect on SDO, DCLK and NVM as in the converter mode. When RST goes low, $\overline{\text{SRST}}$ goes low and remains low after RST goes high, SRST goes high only when RST is high, the reset bit is zero and a valid synchronization sequence is received.
DCLK	Decoder Clock	The decoder clock is a 1x clock recovered from BZI and BOI to synchronously output received NRZ data (SDO).

Table III. Pin descriptions. - Continued

Symbol	Name	Description
GND	Ground	Ground
C_O	Clock Output	Buffered output of clock input I_X, may be used as clock signal for other peripherals.
I_X	Clock Input	I_X is the input for an external clock or, if the internal oscillator is used, I_X and O_X are used for the connection of the crystal.
O_X	Clock Drive	If the internal oscillator is used, O_X and I_X are used for the connection of the crystal.
MS	Mode Select	MS must be held low for operation in the converter mode, and high for operation in the repeater mode.
$\overline{CTS}$	Clear to Send	In the converter mode, a high disables the encoder, forcing outputs $\overline{BOO}$, BZO high and ECLK low. A high to low transition of CTS initiates transmission of a command sync pulse. A low on CTS enables BOO, BZO and ECLK. In the repeater mode, the function of CTS is identical to that of the converter mode with the exception that a transition of CTS does not initiate a synchronization sequence.
ECLK	Encoder Clock	In the converter mode, ECLK is a 1X clock output used to receive serial NRZ data to SD/CDS. In the repeater mode, ECLK is a 2X clock which is recovered from BZI and BOI data by the digital phase locked loop.
SS	Speed Select	A logic high on SS sets the data rate at 1/32 times the clock frequency while a low sets the data rate at 1/16 times the clock frequency.
$\overline{BZO}$	$\overline{\text{Bipolar Zero Output}}$	$\overline{BZO}$ and its logical complement $\overline{BOO}$ are the Manchester data outputs of the encoder. The inactive state for these outputs is in the high state.
$\overline{BOO}$	$\overline{\text{Bipolar One Out}}$	See $\overline{BZO}$
V_{CC}	Supply Voltage	V_{CC} is the +5 V power supply pin. A 0.1 μF decoupling capacitor from V_{CC} (pin 20) to GND (pin 10) is recommended.

6.6 One part - one part number system. The one part - one part number system described below has been developed to allow for transitions between identical generic devices covered by the four major microcircuit requirements documents (MIL-M-38510, MIL-H-38534, MIL-I-38535, and 1.2.1 of MIL-STD-883) without the necessity for the generation of unique PIN's. The four military requirements documents represent different class levels, and previously when a device manufacturer upgraded military product from one class level to another, the benefits of the upgraded product were unavailable to the Original Equipment Manufacturer (OEM), that was contractually locked into the original unique PIN. By establishing a one part number system covering all four documents, the OEM can acquire to the highest class level available for a given generic device to meet system needs without modifying the original contract parts selection criteria.

Military documentation format	Example PIN under new system	Manufacturing source listing	Document listing
New MIL-M-38510 Military Detail Specifications (in the SMD format)	5962-XXXXXZZ(B or S)YY	QPL-38510 (Part 1 or 2)	MIL-BUL-103
New MIL-H-38534 Standardized Military Drawings	5962-XXXXXZZ(H or K)YY	QML-38534	MIL-BUL-103
New MIL-I-38535 Standardized Military Drawings	5962-XXXXXZZ(Q or V)YY	QML-38535	MIL-BUL-103
New 1.2.1 of MIL-STD-883 Standardized Military Drawings	5962-XXXXXZZ(M)YY	MIL-BUL-103	MIL-BUL-103

6.7 Sources of supply.

6.7.1 Sources of supply for device classes B and S. Sources of supply for device classes B and S are listed in QPL-38510.

6.7.2 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DESC-EC and have agreed to this drawing.

6.7.3 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-EC.