REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																				
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SHEET	15	16																		

REV STATUS OF SHEETS	REV														
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

SC N/A

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DRAWING APPROVAL DATE
92-10-26

REVISION LEVEL

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUITS, DIGITAL, CMOS, OCTAL REGISTERED TRANSCEIVER, MONOLITHIC SILICON

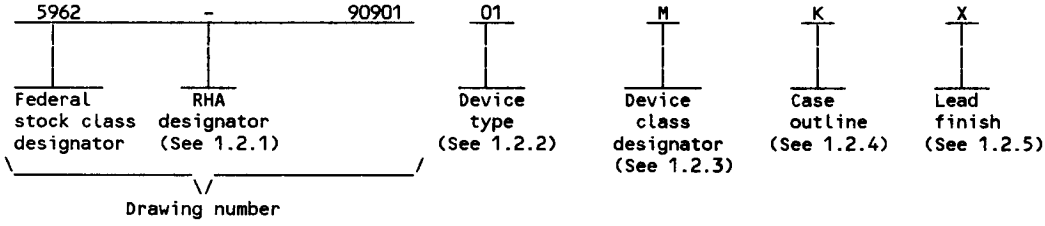
SIZE	CAGE CODE	5962-90901
A	67268	

SHEET 1 OF 16

1. SCOPE

1.1 Scope. This drawing forms a part of a one part - one part number documentation system (see 6.6 herein). Two product assurance classes consisting of military high reliability (device classes B, Q, and M) and space application (device classes S and V), and a choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). Device class M microcircuits represent non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices". When available, a choice of radiation hardness assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:



1.2.1 RHA designator. Device classes M, B, and S RHA marked devices shall meet the MIL-M-38510 specified RHA levels and shall be marked with the appropriate RHA designator. Device classes Q and V RHA marked devices shall meet the MIL-I-38535 specified RHA levels and shall be marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	29FCT52A/54FCT52A	Octal registered transceiver with three-state outputs
02	29FCT52B/54FCT52B	Octal registered transceiver with three-state outputs
03	29FCT52C/54FCT52C	Octal registered transceiver with three-state outputs

1.2.3 Device class designator. The device class designator shall be a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883
B or S	Certification and qualification to MIL-M-38510
Q or V	Certification and qualification to MIL-I-38535

1.2.4 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package type
K	GDFP2-F24 or CDFP3-F24	24	flat pack
L	GDIP3-T24 or CDIP4-T24	24	dual-in-line
3	CQCC1-N28	28	leadless chip carrier

1.2.5 Lead finish. The lead finish shall be as specified in MIL-M-38510 for classes M, B, and S or MIL-I-38535 for classes Q and V. Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference.

1.3 Absolute maximum ratings. 1/

Terminal voltage range (V_{TERM}) (referenced to ground):	
Inputs and V_{CC} terminals	-0.5 V dc to +7.0 V dc
Outputs and I/O terminals	-0.5 V dc to V_{CC}
Storage temperature range (T_{STG})	-65°C to +150°C
Bias temperature range (T_{BIAS})	-65°C to +135°C
DC output current (I_{OUT})	120 mA
Power dissipation (P_D)	500 mW
Junction temperature	+175°C
Thermal resistance (Θ_{JC})	See MIL-STD-1835
Lead temperature (soldering, 10 seconds)	+275°C

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	4.5 V dc to 5.5 V dc
High-level input voltage (V_{IH})	2.0 V dc minimum
Low-level input voltage (V_{IL})	0.8 V dc maximum
Case operating temperature range (T_C)	-55°C to +125°C

1.5 Digital logic testing for device classes Q and V.

Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012)	XX percent 2/

2. APPLICABLE DOCUMENTS

2.1 Government specifications, standards, bulletin, and handbook. Unless otherwise specified, the following specifications, standards, bulletin, and handbook of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATIONS

MILITARY

MIL-M-38510	-	Microcircuits, General Specification for.
MIL-I-38535	-	Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

MILITARY

MIL-STD-480	-	Configuration Control-Engineering Changes, Deviations and Waivers.
MIL-STD-883	-	Test Methods and Procedures for Microelectronics.
MIL-STD-1835	-	Microcircuit Case Outlines.

BULLETIN

MILITARY

MIL-BUL-103	-	List of Standardized Military Drawings (SMD's).

HANDBOOK

MILITARY

MIL-HDBK-780	-	Standardized Military Drawings.

(Copies of the specifications, standards, bulletin, and handbook required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

2/ Values will be added when they become available.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device class M shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein. The individual item requirements for device classes B and S shall be in accordance with MIL-M-38510 and as specified herein. For device classes B and S, a full electrical characterization table for each device type shall be included in this SMD. The individual item requirements for device classes Q and V shall be in accordance with MIL-I-38535, the device manufacturer's Quality Management (QM) plan, and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 for device classes M, B, and S and MIL-I-38535 for device classes Q and V and herein.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth tables. The truth tables shall be as specified on figure 2.

3.2.4 Logic diagram. The logic diagram shall be as specified on figure 3.

3.2.5 Radiation exposure circuit. The radiation exposure circuit shall be specified when available.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. Marking for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein). In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103. Marking for device classes B and S shall be in accordance with MIL-M-38510. Marking for device classes Q and V shall be in accordance with MIL-I-38535.

3.5.1 Certification/compliance mark. The compliance mark for device class M shall be a "C" as required in MIL-STD-883 (see 3.1 herein). The certification mark for device classes B and S shall be a "J" or "JAN" as required in MIL-M-38510. The certification mark for device classes Q and V shall be a "QML" as required in MIL-I-38535.

3.6 Certificate of compliance. For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.7.3 herein). For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.7.2 herein). The certificate of compliance submitted to DESC-EC prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device class M the requirements of MIL-STD-883 (see 3.1 herein), or for device classes Q and V, the requirements of MIL-I-38535 and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required for device class M in MIL-STD-883 (see 3.1 herein) or device classes B and S in MIL-M-38510 or for device classes Q and V in MIL-I-38535 shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DESC-EC of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-480.

3.9 Verification and review for device class M. For device class M, DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device classes M, B, and S. Device classes M, B, and S devices covered by this drawing shall be in microcircuit group number 105 (see MIL-M-38510, appendix E).

3.11 Serialization for device class S. All device class S devices shall be serialized in accordance with MIL-M-38510.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified 1/		Group A subgroups	Device type	Limits		Unit
						Min	Max	
Input high voltage	V_{IH}			1,2,3	All	2.0	$V_{CC}+0.5$	V
Input low voltage	V_{IL}			1,2,3	All	-0.5	0.8	V
Output high voltage	V_{OH}	V_{CC} = 3 V, V_{IN} = 0.2 V, 2.8 V	I_{OH} = -32 µA	1,2,3	All	2.8		V
		V_{CC} = 4.5 V, V_{IN} = V_{IH}, V_{IL}	I_{OH} = -300 µA	1,2,3	All	4.3		V
			I_{OH} = -15 mA	1,2,3	All	2.4		V
Output low voltage	V_{OL}	V_{CC} = 3 V, V_{IN} = 0.2 V, 2.8 V	I_{OL} = 300 µA	1,2,3	All		0.2	V
		V_{CC} = 4.5 V, V_{IN} = V_{IH}, V_{IL}	I_{OL} = 300 µA	1,2,3	All		0.2	V
			I_{OL} = 48 mA	1,2,3	All		0.55	V
Clamp diode voltage	V_{CD}	V_{CC} = 4.5 V, I_{IN} = -18 mA		1,2,3	All		-1.2	V
Input high current (except I/O pins)	I_{IH}	V_{CC} = 5.5 V	V_{IN} = V_{CC}	1,2,3	All		5	µA
			V_{IN} = 2.7 V 2/	1,2,3	All		5	µA
Input high current (I/O pins only)			V_{IN} = V_{CC}	1,2,3	All		15	µA
			V_{IN} = 2.7 V 2/	1,2,3	All		15	µA
Input low current (except I/O pins)	I_{IL}		V_{IN} = GND	1,2,3	All		-5	µA
			V_{IN} = 0.5 V 2/	1,2,3	All		-5	µA
Input low current (I/O pins only)			V_{IN} = GND	1,2,3	All		-15	µA
			V_{IN} = 0.5 V 2/	1,2,3	All		-15	µA
Short circuit current	I_{OS}	V_{CC} = 5.5 V, V_{OUT} = GND 3/		1,2,3	All	-60		mA
Quiescent power supply current	I_{CC}	V_{CC} = 5.5 V, $V_{IN} \ge 5.3$ V, $V_{IN} \le 0.2$ V, f = 0 MHz, outputs open		1,2,3	All		1.5	mA
Quiescent power supply current, TTL inputs high	ΔI_{CC}	V_{CC} = 5.5 V, V_{IN} = 3.4 V, f = 0 MHz, outputs open 4/		1,2,3	All		2.0	mA
Dynamic power supply current	I_{CCD}	V_{CC} = 5.5 V, outputs open, one input toggling, $\overline{OE}$ = GND, 50% duty cycle, $V_{IN} \ge 5.3$ V, $V_{IN} \le 0.2$ V 5/		1,2,3	All		0.25	mA/MHz

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified 1/		Group A subgroups	Device type	Limits		Unit
						Min	Max	
Total power supply current	I_C 6/	V_{CC} = 5.5 V, outputs open, f_{CP} = 10 MHz, 50% duty cycle, $\overline{OE}$ = GND, one bit toggling at f_i = 5 MHz 50% duty cycle	$V_{IN} \ge 5.5$ V, $V_{IN} \le 0.2$ V	1,2,3	All		4.0	mA
			V_{IN} = 3.4 V, V_{IN} = GND	1,2,3	All		6.0	mA
		V_{CC} = 5.5 V, outputs open, f_{CP} = 10 MHz, 50% duty cycle $\overline{OE}$ = GND, eight bits toggling at f_i = 2.5 MHz 50% duty cycle	$V_{IN} \ge 5.3$ V, $V_{IN} \le 0.2$ V	1,2,3	All		7.8	mA
			V_{IN} = 3.4 V, V_{IN} = GND	1,2,3	All		16.8	mA
Input capacitance	C_{IN}	All input terminals, see 4.4.1c		4	All		10	pF
I/O capacitance	$C_{I/O}$	All I/O terminals, see 4.4.1c		4	All		12	pF
Functional tests		V_{CC} = 4.5 V, 5.5 V; see 4.4.1b		7,8	All			
Propagation delay CPA, CPB to A_N, B_N	t_{PLH}, t_{PHL} 7/	C_L = 50 pF, R_L = 500Ω, see figure 4		9,10,11	01	2.0	11.0	ns
					02	2.0	8.0	ns
					03	2.0	7.3	ns
Output enable time $\overline{OEA}$, OEB to A_N, B_N valid	t_{PZH}, t_{PZL} 7/			9,10,11	01	1.5	13.0	ns
					02	1.5	8.5	ns
					03	1.5	8.0	ns
Output disable time $\overline{OEA}$, OEB to A_N, B_N high-impedance	t_{PHZ}, t_{PLZ} 7/			9,10,11	01	1.5	10.0	ns
					02	1.5	8.0	ns
					03	1.5	7.5	ns
Setup time high or low A_N, B_N to CPA, CPB	t_{S1}			9,10,11	All	2.5		ns
Hold time high or low A_N, B_N to CPA, CPB	t_{H1}			9,10,11	01	2.0		ns
					02,03	1.5		ns
Setup time high or low CEA, CEB to CPA, CPB	t_{S2}			9,10,11	All	3.0		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified 1/	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Hold time high or low CEA, CEB to CPA, CPB	t_{H2}	C_L = 50 pF, R_L = 500Ω, see figure 4	9,10,11	All	2.0		ns
Pulse width high or low CPA or CPB	t_{PW}		9,10,11	All	3.0		ns

1/ All tests shall be performed using worst-case test conditions, unless otherwise specified.

2/ Parameter is not tested for devices 01, 02, and 03, but limit shall be guaranteed.

3/ Only one output shorted at a time for 1 second maximum duration.

4/ Per TTL driven input (V_{IN} = 3.4 V); all other inputs at V_{CC} or GND.

5/ This parameter is not directly testable, but is derived for use in total power supply (I_C) calculations.

6/ $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
$I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD}(f_{CP}/2 + f_i N_i)$
I_{CC} = Quiescent current
ΔI_{CC} = Power supply current for a TTL high input (V_{IN} = 3.4 V)
D_H = Duty cycle for TTL inputs high
N_T = Number of TTL inputs a D_H
I_{CCD} = Dynamic current caused by an input transition pair (HLH or LHL)
f_{CP} = clock frequency for devices
f_i = Input frequency
N_i = Number of inputs at f_i
All currents are in mA and all frequencies are in MHz.

7/ Minimum limits are guaranteed but not tested.

Device types		01,02,03	
Case outlines		K,L	
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	B_7	13	$\overline{CEB}$
2	B_6	14	CPB
3	B_5	15	$\overline{OEA}$
4	B_4	16	A_0
5	B_3	17	A_1
6	B_2	18	A_2
7	B_1	19	A_3
8	B_0	20	A_4
9	$\overline{OEB}$	21	A_5
10	CPA	22	A_6
11	$\overline{CEA}$	23	A_7
12	GND	24	V_{CC}

Device types		01,02,03	
Case outlines		3	
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	NC	15	NC
2	B_7	16	$\overline{CEB}$
3	B_6	17	CPB
4	B_5	18	$\overline{OEA}$
5	B_4	19	A_0
6	B_3	20	A_1
7	B_2	21	A_2
8	NC	22	NC
9	B_1	23	A_3
10	B_0	24	A_4
11	$\overline{OEB}$	25	A_5
12	CPA	26	A_6
13	$\overline{CEA}$	27	A_7
14	GND	28	V_{CC}

FIGURE 1. Terminal connections.

Register functional table (Applies to A or B register)				
Inputs			Internal Q	Function
D	CP	$\overline{CE}$		
X	X	H	NC	Hold data
L	↑	L	L	Load data
H	↑	L	H	Load data

Output control			
$\overline{OE}$	Internal Q	Y-Outputs	Function
H	X	Z	Disable outputs
L	L	L	Enable outputs
L	H	H	Enable outputs

NOTES:
H = HIGH voltage level
L = LOW voltage level
X = Don't care
NC = No change
↑ = LOW-to-HIGH transition

FIGURE 2. Truth tables.

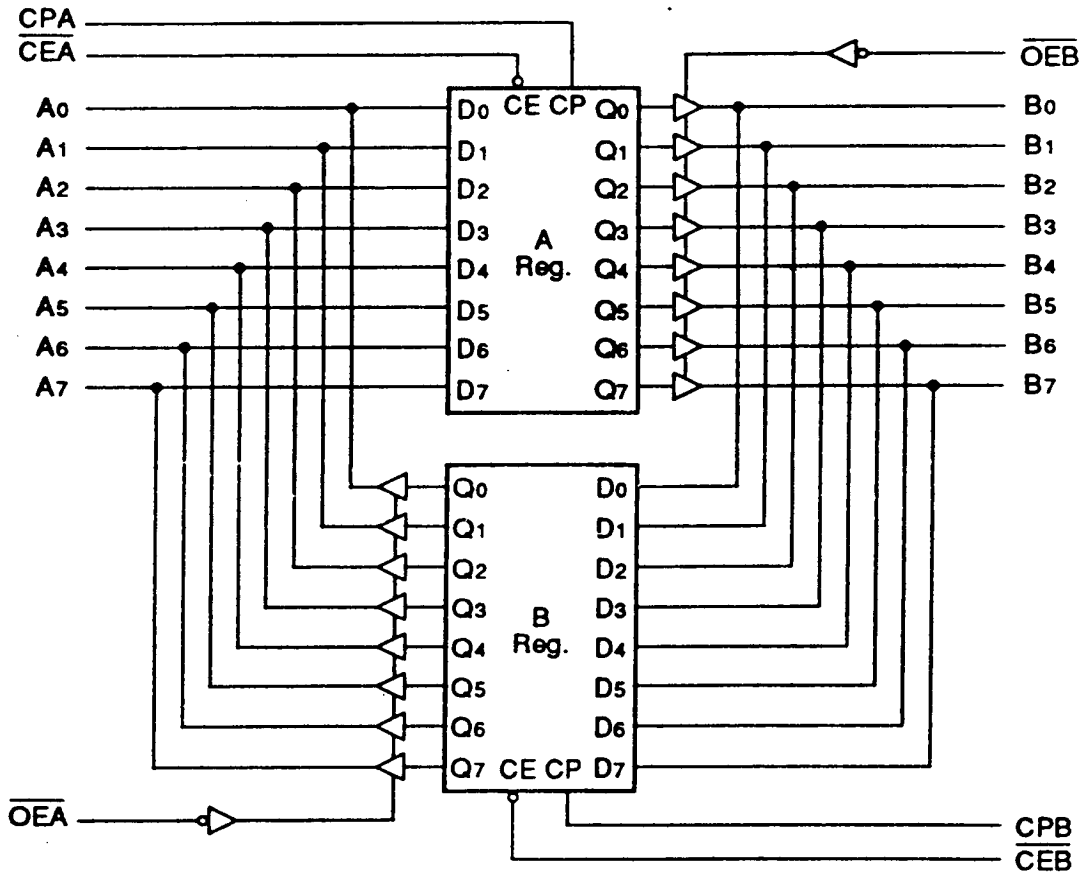
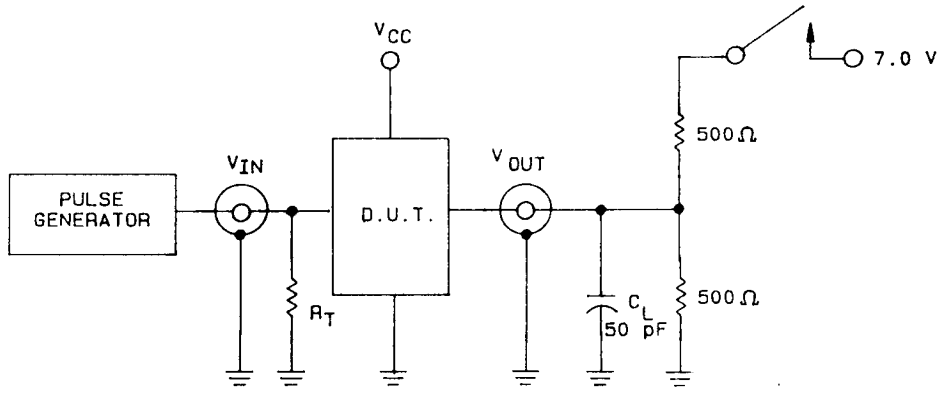


FIGURE 3. Logic diagram.

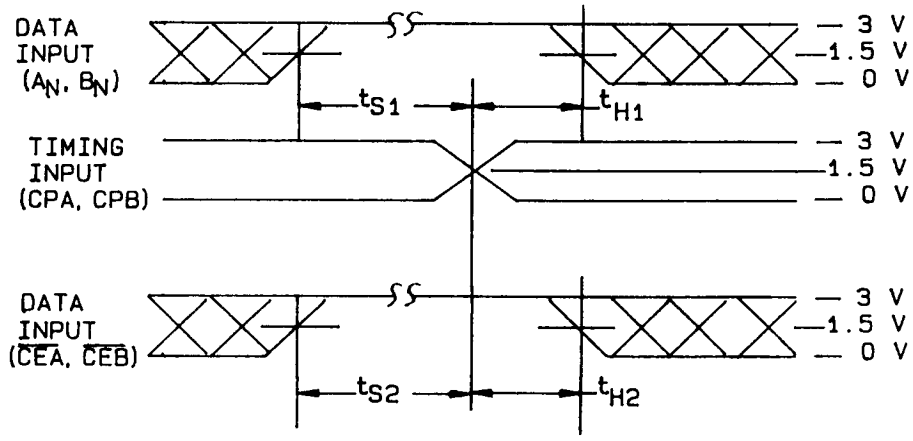
STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-90901
		REVISION LEVEL	SHEET 10



Switch position	
Test	Switch
t_{LZ} t_{ZL} All other outputs	Closed Closed Open

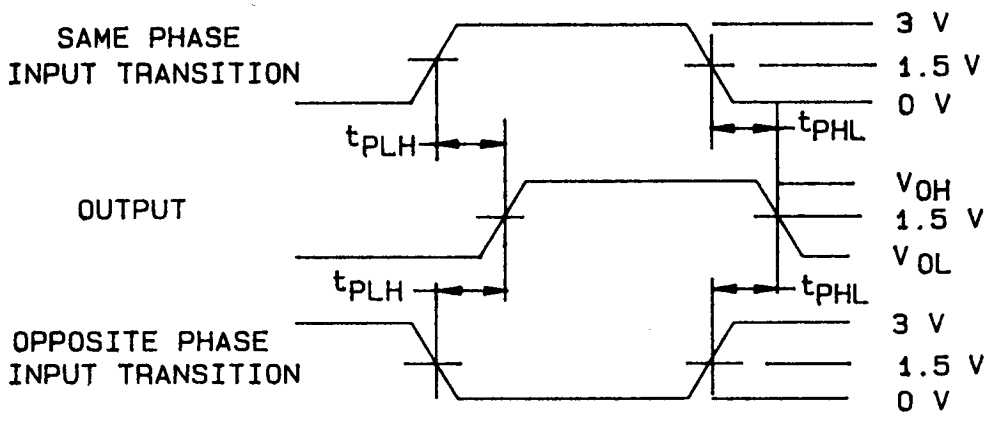
Definitions:
C_L = Load capacitance (includes jig and probe capacitance)
R_T = Termination should be equal to Z_{OUT} of pulse generators

Test circuit for three-state outputs

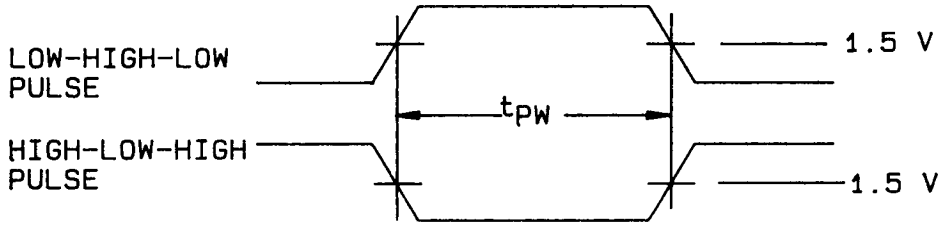


Setup and hold times

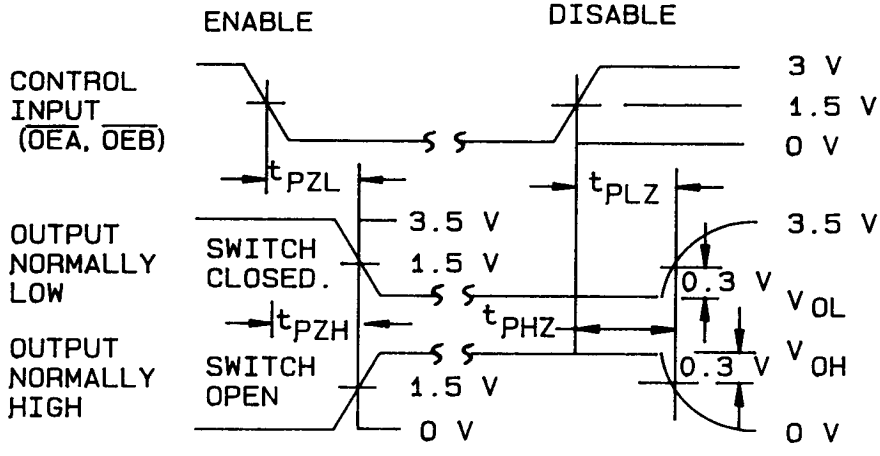
FIGURE 4. Switching waveforms and test circuit.



Propagation delay



Pulse width



NOTES:
1. Diagram shown for input control enable low and input control disable high.
2. Pulse generator for all pulses: rate ≤ 1.0 MHz; Z_o ≤ 50Ω; t_r ≤ 2.5 ns; t_f ≤ 2.5 ns.

Enable and disable times

FIGURE 4. Switching waveforms and test circuit - Continued.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device class M, sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein). For device classes B and S, sampling and inspection procedures shall be in accordance with MIL-M-38510 and method 5005 of MIL-STD-883, except as modified herein. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-I-38535 and the device manufacturer's QM plan.

4.2 Screening. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. For device classes B and S, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to qualification and quality conformance inspection. For device classes Q and V, screening shall be in accordance with MIL-I-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes M, B, and S.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. For device class M, the test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. For device classes B and S, the test circuit shall be submitted to the qualifying activity. For device classes M, B, and S, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-I-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in appendix B of MIL-I-38535.

4.3 Qualification inspection.

4.3.1 Qualification inspection for device classes B and S. Qualification inspection for device classes B and S shall be in accordance with MIL-M-38510. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5).

4.3.2 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-I-38535. Inspections to be performed shall be those specified in MIL-I-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5).

4.4 Conformance inspection. Quality conformance inspection for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein) and as specified herein. Quality conformance inspection for device classes B and S shall be in accordance with MIL-M-38510 and as specified herein. Inspections to be performed for device classes M, B, and S shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5). Technology conformance inspection for classes Q and V shall be in accordance with MIL-I-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-I-38535 permits alternate in-line control testing.

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)			Subgroups (in accordance with MIL-I-38535, table III)	
	Device class M	Device class B	Device class S	Device class Q	Device class V
Interim electrical parameters (see 4.2)		1,7,9	1,7,9	1,7,9	1,7,9
Final electrical parameters (see 4.2)	1/ 1,2,3 7,8,9,10,11	1/ 1,2,3 7,8,9,10,11	2/ 1,2,3 7,8,9,10,11	1/ 1,2,3 7,8,9,10,11	2/ 1,2,3 7,8,9,10,11
Group A test requirements (see 4.4)	1,2,3,4,7, 8,9,10,11	1,2,3,4,7, 8,9,10,11	1,2,3,4,7, 8,9,10,11	1,2,3,4,7, 8,9,10,11	1,2,3,4,7, 8,9,10,11
Group B end-point electrical parameters (see 4.4)			1,7,9		
Group C end-point electrical parameters (see 4.4)	1,2,3	1,2,3		1,2,3	1,2,3
Group D end-point electrical parameters (see 4.4)	1,2,3	1,2,3	1,2,3	1,2,3	1,2,3
Group E end-point electrical parameters (see 4.4)	1,7,9	1,7,9	1,7,9	1,7,9	1,7,9

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1 and 7.

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the functionality of the device. For device classes B and S, subgroups 7 and 8 tests shall be sufficient to verify the truth table as approved by the qualifying activity. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).

c. Subgroup 4 (C_{IN} and $C_{I/O}$ measurements) shall be measured only for the initial test and after process or design changes which may affect capacitance. A minimum sample size of 5 devices with zero rejects shall be required.

4.4.2 Group B inspection. The group B inspection end-point electrical parameters shall be as specified in table II herein. For device class S steady-state life tests, the test circuit shall be submitted to the qualifying activity.

4.4.3 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.3.1 Additional criteria for device classes M and B. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A, B, C, or D. For device class M, the test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. For device class B, the test circuit shall be submitted to the qualifying activity. For device classes M and B, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.3.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-I-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

4.4.4 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.5 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes B, S, Q, and V shall be M, D, R, and H and for device class M shall be M and D.

a. End-point electrical parameters shall be as specified in table II herein.

b. For device classes M, B, and S, the devices shall be subjected to radiation hardness assured tests as specified in MIL-M-38510 for the RHA level being tested. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-I-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510 for device classes M, B, and S and MIL-I-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device classes B and Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).

6.3 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and which SMD's are applicable to that system. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DESC-EC, telephone (513) 296-6074.

6.4 Comments. Comments on this drawing should be directed to DESC-EC, Dayton, Ohio 45444, or telephone (513) 296-5377.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-M-38510, MIL-STD-1331, and table III herein.

TABLE III. Pin descriptions.

Name	I/O	Description
A_{0-7}	I/O	Eight bidirectional lines carrying the A register inputs or B register outputs.
B_{0-7}	I/O	Eight bidirectional lines carrying the B register inputs or A register outputs.
CPA	I	Clock for the A register. When $\overline{CEA}$ is low, data is entered into the A register on the low-to-high transition of the CPA signal.
$\overline{CEA}$	I	Clock Enable for the A register. When $\overline{CEA}$ is low, data is entered into the A register on the low-to-high transition of the CPA signal. When CEA is high, the A register holds its contents, regardless of CPA signal transitions.
$\overline{OEB}$	I	Output Enable for the A register. When $\overline{OEB}$ is low, the A register outputs are enabled onto the B_{0-7} lines. When OEB is high, the B_{0-7} outputs are in the high impedance state.
CPB	I	Clock for the B register. When $\overline{CEB}$ is low, data is entered into the B register on the low-to-high transition of the CPB signal.
$\overline{CEB}$	I	Clock Enable for the B register. When $\overline{CEB}$ is low data is entered into the B register on the low-to-high transition of the CPB signal. When CEB is high, the B register holds its contents, regardless of CPB signal transitions.
$\overline{OEA}$	I	Output Enable for the B register. When $\overline{OEA}$ is low, the B register outputs are enabled onto the A_{0-7} lines. When OEA is high, the A_{0-7} outputs are in the high impedance state.

6.6 One part - one part number system. The one part - one part number system described below has been developed to allow for transitions between identical generic devices covered by the four major microcircuit requirements documents (MIL-M-38510, MIL-H-38534, MIL-I-38535, and 1.2.1 of MIL-STD-883) without the necessity for the generation of unique PIN's. The four military requirements documents represent different class levels, and previously when a device manufacturer upgraded military product from one class level to another, the benefits of the upgraded product were unavailable to the Original Equipment Manufacturer (OEM), that was contractually locked into the original unique PIN. By establishing a one part number system covering all four documents, the OEM can acquire to the highest class level available for a given generic device to meet system needs without modifying the original contract parts selection criteria.

Military documentation format	Example PIN under new system	Manufacturing source listing	Document
New MIL-M-38510 Military Detail Specifications (in the SMD format)	5962-XXXXXZZ(B or S)YY	QPL-38510 (Part 1 or 2)	MIL-BUL-103
New MIL-H-38534 Standardized Military Drawings	5962-XXXXXZZ(H or K)YY	QML-38534	MIL-BUL-103
New MIL-I-38535 Standardized Military Drawings	5962-XXXXXZZ(Q or V)YY	QML-38535	MIL-BUL-103
New 1.2.1 of MIL-STD-883 Standardized Military Drawings	5962-XXXXXZZ(M)YY	MIL-BUL-103	MIL-BUL-103

6.7 Sources of supply.

6.7.1 Sources of supply for device classes B and S. Sources of supply for device classes B and S are listed in QPL-38510.

6.7.2 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DESC-EC and have agreed to this drawing.

6.7.3 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-EC.