REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add device types 03 and 04. Add package J. Editorial changes throughout.	95-11-08	M. A. Frye

REV																			
SHEET																			
REV	A	A	A	A	A	A	A												
SHEET	15	16	17	18	19	20	21												

REV STATUS OF SHEETS	REV	A	A	A	A	A	A	A	A	A	A	A	A	A
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

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DRAWING APPROVAL DATE
93-03-11

REVISION LEVEL
A

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, LINEAR, 12-BIT A/D CONVERTER, MICROPROCESSOR COMPATIBLE WITH SAMPLE AND HOLD, MONOLITHIC SILICON

SIZE	CAGE CODE	5962-91578
A	67268	

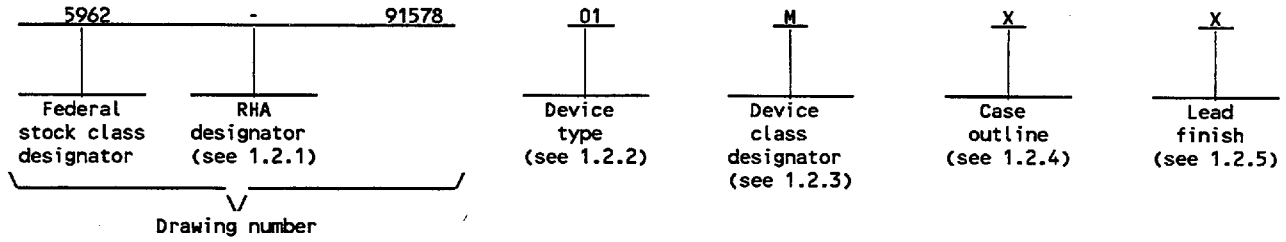
SHEET 1 OF 21

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing forms a part of a one part - one part number documentation system (see 6.6 herein). Two product assurance classes consisting of military high reliability (device classes Q and M) and space application (device class V), and a choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). Device class M microcircuits represent non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices". When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:



1.2.1 RHA designator. Device class M RHA marked devices shall meet the MIL-I-38535 appendix A specified RHA levels and shall be marked with the appropriate RHA designator. Device classes Q and V RHA marked devices shall meet the MIL-I-38535 specified RHA levels and shall be marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	ADC1241	Self-calibrating 12-bit plus sign µP-compatible A/D converter with sample-and-hold
02	ADC12441	Dynamically-tested self-calibrating 12-bit plus sign µP-compatible A/D converter with sample-and-hold
03	ADC1251	Self-calibrating 12-bit plus sign µP-compatible A/D converter with sample-and-hold
04	ADC12451	Dynamically-tested self-calibrating 12-bit plus sign µP-compatible A/D converter with sample-and-hold

1.2.3 Device class designator. The device class designator shall be a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883
Q or V	Certification and qualification to MIL-I-38535

1.2.4 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	GDIP1-T28 or CDIP2-T28	28	Dual-in-line
J	GDIP1-T24 or CDIP2-T24	24	Dual-in-line

1.2.5 Lead finish. The lead finish shall be as specified in MIL-STD-883 (see 3.1 herein) for class M or MIL-I-38535 for classes Q and V. Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference.

1.3 Absolute maximum ratings. 1/

Positive supply voltage (DV_{CC} and AV_{CC})	6.5 V dc
Negative supply voltage (V-)	-6.5 V dc
Voltage range at logic control inputs	-0.3 V dc to (V_{CC} + 0.3 V dc)
Voltage range at analog input (V_{IN}) 2/	(V- -0.3 V dc) to (V_{CC} + 0.3 V dc)
AV_{CC} - DV_{CC} 3/	0.3 V dc
Input current at any pin (I_{IN}) 4/	±5 mA
Package input current 4/	±20 mA
Storage temperature range	-65°C to +150°C
Lead temperature (soldering, 10 seconds)	+300°C
Power dissipation at +25°C 5/	875 mW
Junction temperature (T_J)	+125°C
Thermal resistance, junction-to-ambient (θ_{JA})	80°C/W

1.4 Recommended operating conditions.

Positive supply voltage range (V_{CC} and AV_{CC})	4.5 V dc to 5.5 V dc
Negative supply voltage range (V-)	-4.5 V dc to -5.5 V dc
Reference voltage range (V_{REF}) 3/	3.5 V dc to AV_{CC} +50 mV dc
Ambient operating temperature range (T_A)	-55°C to +125°C
Voltage at analog input (V_{IN}) 2/	(V-) - 0.05 V dc to V_{CC} + 0.05 V dc

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, bulletin, and handbook. Unless otherwise specified, the following specification, standards, bulletin, and handbook of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-I-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Microcircuit Case Outlines.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ Two on-chip diodes are tied to the analog input. Errors in the A/D conversion can occur if these diodes are forward biased more than 50 mV.
3/ A diode exists between AV_{CC} and DV_{CC}. To guarantee accuracy, it is required that the AV_{CC} and DV_{CC} be connected together to a power supply with separate bypass filters at each V_{CC} pin.
4/ When the input voltage (V_{IN}) at any pin exceeds the power supply rails (V_{IN} < V- or V_{IN} > (AV_{CC} or DV_{CC})) the current at that pin should be limited to 5 mA. The 20 mA maximum package input current rating allows the voltage at any four pins, with an input current limit of 5 mA, to simultaneously exceed the power supply voltages.
5/ The maximum power dissipation must be derated at elevated temperatures and is dictated by T_J MAX, θ_{JA} and T_A. The maximum allowable power dissipation at any temperature is P_D MAX = (T_J MAX - T_A)/θ_{JA} or the number given in the absolute maximum ratings, whichever is lower. The typical thermal resistance when board mounted is 47°C/W.

HANDBOOK

MILITARY

MIL-HDBK-780 - Standardized Military Drawings.

(Copies of the specification, standards, bulletin, and handbook required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device class M shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein. The individual item requirements for device classes Q and V shall be in accordance with MIL-I-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not effect the form, fit, or function as described herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-STD-883 (see 3.1 herein) for device class M and MIL-I-38535 for device classes Q and V and herein.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth tables. The truth tables shall be as specified on figure 2.

3.2.4 Logic diagrams. The block or logic diagrams shall be as specified on figure 3.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. Marking for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein). In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103. Marking for device classes Q and V shall be in accordance with MIL-I-38535.

3.5.1 Certification/compliance mark. The compliance mark for device class M shall be a "C" as required in MIL-STD-883 (see 3.1 herein). The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-I-38535.

3.6 Certificate of compliance. For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.7.2 herein). For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.7.1 herein). The certificate of compliance submitted to DESC-EC prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device class M, the requirements of MIL-STD-883 (see 3.1 herein), or for device classes Q and V, the requirements of MIL-I-38535 and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required for device class M in MIL-STD-883 (see 3.1 herein) or for device classes Q and V in MIL-I-38535 shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DESC-EC of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-973.

3.9 Verification and review for device class M. For device class M, DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 81 (see MIL-I-38535, appendix A).

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ $V_{CC} = DV_{CC} = AV_{CC} = +5$ V $V^- = -5$ V, $V_{REF} = +5$ V unless otherwise specified	Group A subgroups	Device type	Limits 2/ Min	Limits 2/ Max	Unit
Positive integral linearity error	$+E_{IL}$	After auto-cal 3/, 4/	1, 2, 3	01,03		±1	LSB
Negative integral linearity error	$-E_{IL}$	After auto-cal 3/, 4/	1, 2, 3			±1	
Differential linearity	E_{DL}	After auto-cal 3/, 4/	1, 2, 3	01,03	12		Bits
Zero error	E_Z	After auto-zero or auto-cal 4/, 5/	1, 2, 3	01,02		±1	LSB
		$\overline{AZ} = 0$, $f_{CLK} = 1.75$ Mhz	1, 2, 3	03		±1	
		After auto-cal only	1			±2	
			2, 3			±2.5	
		After auto-cal only	1	04		±2	
			2, 3			±3	
Positive full-scale error	$+E_{FS}$	After auto-cal 4/	1, 2, 3	01,02		±1	
		$\overline{AZ} = 0$, $f_{CLK} = 1.75$ Mhz	1, 2, 3	03		±1.5	
		After auto-cal only	1			±1.5	
			2, 3			±2.0	
			1	04		±1.5	
			2, 3			±2.5	
Negative full-scale error	$-E_{FS}$	After auto-cal only 4/	1	01,02		±1	
			2, 3			±2	
		$\overline{AZ} = 0$, $f_{CLK} = 1.75$ Mhz	1, 2, 3	03		±1.5	
		After auto-cal only	1			±1.5	
			2, 3			±2.0	
			1	04		±1.5	
			2, 3			±3.0	
Bipolar effective bits	BIP	$f_{IN} = 20$ kHz, $V_{IN} = \pm 4.85$ V 6/	1, 2, 3	02	12.4		Bits
		$f_{IN} = 20.67$ kHz, $V_{IN} = \pm 4.85$ V		04	11.9		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ $V_{CC} = DV_{CC} = AV_{CC} = +5$ V $V^- = -5$ V, $V_{REF} = +5$ V unless otherwise specified	Group A subgroups	Device type	Limits 2/ Min	Limits 2/ Max	Unit
Unipolar effective bits	UNI	f_{IN} = 20 kHz 6/ V_{IN} = +4.85 V p-p	1, 2, 3	02	11.6		Bits
		f_{IN} = 20.67 kHz, V_{IN} = ±4.85 V		04	11.1		
Bipolar signal-to-noise ratio	BSNR	f_{IN} = 20 kHz 6/ V_{IN} = ±4.85 V	1, 2, 3	02	76.5		dB
		f_{IN} = 20.67 kHz, V_{IN} = ±4.85 V		04	73.5		
Unipolar signal-to-noise ratio	USNR	f_{IN} = 20 kHz 6/ V_{IN} = +4.85 V p-p	1, 2, 3	02	71.5		
		f_{IN} = 20.67 kHz, V_{IN} = ±4.85 V		04	68.7		
Bipolar total harmonic distortion	BTHD	f_{IN} = 19.688 kHz 6/ V_{IN} = ±4.85 V p-p	1, 2, 3	02		-75.0	dB
		f_{IN} = 20.67 kHz, V_{IN} = ±4.85 V		04		-78.0	
Unipolar total harmonic distortion	UTHD	f_{IN} = 19.688 kHz 6/ V_{IN} = +4.85 V p-p	1, 2, 3	02		-75.0	
		f_{IN} = 20.67 kHz, V_{IN} = ±4.85 V		04		-73.1	
Bipolar two tone intermodulation distortion	BIMD	f_{IN1} = 19.375 kHz 6/ f_{IN2} = 20.625 kHz V_{IN} = ±4.85 V	1, 2, 3	02		-74.0	
Unipolar two tone intermodulation distortion	UIMD	f_{IN1} = 19.375 kHz 6/ f_{IN2} = 20.625 kHz V_{IN} = +4.85 V p-p	1, 2, 3	02		-73.0	
-3 dB bipolar pull power bandwidth	BFPBW	V_{IN} = ±4.85 V p-p 6/	1, 2, 3	02	20.0		KHz
				04	20.67		
-3 dB unipolar pull power bandwidth	UFPBW	V_{IN} = ±4.85 V p-p 6/	1, 2, 3	02	20.0		
				04	20.67		
Logical "1" input for all inputs except CLK IN	$V_{IN(1)}$	V_{CC} = 5.25 V	1, 2, 3	All	2.0		V
Logical "0" input for all inputs except CLK IN	$V_{IN(0)}$	V_{CC} = 4.75 V	1, 2, 3	All		0.8	V

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ $V_{CC} = DV_{CC} = AV_{CC} = +5$ V $V- = -5$ V, $V_{REF} = +5$ V unless otherwise specified	Group A subgroups	Device type	2/ Limits Min	Limits Max	Unit
Analog input voltage	V_{IN}		1, 2, 3	02 03,04	V- -0.05	V_{CC} +0.05	V
Logical "1" input current	$I_{IN(1)}$	V_{IN} = 5 V	1, 2, 3	All		1	µA
Logical "0" input current	$I_{IN(0)}$	V_{IN} = 0 V	1, 2, 3	All		-1	
CLK IN positive going threshold voltage	V_T+		1, 2, 3	All	2.7		V
CLK IN negative going threshold voltage	V_T-		1, 2, 3	All		2.3	
CLK IN hysteresis $[V_T+(min) - V_T-(max)]$	V_H		1, 2, 3	All	0.4		
Logical "1" output voltage	$V_{OUT(1)}$	V_{CC} = 4.75 V, I_{OUT} = -360 µA	1, 2, 3	All	2.4		
		V_{CC} = 4.75 V, I_{OUT} = -10 µA			4.5		
Logical "0" output voltage	$V_{OUT(0)}$	V_{CC} = 4.75 V, I_{OUT} = 1.6 mA	1, 2, 3	All		0.4	
Three-state output leakage current	I_{OUT}	V_{OUT} = 0 V	1, 2, 3	All		-3	µA
		V_{OUT} = 5 V				3	
Output source current	I_{SOURCE}	V_{OUT} = 0 V	1, 2, 3	All	-6		mA
Output sink current	I_{SINK}	V_{OUT} = 5 V	1, 2, 3	All	8		
DV_{CC} supply current	DI_{CC}	CS = "1"	1, 2, 3	01,02		2	
				03,04		2.5	
AV_{CC} supply current	AI_{CC}	CS = "1"	1, 2, 3	01,02		6	mA
				03,04		10	
V- supply current	I-	CS = "1"	1, 2, 3	01,02		6	
				03,04		10	
Functional tests	FT	See 4.4.1c	7, 8	All			

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ $V_{CC} = DV_{CC} = AV_{CC} = +5$ V $V- = -5$ V, $V_{REF} = +5$ V unless otherwise specified	Group A subgroups	Device type	Limits 2/ Min	Limits 2/ Max	Unit
Clock frequency	f_{CLK}	$t_r = t_f = 20$ ns	9, 10, 11	01,02		2	MHz
				03,04		3.5	
Clock duty cycle	t_{CLK}	$t_r = t_f = 20$ ns	9, 10, 11	All	40	60	%
Conversion time	t_c	$f_{CLK} = 2.0$ MHz, See figure 5	9, 10, 11	01,02		13.8	µs
Conversion time using $\overline{WR}$ to start a conversion	t_c	$f_{CLK} = 2.0$ Mhz, $t_r = t_f = 20$ ns	9, 10, 11	03,04		13.75	
		$f_{CLK} = 3.5$ Mhz, $\overline{AZ} = 1$, $t_r = t_f = 20$ ns				7.95	
		$f_{CLK} = 1.75$ Mhz, $\overline{AZ} = 0$, $t_r = t_f = 20$ ns				15.65	
Conversion time using S/H to start a conversion	t_c	$f_{CLK} = 2.0$ MHz, $\overline{AZ} = 1$, $t_r = t_f = 20$ ns	9, 10, 11	03,04		17.25	
		$f_{CLK} = 3.5$ Mhz, $\overline{AZ} = 1$, $t_r = t_f = 20$ ns				9.95	
Acquisition time	t_{AC}	$f_{CLK} = 2.0$ Mhz, $R_S = 50\Omega$, See figure 5	9, 10, 11	01,02		3.8	µs
		$R_S = 50\Omega$, $t_r = t_f = 20$ ns 7/		03,04	3.5		
Internal acquisition time when using WR control only	t_{AC}	$f_{CLK} = 2.0$ MHz, $t_r = t_f = 20$ ns	9, 10, 11	03,04		3.5	µs
Auto zero time	t_Z	$f_{CLK} = 2.0$ MHz, See figure 5	9, 10, 11	01,02		13	µs
Auto zero time + acquisition time	t_{ZA}	$f_{CLK} = 2.0$ MHz, $t_r = t_f = 20$ ns	9, 10, 11	03,04		16.75	
		$f_{CLK} = 1.75$ Mhz, $t_r = t_f = 20$ ns				19.05	
Delay from hold command to falling edgeof EOC	$t_{D(EOC)L}$	$t_r = t_f = 20$ ns using WR control	9, 10, 11	03,04		350	ns
		$t_r = t_f = 20$ ns using S/H control				150	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ $V_{CC} = DV_{CC} = AV_{CC} = +5$ V, $V^- = -5$ V, $V_{REF} = +5$ V unless otherwise specified	Group A subgroups	Device type	Limits 2/ Min	Limits 2/ Max	Unit
Calibration time	$t_{\overline{CAL}}$	f_{CLK} = 2.0 MHz, $t_r = t_f$ = 20 ns, See figure 5	9, 10, 11	01,02		706	µs
				03,04		700	
		f_{CLK} = 3.5 Mhz, $t_r = t_f$ = 20 ns				400	
Calibration pulse width	$t_{W(CAL)L}$	$t_r = t_f$ = 20 ns 8/ See figure 5	9, 10, 11	All	200		ns
Minimum $\overline{WR}$ pulse width	$t_{W(\overline{WR})L}$	$t_r = t_f$ = 20 ns See figure 5	9, 10, 11	All	200		
Maximum access time (delay from falling edge of RD to output data valid)	t_{ACC}	C_L = 100 pF, See figure 5	9	01,02		85	ns
			10, 11	01		140	
		$t_r = t_f$ = 20 ns	9, 10, 11	03,04		95	
Three-state control (delay from rising edge of RD to Hi-Z state)	t_{OH}, t_{1H}	R_L = 1 kΩ, C_L = 100 pF, See figures 4 and 5	9	01,02		90	
			10, 11	01		120	
		$t_r = t_f$ = 20 ns	9, 10, 11	03,04		70	
Maximum $\overline{RD}$ or $\overline{WR}$ to reset of $\overline{INT}$	$t_{PD(\overline{INT})}$	See figure 5 $t_r = t_f$ = 20 ns	9, 10, 11	All		175	
Delay between successive RD pulses	t_{RR}	$t_r = t_f$ = 20 ns	9, 10, 11	03,04	60		

1/ Device types 01 and 02, f_{CLK} = 2 Mhz. Device types 03 and 04, f_{CLK} = 3.5 Mhz.

2/ The limiting terms "min" (minimum) and "max" (maximum) shall be considered to apply to magnitudes only. Negative current shall be defined as conventional current flow out of a device terminal.

3/ Positive linearity error is defined as the deviation of the analog value, expressed in LSBs, from the straight line that passes through positive full scale and zero. For negative linearity error the straight line passes through negative full scale and zero.

4/ This device's self-calibration technique ensures linearity, full scale, and offset errors as specified, but noise inherent in the self-calibration process will result in a repeatability uncertainty of ±0.20 LSB.

5/ If T_A changes then auto-zero or auto-cal cycle will have to be re-started.

6/ Valid after an auto-cal cycle has been completed.

7/ When using the $\overline{WR}$ control to start a conversion if the clock is asynchronous to the rising edge of $\overline{WR}$ an uncertainty of one clock period will exist in the end of the interval t_A, therefore making t_A end a minimum 6 clock periods or a maximum 7 clock periods after the rising edge of WR. If the falling edge of the clock is synchronous to the rising edge of WR then t_A will end exactly 6.5 clock periods after the rising edge of WR. This does not occur when S/H control used.

8/ The $\overline{CAL}$ line must be high before any other conversion is started.

Device types	01 and 02	03 and 04
Case outline	X	J
Terminal number	Terminal symbol	
1	V_{IN}	V_{IN}
2	V_{REF}	V_{REF}
3	AGND	AGND
4	AV_{CC}	AV_{CC}
5	V-	V-
6	$\overline{AZ}$	$\overline{AZ}$
7	$\overline{WR}$	$\overline{WR}$
8	CLKIN	CLKIN
9	$\overline{CAL}$	$\overline{CAL}$
10	$\overline{CS}$	$\overline{CS}$
11	$\overline{RD}$	$\overline{S/H}$
12	EOC	DGND
13	$\overline{INT}$	DB0/DB8
14	DGND	DB1/DB9
15	DB0(LSB)	DB2/DB10
16	DB1	DB3/DB11
17	DB2	DB4/DB12
18	DB3	DB5/DB12
19	DB4	DB6/DB12
20	DB5	DB7/DB12
21	DB6	$\overline{INT}$
22	DB7	EOC
23	DB8	$\overline{RD}$
24	DB9	DV_{CC}
25	DB10	- - -
26	DB11(MSB)	- - -
27	DB12(SIGN BIT)	- - -
28	DV_{CC}	- - -

FIGURE 1. Terminal connections.

Device types 01 and 02

Digital control inputs					A/D function
$\overline{CS}$	$\overline{WR}$	$\overline{RD}$	$\overline{CAL}$	$\overline{AZ}$	
⊔	⊔	1	1	1	Start conversion without auto-zero
⊔	1	⊔	1	1	Read conversion result without auto-zero
⊔	⊔	1	1	0	Start conversion with auto-zero
⊔	1	⊔	1	0	Read conversion result with auto-zero
1	X	X	⊔	X	Start calibration cycle
0	X	1	0	X	Test mode (DB2, DB3, DB5 and DB6 becomeactive)

Device types 03 and 04

Digital control inputs						A/D function
$\overline{CS}$	$\overline{WR}$	$\overline{S/H}$	$\overline{RD}$	$\overline{CAL}$	$\overline{AZ}$	
⊔	⊔	1	1	1	1	Start conversion without auto-zero
⊔	1	⊔	1	1	1	Start conversion synchronous with rising edge of S/H without auto-zero
⊔	1	1	⊔	1	1	Read conversion result without auto-zero
⊔	⊔	1	1	1	0	Start conversion with auto-zero
⊔	1	1	⊔	1	0	Read conversion result with auto-zero
1	X	1	X	⊔	X	Start calibration cycle
0	X	1	1	0	X	Test mode (DB2, DB3, DB5 and DB6 becomeactive)

FIGURE 2. Truth tables.

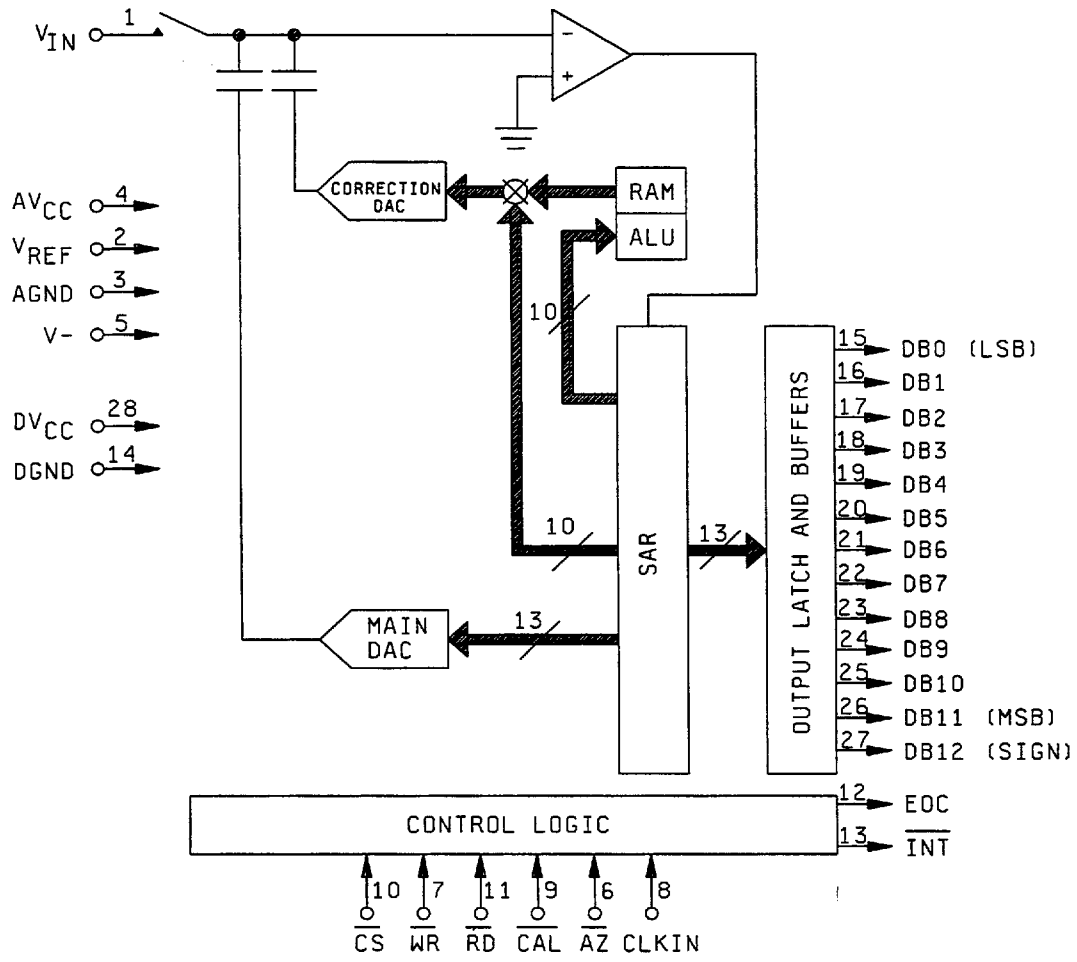


FIGURE 3. Logic diagram. (device types 01and 02)

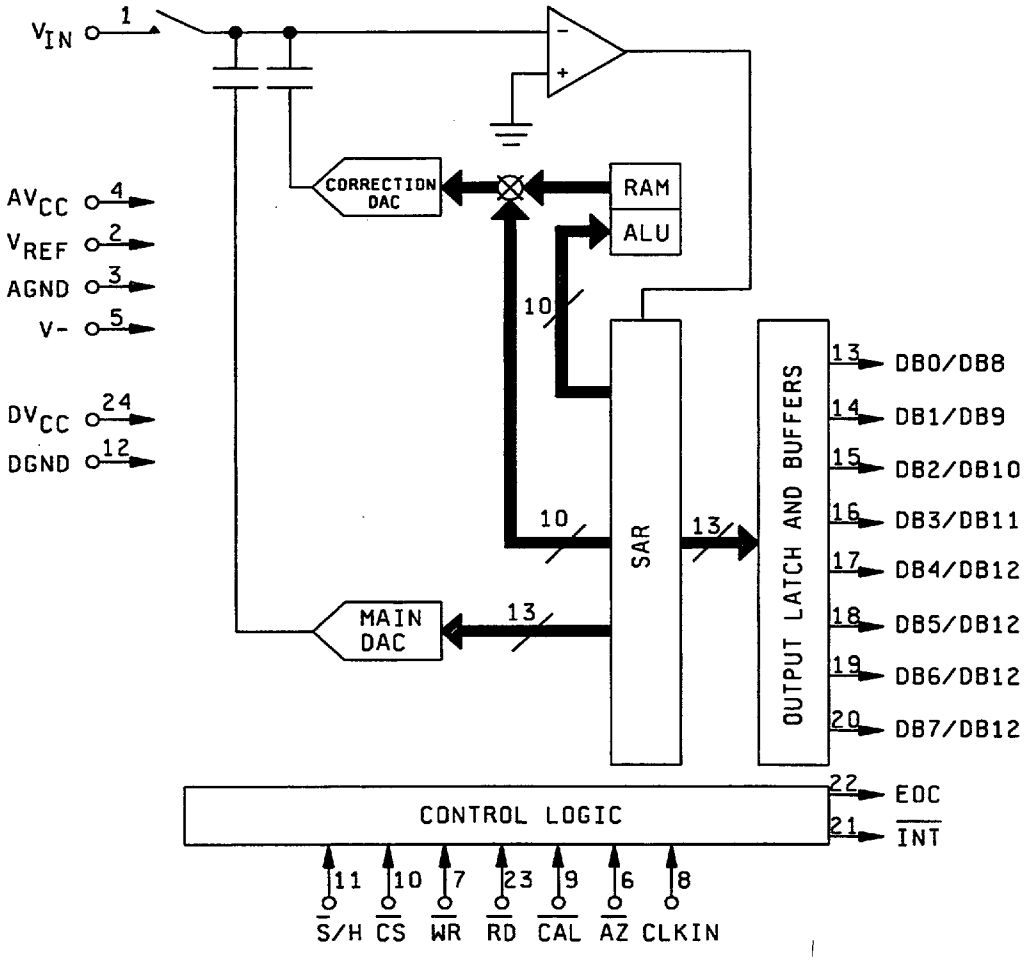


FIGURE 3. Logic diagram - continued. (device types 03nd 04)

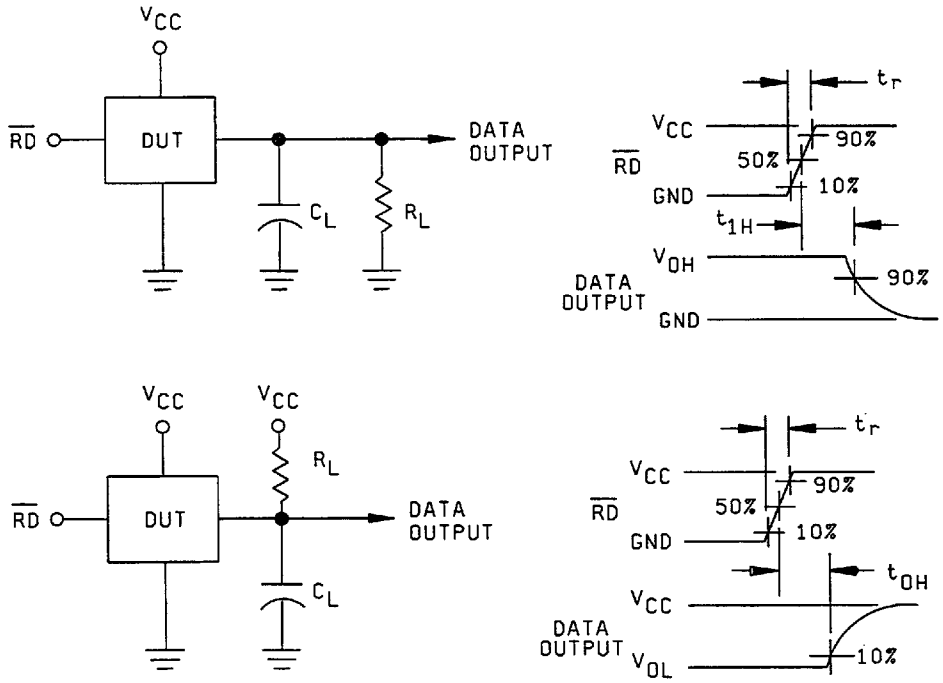


FIGURE 4. Three state test circuit and waveforms.

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		REVISION LEVEL A	SHEET 14

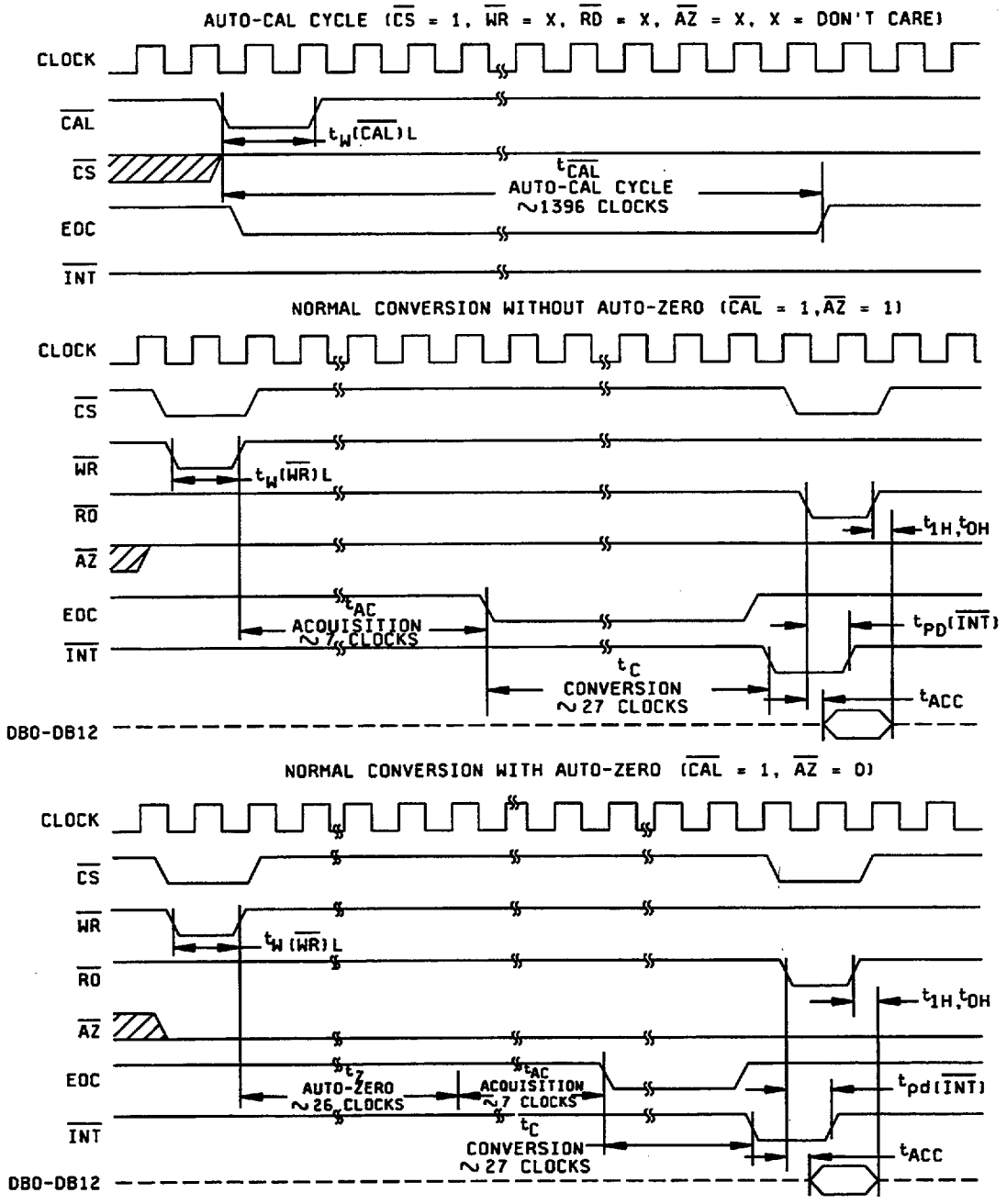

FIGURE 5. Timing diagram. (device types 01 and 02)

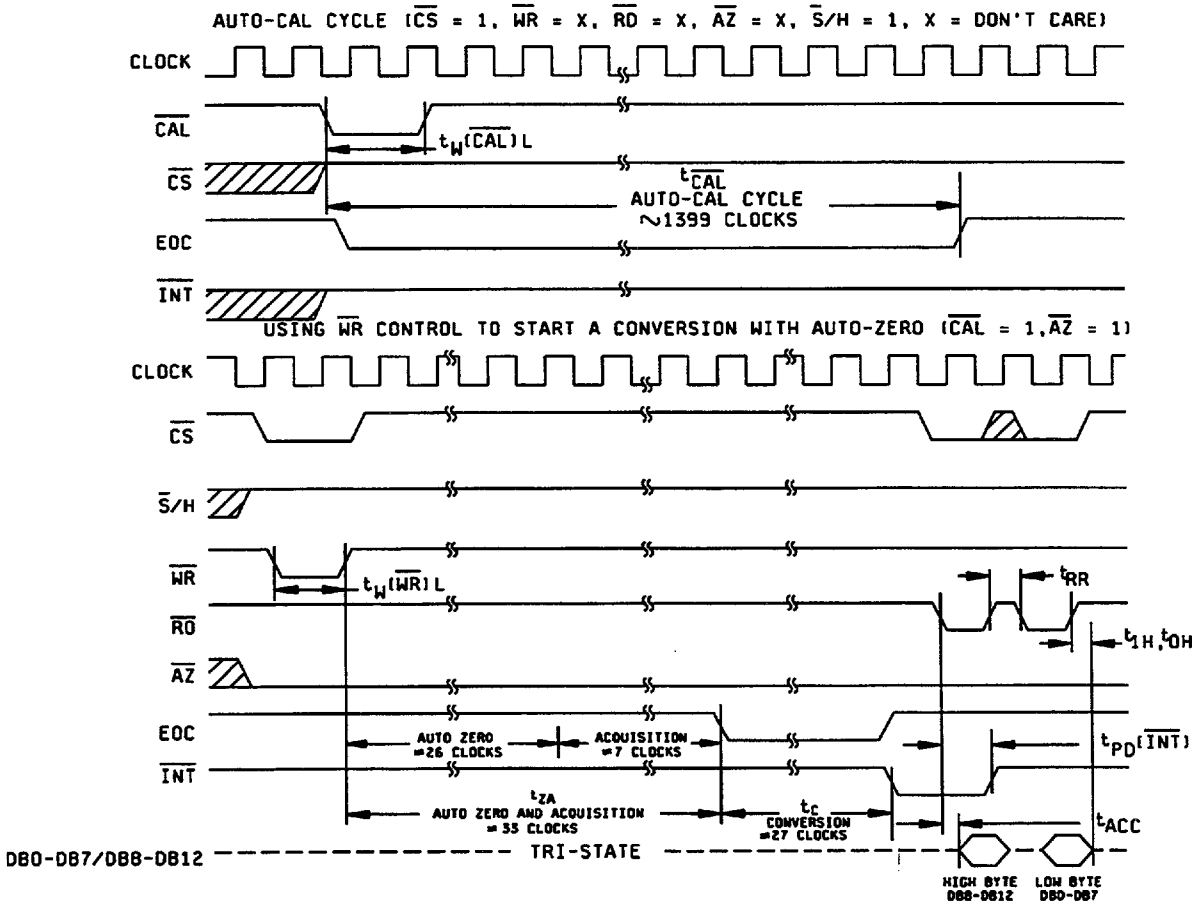

FIGURE 5. Timing diagram - continued. (device types 03 and 04)

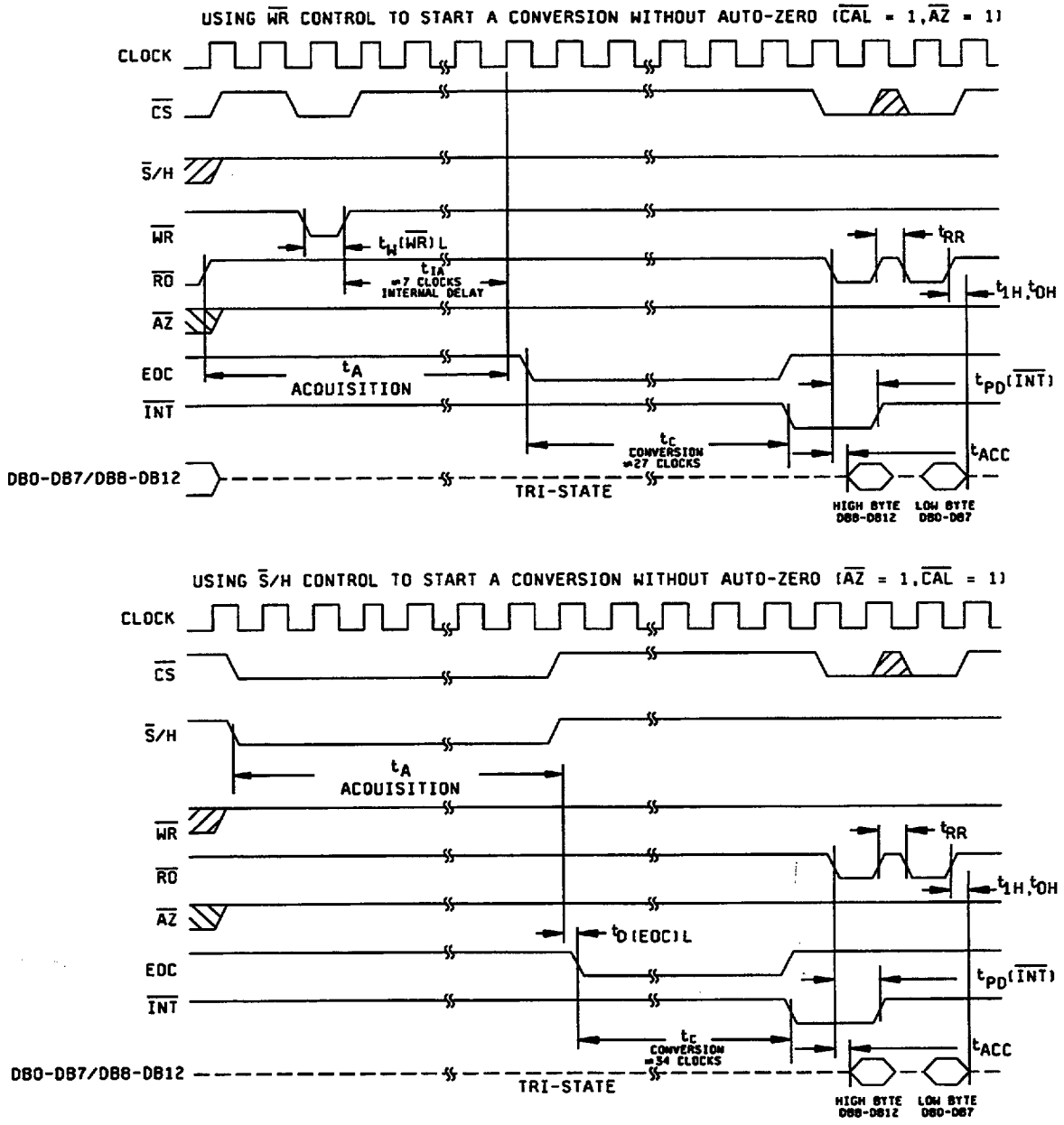

FIGURE 5. Timing diagram - continued. (device types 03 and 04)

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device class M, sampling and inspection procedures shall be in accordance with MIL-STD-883 (see 3.1 herein). For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-I-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not effect the form, fit, or function as described herein.

4.2 Screening. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. For device classes Q and V, screening shall be in accordance with MIL-I-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes M, B, and S.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-I-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in appendix B of MIL-I-38535.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-I-38535. Inspections to be performed shall be those specified in MIL-I-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Quality conformance inspection for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein) and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4). Technology conformance inspection for classes Q and V shall be in accordance with MIL-I-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-I-38535 permits alternate in-line control testing.

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 4, 5, and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. For device class M, Q, and V, subgroups 7 and 8 tests shall be sufficient to verify the truth table.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, TM 5005, table I)	Subgroups (in accordance with MIL-I-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1	1	1
Final electrical parameters (see 4.2)	1/ 1, 2, 3, 7, 8, 9 10, 11	1/ 1, 2, 3, 7, 8, 9, 10, 11	1/ 1, 2, 3, 7, 8, 9, 10, 11
Group A test requirements (see 4.4)	1, 2, 3, 9, 9, 10, 11	1, 2, 3, 9 ,10, 11	1, 2, 3, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3	1, 2, 3, 9, 10, 11
Group D end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3	1, 2, 3

1/ PDA applies to subgroup 1.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB, in accordance with MIL-I-38535, and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes Q and V shall be M, D, L, R, F, G, and H and for device class M shall be M and D.

a. End-point electrical parameters shall be as specified in table II herein.

b. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-I-38535, appendix A, for the RHA level being tested. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-I-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-STD-883 (see 3.1 herein) for device class M and MIL-I-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and which SMD's are applicable to that system. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DESC-EC, telephone (513) 296-6047.

6.4 Comments. Comments on this drawing should be directed to DESC-EC, Dayton, Ohio 45444-5270, or telephone (513) 296-5377.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-M-38510 and MIL-STD-1331.

DV_{CC}, AV_{CC}	The digital and analog positive power supply pins. The digital and analog power supply voltage range of the ADC1241 is +4.5 V to +5.5 V. To guarantee accuracy, it is required that the AV_{CC} and DV_{CC} be connected together to the same power supply with separate bypass filters (10 µF tantalum in parallel with a 0.1 µF ceramic) at each V_{CC} pin.
V-	The analog negative supply voltage pin. V- has a range of -4.5 V to -5.5 V and needs a bypass filter of 10 µF tantalum in parallel with a 0.1 µF ceramic
DGND, AGND	The digital and analog ground pins. AGND and DGND must be connected together externally to guarantee accuracy.
V_{REF}	The reference input voltage pin. To maintain accuracy the voltage at this pin should not exceed AV_{CC} or DV_{CC} by more than 50 mV or go below 3.5 V dc.
V_{IN}	The analog input voltage pin. To guarantee accuracy the voltage at this pin should not exceed V_{CC} by more than 50 mV or go below V- by more than 50 mV.
$\overline{CS}$	The chip select control input. This input is active low and enables the $\overline{WR}$ and RD functions.
$\overline{RD}$	The read control input. With both $\overline{CS}$ and $\overline{RD}$ low the Three-state output buffers are enabled and the INT output is reset high.
$\overline{WR}$	The write control input. The conversion is started on the rising edge of the WR pulse when CS is low.
CLK	The external clock input pin. The clock frequency range is 500 kHz to 4 MHz.
$\overline{CAL}$	The auto-calibration control input. When $\overline{CAL}$ is low the ADC1241 is reset and a calibrationcycle is initiated. During the calibration cycle the values of the comparator offset voltage and the mismatch errors in the capacitor reference ladder are determined and stored in RAM. These values are used to correct the errors during a normal cycle of A/D conversion.
EOC	The end-of-conversion control output. This output is low during a conversion or a calibration cycle.

$\overline{AZ}$ — The auto-zero control input. With the $\overline{AZ}$ pin held low during a conversion, the ADC1241 goes into an auto-zero cycle before the actual A/D conversion is started. This auto-zero cycle corrects for the comparator offset voltage. The total conversion time (t_c) is increased by 26 clock periods when auto-zero is used.

$\overline{INT}$ — The interrupt control output. This output goes low when a conversion has been completed and indicates that the conversion result is available in the output latches. Reading the result or starting a conversion or calibration cycle will reset this output high.

$\overline{S/H}$ — The sample and hold control input. This control input can also be used to start a conversion. With CS low the falling edge of S/H starts the analog input aquisition window. The rising edge of S/H ends the aquisition window and starts a conversion.

6.6 One part - one part number system. The one part - one part number system described below has been developed to allow for transitions between identical generic devices covered by the three major microcircuit requirements documents (MIL-H-38534, MIL-I-38535, and 1.2.1 of MIL-STD-883) without the necessity for the generation of unique PIN's. The three military requirements documents represent different class levels, and previously when a device manufacturer upgraded military product from one class level to another, the benefits of the upgraded product were unavailable to the Original Equipment Manufacturer (OEM), that was contractually locked into the original unique PIN. By establishing a one part number system covering all three documents, the OEM can acquire to the highest class level available for a given generic device to meet system needs without modifying the original contract parts selection criteria.

Military documentation format	Example PIN under new system	Manufacturing source listing	Document listing
New MIL-H-38534 Standard Microcircuit Drawings	5962-XXXXXZZ(H or K)YY	QML-38534	MIL-BUL-103
New MIL-I-38535 Standard Microcircuit Drawings	5962-XXXXXZZ(Q or V)YY	QML-38535	MIL-BUL-103
New 1.2.1 of MIL-STD-883 Standard Microcircuit Drawings	5962-XXXXXZZ(M)YY	MIL-BUL-103	MIL-BUL-103

6.7 Sources of supply.

6.7.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DESC-EC and have agreed to this drawing.

6.7.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-EC.