REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Changes in accordance with NOR 5962-R144-93.	93-06-15	M.L. Poelking
B	Add device 03. Editorial changes throughout.	94-04-18	M.L. Poelking
C	Add device 04. Editorial changes throughout.	95-03-25	M.L. Poelking

REV																				
SHEET																				
REV	C	C	C	C	C	C	C	C	C	C	C	C	C	C						
SHEET	35	36	37	38	39	40	41	42	43	44	45	46	47	48						
REV	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C	C
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34

REV STATUS OF SHEETS	REV	C	C	C	C	C	C	C	C	C	C	C	C	C	C
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

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DRAWING APPROVAL DATE 92-04-27

REVISION LEVEL C

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, DIGITAL, CMOS, GRAPHICS SYSTEM PROCESSOR, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	67268	5962-91623
SHEET 1	OF 48	

DESC FORM 193
JUL 91

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

5962-E136-95

9004708 0004995 0T2

1. SCOPE

1.1 Scope. This drawing forms a part of a one part - one part number documentation system (see 6.6 herein). Two product assurance classes consisting of military high reliability (device classes Q and M) and space application (device class V), and a choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). Device class M microcircuits represent non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices". When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:

```
   5962              -              91623       01         M          X          X
    |                |                          |          |          |          |
 Federal            RHA                       Device     Device      Case       Lead
 stock class     designator                    type      class      outline    finish
 designator      (see 1.2.1)               (see 1.2.2) designator (see 1.2.4) (see 1.2.5)
                                                       (see 1.2.3)
 \__________________\/__________________/
              Drawing number
```

1.2.1 RHA designator. Device class M RHA marked devices shall meet the MIL-I-38535 appendix A specified RHA levels and shall be marked with the appropriate RHA designator. Device classes Q and V RHA marked devices shall meet the MIL-I-38535 specified RHA levels and shall be marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	34020-28	Graphics system processor
02	34020-30	Graphics system processor
03	34020A-32	Graphics system processor
04	34020A-40	Graphics system processor

1.2.3 Device class designator. The device class designator shall be a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883
Q or V	Certification and qualification to MIL-I-38535

1.2.4 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	CMGA7-P145	145	Pin grid array
Y	CQCC1-F132	132	Leaded chip carrier

1.2.5 Lead finish. The lead finish shall be as specified in MIL-STD-883 (see 3.1 herein) for class M or MIL-I-38535 for classes Q and V. Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference.

1.3 Absolute maximum ratings. 1/

Maximum supply voltage (V_{CC}) 2/ - - - - - - - - - - - - -	7.0 V dc
Input voltage range - - - - - - - - - - - - - - - - - - -	-0.3 V dc to 7.0 V dc
Off-state output voltage range - - - - - - - - - - - - - -	-2.0 V dc to 7.0 V dc
Operating temperature range - - - - - - - - - - - - - - -	-55°C to +125°C
Storage temperature range - - - - - - - - - - - - - - - -	-65°C to +150°C
Lead temperature (soldering, 10 seconds) - - - - - - - - -	+260°C
Thermal resistance, junction-to-case (θ_{JC}) - - - - - - -	See MIL-M-38510, appendix C
Junction temperature (T_J) - - - - - - - - - - - - - - - -	+175°C
Power dissipation -	1.375 W

1.4 Recommended operating conditions.

Supply voltage range (V_{CC}):	
Device 01, 03 -	4.5 V dc to 5.5 V dc
Device 02, 04 -	4.75 V dc to 5.25 V dc
Supply voltage (V_{SS}) 3/ - - - - - - - - - - - - - - - - -	0 V dc
Maximum high level output current (I_{OH}) - - - - - - - - -	400 µA
Maximum low level output current (I_{OL}) - - - - - - - - - -	2 mA
Case operating temperature range (T_C) - - - - - - - - - -	-55°C to +125°C

1.5 Digital logic testing for device classes Q and V.

Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012) . . . . . . XX percent 2/

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ All voltage values are with respect to V_{SS}.
3/ Take care to provide a minimum inductance path between the V_{SS} pins and system ground in order to miminize noise on V_{SS}.
4/ Values will be added when they become available.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, bulletin, and handbook. Unless otherwise specified, the following specification, standards, bulletin, and handbook of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-I-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Microcircuit Case Outlines.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

HANDBOOK

MILITARY

MIL-HDBK-780 - Standardized Military Drawings.

(Copies of the specification, standards, bulletin, and handbook required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device class M shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein. The individual item requirements for device classes Q and V shall be in accordance with MIL-I-38535, the device manufacturer's Quality Management (QM) plan, and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-STD-883 (see 3.1 herein) for device class M and MIL-I-38535 for device classes Q and V and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Block diagram. The block diagram shall be as specified on figure 2.

3.2.5 Radiation exposure circuit. The radiation exposure circuit shall be specified when available.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. Marking for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein). In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103. Marking for device classes Q and V shall be in accordance with MIL-I-38535.

3.5.1 Certification/compliance mark. The compliance mark for device class M shall be a "C" as required in MIL-STD-883 (see 3.1 herein). The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-I-38535.

3.6 Certificate of compliance. For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.7.2 herein). For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.7.1 herein). The certificate of compliance submitted to DESC-EC prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device class M, the requirements of MIL-STD-883 (see 3.1 herein), or for device classes Q and V, the requirements of MIL-I-38535 and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required for device class M in MIL-STD-883 (see 3.1 herein) or for device classes Q and V in MIL-I-38535 shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DESC-EC of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-973.

3.9 Verification and review for device class M. For device class M, DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 105 (see MIL-I-38535, appendix A).

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device class M, sampling and inspection procedures shall be in accordance with MIL-STD-883 (see 3.1 herein). For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-I-38535 and the device manufacturer's QM plan.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \leq T_C \leq +125°C$ V_{CC} = min to max 1/ 2/ unless otherwise specified		Group A subgroups	Device type	Limits Min	Limits Max	Unit
High level input voltage	V_{IH}		BUSFLT, LRDY, VCLK, PGMD, SIZE16	1,2,3	All	2.3	V_{CC}+0.3	V
			CLKIN only			3.0	V_{CC}+0.3	
		HWRITE, HREAD, HA5-HA31, HCS, HBS0-HBS3	CSYNC, HSYNC, VSYNC			2.3	V_{CC}+0.3	
			All other input pins			2.0	V_{CC}+0.3	
Low level input voltage	V_{IL}		HCS	1,2,3	All	-0.3	0.7	
			All other input pins	1,2,3	All	-0.3	0.8	
High level output voltage	V_{OH}	V_{CC} = min, I_{OH} = 400 µA		1,2,3	All	2.6		
Low level output voltage	V_{OL}	V_{CC} = max, I_{OL} = 2 mA	DDIN, HINT, HRDY, R0, R1, EMU3	1,2,3	All		0.8	
			HSYNC, VSYNC				0.8	
			All other output pins				0.6	
Output leakage current (high impedance)	I_O	V_{CC} = max	V_O = 2.8 V	1,2,3	All		20	µA
			V_O = 0.6 V				-20	
Input current	I_I	V_I = V_{SS} to V_{CC}	3/ All input pins except EMU0-EMU2, HREAD, HWRITE	1,2,3	All		±20	
Supply current	I_{CC}	V_{CC} = max, freq = max		1,2,3	01-03		265	mA
					04		280	
Input capacitance	C_I	See 4.4.1.b		4	ALL		18	pF
Output capacitance	C_O	See 4.4.1.b		4	ALL		25	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ V_{CC} = min to max 1/ 2/ unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
Functional test		See 4.4.1.c		7,8	ALL			ns
Period, CLKIN (t_Q)	t_{c1}	See figure 3 (1)		9,10,11	01	35	50	
					02	33	50	
					03	31.25	50	
					04	25	50	
Pulse duration, CLKIN high	t_{w1}	See figure 3 (2)		9,10,11	01-03	10		
					04	8		
Pulse duration, CLKIN low	t_{w2}	See figure 3 (3)		9,10,11	01-03	10		
					04	8		
Transition time, CLKIN	t_{t1}	See figure 3 (4) 4/		9,10,11	All	2	5	
Hold time, $\overline{RESET}$ low after CLKIN high	t_{h1}	See figure 3 (5) 5/		9,10,11	01-03	15		
					04	12		
Setup time, $\overline{RESET}$ high to CLKIN going high	t_{su1}	See figure 3 (6) 5/		9,10,11	01-03	10		
					04	6		
Pulse width, $\overline{RESET}$ low	t_{w3}	See figure 3 (7) 6/	Initial reset during powerup	9,10,11	All	$160t_Q-40$		
			Reset during active operation			$16t_Q-40$		
Setup time, $\overline{HCS}$ low to RESET high to configure self-bootstrap mode	t_{su2}	See figure 3 (8)		9,10,11	All	$8t_Q+55$		
Delay time, $\overline{HCS}$ going high to RESET high to configure self-bootstrap mode	t_{d1}	See figure 3 (9) 7/		9,10,11	All		$4t_Q-50$	
Pulse width, $\overline{HCS}$ low to configure GSP in self-bootstrap mode	t_{w4}	See figure 3 (10)		9,10,11	All	$4t_Q+55$		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \leq T_C \leq +125°C$ V_{CC} = min to max 1/ 2/ unless otherwise specified	Group A subgroups	Device type	Limits Min	Limits Max	Unit
Period of local clocks LCLK1, LCLK2	t_{c2}	See figure 3 (11) 8/	9,10,11	All	$4t_{c1}$+s		ns
Pulse width, local clock high	t_{w5}	See figure 3 (12)	9,10,11	01-03	$2t_Q$-15		
				04	$2t_Q$-13.5		
Pulse width, LCLK1 high (measured at 1.5 V)	t_{w6}	See figure 3 (12a)	9,10,11	01-03	$2t_Q$-10		
				04	$2t_Q$-7		
Pulse width, local clock low	t_{w7}	See figure 3 (13)	9,10,11	01-03	$2t_Q$-15+S		
				04	$2t_Q$-13.5+S		
Pulse width, LCLK1 low (measured at 1.5 V)	t_{w8}	See figure 3 (13a)	9,10,11	01-03	$2t_Q$-10+S		
				04	$2t_Q$-7+S		
Transition time, LCLK1 or LCLK2	t_{t2}	See figure 3 (14)	9,10,11	01-03		15	
				04		13.5	
Hold time, LCLK2 low after LCLK1 high	t_{h2}	See figure 3 (15)	9,10,11	01-03	t_Q-15		
				04	t_Q-13.5		
Hold time, LCLK1 high after LCLK2 high	t_{h3}	See figure 3 (16)	9,10,11	01-03	t_Q-15		
				04	t_Q-13.5		
Hold time, LCLK2 high after LCLK1 low	t_{h4}	See figure 3 (17)	9,10,11	01-03	t_Q-15		
				04	t_Q-13.5		
Hold time, LCLK1 low after LCLK2 low	t_{h5}	See figure 3 (18)	9,10,11	01-03	t_Q-15+S		
				04	t_Q-13.5+S		
Hold time, LCLK2 high after LCLK1 high	t_{h6}	See figure 3 (19)	9,10,11	01-03	$3t_Q$-15		
				04	$3t_Q$-13.5		
Hold time, LCLK1 low after LCLK2 high	t_{h7}	See figure 3 (20)	9,10,11	01-03	$3t_Q$-15+S		
				04	$3t_Q$-13.5+S		
Hold time, LCLK2 low after LCLK1 low	t_{h8}	See figure 3 (21)	9,10,11	01-03	$3t_Q$-15+S		
				04	$3t_Q$-13.5+S		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \leq T_C \leq +125°C$ V_{CC} = min to max 1/ 2/ unless otherwise specified	Group A subgroups	Device type	Limits Min	Limits Max	Unit
Hold time, LCLK1 high after LCLK2 low	t_{h9}	See figure 3 (22)	9,10,11	01-03	$3t_Q-15+S$		ns
				04	$3t_Q-13.5+S$		
Hold time, LCLKx 9/ to output signal not valid	t_{h10}		9,10,11	All	t_Q-15		
Delay time, LCLKx start of transition to output signal valid 9/	t_{d2}	Fast: $\overline{RAS}$, $\overline{CAS}$, $\overline{ALTCH}$, $\overline{TR/QE}$, $\overline{DDOUT}$, DDIN, EMU3, $\overline{HOE}$, $\overline{RO}$, $\overline{R1}$, HDST, $\overline{WE}$	9,10,11	All		t_Q+15	
		Slow: LAD, RCA, SF				t_Q+22	
Hold time, output signal valid to output signal not valid 9/	t_{h11}	Fast: $\overline{RAS}$, $\overline{CAS}$, $\overline{ALTCH}$, $\overline{TR/QE}$, $\overline{DDOUT}$, DDIN, EMU3, $\overline{HOE}$, $\overline{RO}$, $\overline{R1}$, HDST, $\overline{WE}$	9,10,11	All	nt_Q-16		
		Slow: LAD, RCA, SF			nt_Q-22		
Delay time, output signal started transition to output signal valid 9/	t_{d3}	Fast: $\overline{RAS}$, $\overline{CAS}$, $\overline{ALTCH}$, $\overline{TR/QE}$, $\overline{DDOUT}$, DDIN, EMU3, $\overline{HOE}$, $\overline{RO}$, $\overline{R1}$, HDST, $\overline{WE}$	9,10,11	All		nt_Q+15	
		Slow: LAD, RCA, SF				nt_Q+22	
Transition time, output signal 9/	t_{t3}	Fast: $\overline{RAS}$, $\overline{CAS}$, $\overline{ALTCH}$, $\overline{TR/QE}$, $\overline{DDOUT}$, DDIN, EMU3, $\overline{HOE}$, $\overline{RO}$, $\overline{R1}$, HDST, $\overline{WE}$	9,10,11	All		15	
		Slow: LAD, RCA, SF				22	
Pulse width, output signal high 9/	t_{w9}	Fast: $\overline{RAS}$, $\overline{CAS}$, $\overline{ALTCH}$, $\overline{TR/QE}$, $\overline{DDOUT}$, DDIN, EMU3, $\overline{HOE}$, $\overline{RO}$, $\overline{R1}$, HDST, $\overline{WE}$	9,10,11	All	nt_Q-15		
		Slow: LAD, RCA, SF			nt_Q-22		
Pulse width, output signal low 9/	t_{w10}	Fast: $\overline{RAS}$, $\overline{CAS}$, $\overline{ALTCH}$, $\overline{TR/QE}$, $\overline{DDOUT}$, DDIN, EMU3, $\overline{HOE}$, $\overline{RO}$, $\overline{R1}$, HDST, $\overline{WE}$	9,10,11	All	nt_Q-15		
		Slow: LAD, RCA, SF			nt_Q-22		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions -55°C ≤ T_C ≤ +125°C V_{CC} = min to max 1/ 2/ unless otherwise specified	Group A subgroups	Device type	Limits Min	Limits Max	Unit
Setup time, address prior to HCS going low	t_{su3}	See figure 3 (23)	9,10,11	01-03	12		ns
				04	10		
Hold time, address after HCS low	t_{h12}	See figure 3 (24)	9,10,11	01-03	12		
				04	10		
Pulse width, HCS high	t_{w11}	See figure 3 (25)	9,10,11	01-03	28		
				04	25		
Pulse width, HREAD high	t_{w12}	See figure 3 (26)	9,10,11	01-03	28		
				04	25		
Pulse width, HWRITE high	t_{w13}	See figure 3 (27)	9,10,11	01-03	28		
				04	25		
Setup time, HREAD high to HWRITE going low	t_{su4}	See figure 3 (28)	9,10,11	01-03	28		
				04	25		
Setup time, HWRITE high to HREAD going low	t_{su5}	See figure 3 (29)	9,10,11	01-03	28		
				04	25		
Pulse width, HREAD low	t_{w14}	See figure 3 (30)	9,10,11	01-03	18		
				04	15		
Pulse width, HWRITE low	t_{w15}	See figure 3 (31)	9,10,11	01-03	18		
				04	15		
Setup time, HCS low to HWRITE going high	t_{su6}	See figure 3 (32)	9,10,11	01-03	18		
				04	15		
Setup time, later of HCS low or HREAD low to LCLK2 going low	t_{su7}	See figure 3 (33) 10/	9,10,11	01-03	30		
				04	25		
Setup time, later of HWRITE high or HCS high to LCLK2 going low	t_{su8}	See figure 3 (34) 10/	9,10,11	01-03	30		
				04	25		
Hold time, HREAD high after LCLK2 going low	t_{h13}	See figure 3 (35) 11/	9,10,11	All	0		
Hold time, HWRITE low after LCLK2 going low	t_{h14}	See figure 3 (36) 11/	9,10,11	All	0		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \leq T_C \leq +125°C$ V_{CC} = min to max 1/ 2/ unless otherwise specified	Group A subgroups	Device type	Limits Min	Limits Max	Unit
Setup time, $\overline{HREAD}$ high to LCLK2 going low, prefetch read mode	t_{su9}	See figure 3 (37) 10/ 12/	9,10,11	01-03	30		ns
				04	25		
Setup time, $\overline{HCS}$ low to $\overline{HREAD}$ going high	t_{su10}	See figure 3 (38)	9,10,11	01-03	18		
				04	15		
Delay time, from LCLK1 going high to HRDY high (end of read cycle)	t_{d4}	See figure 3 (39)	9,10,11	01-03		t_Q+20	
				04		t_Q+18	
Delay time, from earlier of $\overline{HREAD}$ or $\overline{HCS}$ high to HRDY low	t_{d5}	See figure 3 (40)	9,10,11	01-03		20	
				04		18	
Delay time, from LCLK2 going low to HDST low	t_{d6}	See figure 3 (41)	9,10,11	01-03		t_Q+15+S	
				04		t_Q+13.5 +S	
Delay time, from LCLK1 going low to HDST high	t_{d7}	See figure 3 (42)	9,10,11	01-03		t_Q+15	
				04		t_Q+13.5	
Setup time, HDST low to HRDY going high	t_{su12}	See figure 3 (43)	9,10,11	01-03	t_Q-15		
				04	t_Q-13.5		
Delay time, from HRDY going high to HDST high	t_{d8}	See figure 3 (44)	9,10,11	01-03		$2t_Q$+15	
				04		$2t_Q$+13.5	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ V_{CC} = min to max 1/ 2/ unless otherwise specified	Group A subgroups	Device type	Limits Min	Limits Max	Unit
Delay time, from later of HREAD or HCS low to HRDY high after prefetch	t_{d14}	See figure 3 (45)	9,10,11	01-03		25	ns
				04		20	
Delay time, from later of HCS or HWRITE low to HRDY high (device ready)	t_{d15}	See figure 3 (46)	9,10,11	01-03		25	
				04		20	
Delay time, from earlier of HCS or HWRITE high to HRDY low (end of write)	t_{d16}	See figure 3 (47)	9,10,11	01-03		25	
				04		20	
Delay time, from LCLK2 going low to HOE low	t_{d17}	See figure 3 (48)	9,10,11	01-03		t_Q+15+S	
				04		t_Q+13.5 +S	
Delay time, from LCLK1 going low to HOE high	t_{d18}	See figure 3 (49)	9,10,11	01-03		t_Q+15	
				04		t_Q+13.5	
Hold time $\overline{CAS}$, $\overline{TR}/\overline{QE}$, DDIN valid after HDST high	t_{h31}	See figure 3 (50)	9,10,11	03	-2		
				04	-2		
Delay time, from HRDY going high to HOE high	t_{d20}	See figure 3 (51)	9,10,11	01-03		2t_Q+15	
				04		2t_Q+13.5	
Access time, $\overline{CAMD}$ valid after address valid on LAD	t_{a1}	See figure 3 (52)	9,10,11	01-03		3t_Q-45	
				04		3t_Q-37	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \leq T_C \leq +125°C$ V_{CC} = min to max 1/ 2/ unless otherwise specified	Group A subgroups	Device type	Limits Min	Limits Max	Unit
Hold time, CAMD valid after address no longer valid on LAD	t_{h15}	See figure 3 (53)	9,10,11	All	0		ns
Access time, control valid (LRDY, PGMD, SIZE16, BUSFLT) after ALTCH low	t_{a2}	See figure 3 (54)	9,10,11	01-03		$3t_Q$-35+S	
				04		$3t_Q$-27+S	
Hold time, control (LRDY, PGMD, SIZE16, BUSFLT) valid after LCLK2 high	t_{h16}	See figure 3 (55)	9,10,11	All	0		
Setup time, LRDY, PGMD, BUSFLT, SIZE16 valid before LCLK2 going high	t_{su15}	See figure 3 (56)	9,10,11	01-03	20		
				04	15		
Delay time, $\overline{\text{ALTCH}}$ low after LCLK2 going high	t_{d21}	See figure 3 (57)	9,10,11	01-03		t_Q+15	
				04		t_Q+13.5	
Delay time, $\overline{\text{ALTCH}}$ high after LCLK1 going low	t_{d22}	See figure 3 (58)	9,10,11	01-03		t_Q+15	
				04		t_Q+13.5	
Delay time, LAD0-LAD31 address valid after LCLK1 going high	t_{d23}	See figure 3 (59)	9,10,11	01-03		t_Q+22	
				04		t_Q+20	
Hold time, LAD0-LAD31 address valid after LCLK2 low	t_{h17}	See figure 3 (60)	9,10,11	01-03	t_Q-15+S		
				04	t_Q-12+S		
Delay time, LAD0-LAD31 driven after earlier of DDIN going low or CAS going high or TR/QE going high	t_{d24}	See figure 3 (61) 4/	9,10,11	01-03	t_Q-5+S		
				04	t_Q-5+S		
Hold time, LAD0-LAD31 read data valid after earlier of DDIN low or RAS, CAS, or TR/QE high	t_{h18}	See figure 3 (62)	9,10,11	All	3.5		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \leq T_C \leq +125°C$ V_{CC} = min to max 1/ 2/ unless otherwise specified	Group A subgroups	Device type	Limits Min	Limits Max	Unit
Delay time, LAD0-LAD31 data valid after LCLK2 going low (write)	t_{d25}	See figure 3 (63)	9,10,11	01-03		t_Q+22+S	ns
				04		t_Q+22+S	
Hold time, LAD0-LAD31 data valid after LCLK2 low (write)	t_{h19}	See figure 3 (64)	9,10,11	01-03	t_Q-15		
				04	t_Q-13.5		
Delay time, RCA0-RCA12 row address valid after LCLK1 going high	t_{d26}	See figure 3 (65)	9,10,11	All		t_Q+22	
Delay time, LAD0-LAD31 column address valid after LCLK2 going low	t_{d27}	See figure 3 (66)	9,10,11	01-03		t_Q+22+S	
				04		t_Q+20+S	
Hold time, RCA0-RCA12 address valid after LCLK2 low	t_{h20}	See figure 3 (67)	9,10,11	01-03	t_Q-15		
				04	t_Q-13.5		
Delay time, DDIN high after LCLK1 going high	t_{d28}	See figure 3 (68)	9,10,11	01-03		t_Q+15	
				04		t_Q+13.5	
Delay time, DDIN low after LCLK1 going low	t_{d29}	See figure 3 (69)	9,10,11	01-03		t_Q+15	
				04		t_Q+13.5	
Delay time, $\overline{DDOUT}$ low after LCLK1 going high	t_{d30}	See figure 3 (70)	9,10,11	01-03		t_Q+15	
				04		t_Q+13.5	
Delay time, $\overline{DDOUT}$ high after LCLK1 going low	t_{d31}	See figure 3 (71)	9,10,11	01-03		t_Q+15	
				04		t_Q+13.5	
Delay time, $\overline{DDOUT}$ low after LCLK2 going low	t_{d32}	See figure 3 (72)	9,10,11	01-03		t_Q+15+S	
				04		t_Q+13.5 +S	
Setup time, LAD0-LAD31 data valid before $\overline{ALTCH}$ going low	t_{su16}	See figure 3 (73)	9,10,11	01-03	t_Q-16		
				04	t_Q-13.5		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ V_{CC} = min to max 1/ 2/ unless otherwise specified	Group A subgroups	Device type	Limits Min	Limits Max	Unit
Enable time, data valid after DDIN high	t_{en1}	See figure 3 (74) 13/	9,10,11	01-03		$2t_Q$-20	ns
				04		$2t_Q$-17	
Disable time, data high-impedance after DDIN low	t_{dis1}	See figure 3 (75) 13/ 4/	9,10,11	01-03		t_Q-12+S	
				04		t_Q-10+S	
Delay time, $\overline{RAS}$ low after LCLK1 going low	t_{d33}	See figure 3 (76)	9,10,11	01-03		t_Q+12+S	
				04		t_Q+10+S	
Delay time, $\overline{RAS}$ high after LCLK1 going low	t_{d34}	See figure 3 (77)	9,10,11	01-03		t_Q+12	
				04		t_Q+10	
Delay time, $\overline{CAS}$ low after LCLK1 going high	t_{d35}	See figure 3 (78)	9,10,11	01-03		t_Q+12	
				04		t_Q+10	
Delay time, $\overline{CAS}$ high after LCLK1 going low	t_{d36}	See figure 3 (79)	9,10,11	01-03		t_Q+12	
				04		t_Q+10	
Delay time, $\overline{WE}$ low after LCLK2 going low	t_{d37}	See figure 3 (80)	9,10,11	01-03		t_Q+15+S	
				04		t_Q+13.5 +S	
Delay time, $\overline{WE}$ high after LCLK1 going low	t_{d38}	See figure 3 (81)	9,10,11	All		t_Q+15	
Delay time, $\overline{TR/QE}$ low after LCLK2 going low	t_{d39}	See figure 3 (82)	9,10,11	01-03		t_Q+15+S	
				04		t_Q+13.5 +S	
Delay time, $\overline{TR/QE}$ high after LCLK1 going low	t_{d40}	See figure 3 (83)	9,10,11	01-03		t_Q+15	
				04		t_Q+13.5	
Delay time, SF valid after LCLK1 going high	t_{d41}	See figure 3 (84)	9,10,11	01-03		t_Q+22	
				04		t_Q+20	
Delay time, SF valid after LCLK2 going low	t_{d42}	See figure 3 (85)	9,10,11	01-03		t_Q+22+S	
				04		t_Q+20+S	
Delay time, SF high-impedance after LCLK2 going low	t_{d43}	See figure 3 (86) 4/	9,10,11	01-03		t_Q+22	
				04		t_Q+20	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \leq T_C \leq +125°C$ V_{CC} = min to max 1/ 2/ unless otherwise specified	Group A subgroups	Device type	Limits Min	Limits Max	Unit
Setup time, row address valid before RAS going low	t_{su17}	See figure 3 (87) 14/	9,10,11	01-03	$2t_Q$-22		ns
				04	$2t_Q$-20		
Hold time, row address valid after RAS low	t_{h22}	See figure 3 (88) 14/	9,10,11	01-03	t_Q-5+S		
				04	t_Q-5+S		
Setup time, column address valid before CAS going low	t_{su18}	See figure 3 (89)	9,10,11	01-03	t_Q-22		
				04	t_Q-20		
Hold time, column address valid after CAS high	t_{h23}	See figure 3 (90)	9,10,11	01-03	t_Q-15		
				04	t_Q-13.5		
Setup time, write data valid before CAS going low	t_{su19}	See figure 3 (91)	9,10,11	01-03	t_Q-22		
				04	t_Q-20		
Hold time, write data valid after CAS high	t_{h24}	See figure 3 (92)	9,10,11	01-03	t_Q-15		
				04	t_Q-13.5		
Access time, data-in valid after RAS low (assuming maximum transition time	t_{a3}	See figure 3 (93)	9,10,11	01-03		$4t_Q$-8+S	
				04		$4t_Q$-8+S	
Access time, data-in valid after CAS going low	t_{a4}	See figure 3 (94)	9,10,11	All		$2t_Q$-8	
Access time, data-in valid after column address valid	t_{a5}	See figure 3 (95)	9,10,11	01-03		$3t_Q$-20	
				04		$3t_Q$-12	
Setup time, write low before CAS going low (on write cycles)	t_{su20}	See figure 3 (97)	9,10,11	01-03	t_Q-15		
				04	t_Q-13.5		
Pulse width, RAS high	t_{w16}	See figure 3 (98)	9,10,11	01-03	$4t_Q$-12 +S		
				04	$4t_Q$-10 +S		
Pulse width, RAS low	t_{w17}	See figure 3 (99) 15/	9,10,11	01-03	$4nt_Q$-12 +S'		
				04	$4nt_Q$-4 +S'		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \leq T_C \leq +125°C$ V_{CC} = min to max 1/ 2/ unless otherwise specified	Group A subgroups	Device type	Limits Min	Limits Max	Unit
Pulse width, $\overline{\text{CAS}}$ high	t_{w18}	See figure 3 (100)	9,10,11	01-03	$2t_Q$-12		ns
				04	$2t_Q$-10		
Pulse width, $\overline{\text{CAS}}$ low	t_{w19}	See figure 3 (101)	9,10,11	01-03	$2t_Q$-12		
				04	$2t_Q$-8		
Delay time, $\overline{\text{RAS}}$ low to $\overline{\text{CAS}}$ going high	t_{d44}	See figure 3 (102)	9,10,11	01-03	$4t_Q$-12 +S		
				04	$4t_Q$-4+S		
Delay time, $\overline{\text{CAS}}$ low to $\overline{\text{RAS}}$ going low	t_{d45}	See figure 3 (103)	9,10,11	01-03	$2t_Q$-15		
				04	$2t_Q$-13.5		
Delay time, $\overline{\text{RAS}}$ high to $\overline{\text{CAS}}$ going low	t_{d46}	See figure 3 (104)	9,10,11	01-03	$2t_Q$-15 +S		
				04	$2t_Q$-13.5 +S		
Access time, $\overline{\text{GI}}$ valid after $\overline{\text{R0}}$ and $\overline{\text{R1}}$ valid	t_{a6}	See figure 3 (105) 16/	9,10,11	01-03		$2t_Q$-40	
				04		$2t_Q$-30	
Setup time, $\overline{\text{GI}}$ valid before LCLK1 no longer low	t_{su21}	See figure 3 (j) 16/	9,10,11	01-03	40		
				04	35		
Hold time, $\overline{\text{GI}}$ valid after LCLK1 going high	t_{h25}	See figure 3 (106)	9,10,11	All	0		
Delay time, LCLK2 going high to $\overline{\text{R0}}$ or $\overline{\text{R1}}$ valid	t_{d47}	See figure 3 (107)	9,10,11	01-03		t_Q+15	
				04		t_Q+13.5	
Delay time, LCLK2 high to $\overline{\text{R0}}$ or $\overline{\text{R1}}$ no longer valid	t_{d48}	See figure 3 (108)	9,10,11	01-03	t_Q-15		
				04	t_Q-13.5		
Delay time, LAD and RCA high-impedance after LCLK2 going low	t_{d49}	See figure 3 (109) 4/	9,10,11	01-03		t_Q+22+S	
				04		t_Q+20+S	
Delay time, LAD and RCA valid after LCLK1 going high	t_{d50}	See figure 3 (110)	9,10,11	01-03		t_Q+22	
				04		t_Q+20	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \leq T_C \leq +125°C$ V_{CC} = min to max 1/ 2/ unless otherwise specified	Group A subgroups	Device type	Limits Min	Limits Max	Unit
Delay time, $\overline{ALTCH}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{TR}/\overline{QE}$, $\overline{HOE}$, and HDST high-impedance after LCLK1 going high	t_{d51}	See figure 3 (111) 4/	9,10,11	01-03		t_Q+15	ns
				04		t_Q+13.5	
Delay time, $\overline{ALTCH}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{TR}/\overline{QE}$, $\overline{HOE}$, and HDST high-impedance after LCLK2 going low	t_{d52}	See figure 3 (112)	9,10,11	01-03		t_Q+15+S	
				04		t_Q+13.5 +S	
Delay time, DDIN high-impedance after LCLK1 going high	t_{d53}	See figure 3 (113) 4/	9,10,11	01-03		t_Q+15	
				04		t_Q+13.5	
Delay time, DDIN low after LCLK2 going low	t_{d54}	See figure 3 (114)	9,10,11	01-03		t_Q+15 +S	
				04		t_Q+13.5 +S	
Delay time, $\overline{DDOUT}$ high-impedance after LCLK2 going low	t_{d55}	See figure 3 (115) 4/	9,10,11	01-03		t_Q+15 +S	
				04		t_Q+13.5 +S	
Delay time, $\overline{DDOUT}$ high after LCLK2 going low	t_{d56}	See figure 3 (116)	9,10,11	01-03		t_Q+15+S	
				04		t_Q+13.5 +S	
Period, video serial clock SCLK	t_{c3}	See figure 3 (117)	9,10,11	01-03	35	50	
				04	25	50	
Pulse width, SCLK high	t_{w20}	See figure 3 (118)	9,10,11	01-03	12		
				04	10		
Pulse width, SCLK low	t_{w21}	See figure 3 (119)	9,10,11	01-03	12		
				04	10		
Transition time (rise and fall), SCLK	t_{t4}	See figure 3 (120) 4/	9,10,11	All	2	5	
Period, video input clock VCLK	t_{c4}	See figure 3 (123)	9,10,11	All	62.5	100	
Pulse width, VCLK high	t_{w22}	See figure 3 (124)	9,10,11	All	28		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \leq T_C \leq +125°C$ V_{CC} = min to max 1/ 2/ unless otherwise specified	Group A subgroups	Device type	Limits Min	Limits Max	Unit
Pulse width, VCLK low	t_{w23}	See figure 3 (125)	9,10,11	All	28		ns
Transition time (rise and fall), VCLK	t_{t5}	See figure 3 (126) 4/	9,10,11	All	2	5	
Delay time, VCLK low to HSYNC, VSYNC, CSYNC/HBLNK or CBLNK/VBLNK low	t_{d57}	See figure 3 (127)	9,10,11	All		40	
Delay time, VCLK low to HSYNC, VSYNC, CSYNC/HBLNK or CBLNK/VBLNK high	t_{d58}	See figure 3 (128)	9,10,11	All		40	
Hold time, VCLK going low to HSYNC, VSYNC, CSYNC/HBLNK or CBLNK/VBLNK going low	t_{h26}	See figure 3 (129) 4/	9,10,11	All	0		
Hold time, VCLK going low to HSYNC, VSYNC, CSYNC/HBLNK or CBLNK/VBLNK going high	t_{h27}	See figure 3 (130) 4/	9,10,11	All	0		
Setup time, HSYNC, VSYNC, CSYNC low to VLCK going high	t_{su22}	See figure 3 (131) 17/	9,10,11	All	20		
Setup time, HSYNC, VSYNC, CSYNC high to VLCK going high	t_{su23}	See figure 3 (132) 17/	9,10,11	All	20		
Hold time, HSYNC, VSYNC, CSYNC valid after VCLK high	t_{h28}	See figure 3 (133) 17/	9,10,11	All	20		
Setup time, LINT1 or LINT2 low before LCLK2 going high	t_{su24}	See figure 3 (134) 18/	9,10,11	01-03	t_Q+45		
				04	t_Q+40		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ V_{CC} = min to max 1/ 2/ unless otherwise specified	Group A subgroups	Device type	Limits Min	Limits Max	Unit
Pulse width, LINT1 or LINT2 low	t_{w24}	See figure 3 (135) 19/	9,10,11	All	$8t_Q$		ns
Delay time, LCLK1 going high to HINT valid	t_{d59}	See figure 3 (136)	9,10,11	01-03		30	
				04		25	
Setup time, EMU0-EMU2 valid to LCLK1 going high	t_{su25}	See figure 3 (137)	9,10,11	01-03	30		
				04	25		
Hold time, EMU0-EMU2 valid after LCLK1 going high	t_{h29}	See figure 3 (138)	9,10,11	All	0		
Delay time, EMU3 valid after LCLK1 low	t_{d60}	See figure 3 (139)	9,10,11	01-03		25	
				04		20	
Hold time, LCLK2 high before EMU3 not valid	t_{h30}	See figure 3 (140)	9,10,11	01-03	t_Q-15		
				04	t_Q-13.5		

1/ All test to be performed at worst-case test condition unless otherwise specified.
2/ t_Q = quarter cycle, nt_Q = An integral number of quarter cycles. S = t_Q if using the clock stretch, 0 ns if otherwise.
3/ EMU0-2 will not be connected in a typical configuration. Nominal pull-up current for EMU0-2, HREAD and HWRITE will be 600 µA.
4/ These values are based on characterization or computer simulation and are not tested.
5/ These timings are required only to synchronize the device to a particular quarter cycle.
6/ The initial reset pulse on powerup must remain valid until all internal states have been initialized. Resets applied after the device has been initialized need to be present only long enough to be recognized by the internal logic; the internal logic will maintain an internal reset until all internal states have been initialized (34 LCLK1 cycles).
7/ Parameter t_{d1} (9) is the maximum amount by which the RESET low-to-high transition can be delayed after the start of the HCS low-to-high transition and still guarantee that the device is configured to run in the self-bootstrap mode (HLT bit = 0) following the end of reset.
8/ This is a functional minimum and is not tested. This parameter may also be specified as $4t_Q$.
9/ These parameters are common to all output signals from the device unless otherwise specifically given. They are intended as an aid to estimate the timing requirements. Please reference the specific numbered parameter for actual times. "n" is an integral number of quarter cycles.
10/ Setup time to insure recognition of input on this clock edge.
11/ Hold time required to guarantee response on next clock edge. These values are based on computer simulation and are not tested.
12/ When the device is set for block reads, use the deassertion of HREAD to request a local memory cycle at the next sequential address location.
13/ DDIN is used to control LAD bus buffers between the device and local memory. Parameter t_{en1} (74) references the time for these data buffers to go from a high-impedance state to an active level. Parameter t_{dis1} (75) references the time for the buffers to go from an active level to the high-impedance state.
14/ Parameters t_{su17} (87) and t_{h22} (88) also apply to WE, TR/QE, and SF relative to RAS.
15/ S' = $2t_Q$ when using the clock stretch since both the address cycle and read cycle of a read-modify-write will be stretched, 0 ns otherwise.
16/ These timings must be met to insure that the GI input is recognized on this clock cycle.
17/ Setup and hold times on asynchronous inputs are required only to guarantee recognition at indicated clock edges.
18/ Although LINT1 and LINT2 may be asynchronous to the device, this setup insures recognition of the interrupt on this clock edge.
19/ This pulse duration minimum insures that the interrupt is recognized by internal logic; however, the level must be maintained until it has been acknowledged by the interrupt service routine.

Device types	01,02,03 and 04						
Case outline	X						
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
A1	Vss	C9	RCA8	J1	EMU0	N15	LAD17
A2	ALTCH	C10	RCA12	J2	GI	P1	Vcc
A3	CBLNK/VBLNK	C11	LAD30	J3	EMU1	P2	HWRITE
A4	HSYNC	C12	Vss	J13	LAD4	P3	HCS
A5	TR/QE	C13	Vss	J14	Vcc	P4	HA30
A6	RCA2	C14	Vcc	J15	LAD5	P5	HA27
A7	RCA3	C15	LAD26	K1	EMU2	P6	HA24
A8	Vcc	D1	RAS	K2	RESET	P7	HA22
A9	RCA6	D2	CAS2	K3	LINT2	P8	HA18
A10	RCA7	D3	Vss	K13	Vss	P9	HA14
A11	RCA10	D4	NC	K14	LAD3	P10	HA13
A12	SCLK	D13	LAD28	K15	LAD20	P11	HA10
A13	LAD15	D14	LAD11	L1	LINT1	P12	HA7
A14	LAD29	D15	LAD10	L2	CAMD	P13	HA5
A15	Vss	E1	R1	L3	LRDY	P14	HBS0
B1	CAS3	E2	Vcc	L13	LAD1	P15	LAD0
B2	WE	E3	CAS1	L14	LAD2	R1	HREAD
B3	Vss	E13	LAD27	L15	LAD19	R2	HA31
B4	CSYNC/HBLNK	E14	LAD25	M1	BUSFLT	R3	HA28
B5	VSYNC	E15	LAD9	M2	PGMD	R4	HA26
B6	RCA0	F1	HRDY	M3	VCLK	R5	HA23
B7	RCA1	F2	R0	M13	Vss	R6	HA20
B8	RCA5	F3	Vss	M14	LAD16	R7	HA19
B9	RCA9	F13	LAD24	M15	LAD18	R8	HA17
B10	RCA11	F14	LAD8	N1	SIZE16	R9	HA16
B11	LAD31	F15	Vss	N2	Vcc	R10	HA15
B12	LAD14	G1	HINT	N3	CLKIN	R11	HA11
B13	Vcc	G2	HOE	N4	Vss	R12	HA9
B14	LAD13	G3	HDST	N5	HA29	R13	HA8
B15	LAD12	G13	LAD7	N6	HA25	R14	HBS3
C1	CAS0	G14	Vss	N7	HA21	R15	Vss
C2	Vcc	G15	LAD23	N8	Vss		
C3	DDOUT	H1	LCKL1	N9	Vss		
C4	DDIN	H2	EMU3	N10	HA12		
C5	Vss	H3	LCLK2	N11	HA6		
C6	SF	H13	LAD22	N12	HBS2		
C7	RCA4	H14	LAD21	N13	HBS1		
C8	Vss	H15	LAD6	N14	Vcc		

FIGURE 1. Terminal connections.

Device types	01,02.03 and 04						
Case outline	Y						
Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	CAS3	34	HCS	67	LAD0	100	LAD29
2	CAS2	35	HA31	68	LAD16	101	LAD14
3	CAS1	36	HA30	69	LAD1	102	LAD30
4	CAS0	37	HA29	70	LAD17	103	LAD15
5	Vcc	38	HA28	71	LAD2	104	LAD31
6	RAS	39	HA27	72	LAD18	105	SCLK
7	Vss	40	HA26	73	Vss	106	RCA12
8	R0	41	HA25	74	LAD3	107	RCA11
9	R1	42	HA24	75	LAD19	108	RCA10
10	HOE	43	HA23	76	Vcc	109	RCA9
11	HDST	44	HA22	77	LAD4	110	RCA8
12	HRDY	45	HA21	78	LAD20	111	RCA7
13	HINT	46	HA20	79	LAD5	112	RCA6
14	EMU3	47	HA19	80	LAD21	113	RCA5
15	LCLK1	48	HA18	81	LAD6	114	Vcc
16	LCLK2	49	HA17	82	LAD22	115	Vss
17	EMU1	50	Vss	83	LAD7	116	RCA4
18	EMU0	51	HA16	84	LAD23	117	RCA3
19	EMU2	52	HA15	85	Vss	118	RCA2
20	GI	53	HA14	86	Vss	119	RCA1
21	RESET	54	HA13	87	LAD8	120	RCA0
22	LINT2	55	HA12	88	LAD24	121	SF
23	LINT1	56	HA11	89	LAD9	122	TR/QE
24	CAMD	57	HA10	90	LAD25	123	VSYNC
25	BUSFLT	58	HA9	91	LAD10	124	HSYNC
26	SIZE16	59	HA8	92	LAD26	125	CBLNK/VBLNK
27	PGMD	60	HA7	93	LAD11	126	CSYNC/HBLNK
28	LRDY	61	HA6	94	LAD27	127	Vss
29	Vcc	62	HA5	95	Vcc	128	Vss
30	VCLK	63	HBS3	96	LAD12	129	ALTCH
31	CLKIN	64	HBS2	97	LAD28	130	DDIN
32	HWRITE	65	HBS1	98	Vss	131	DDOUT
33	HREAD	66	HBS0	99	LAD13	132	WE

FIGURE 1. Terminal connections - Continued.

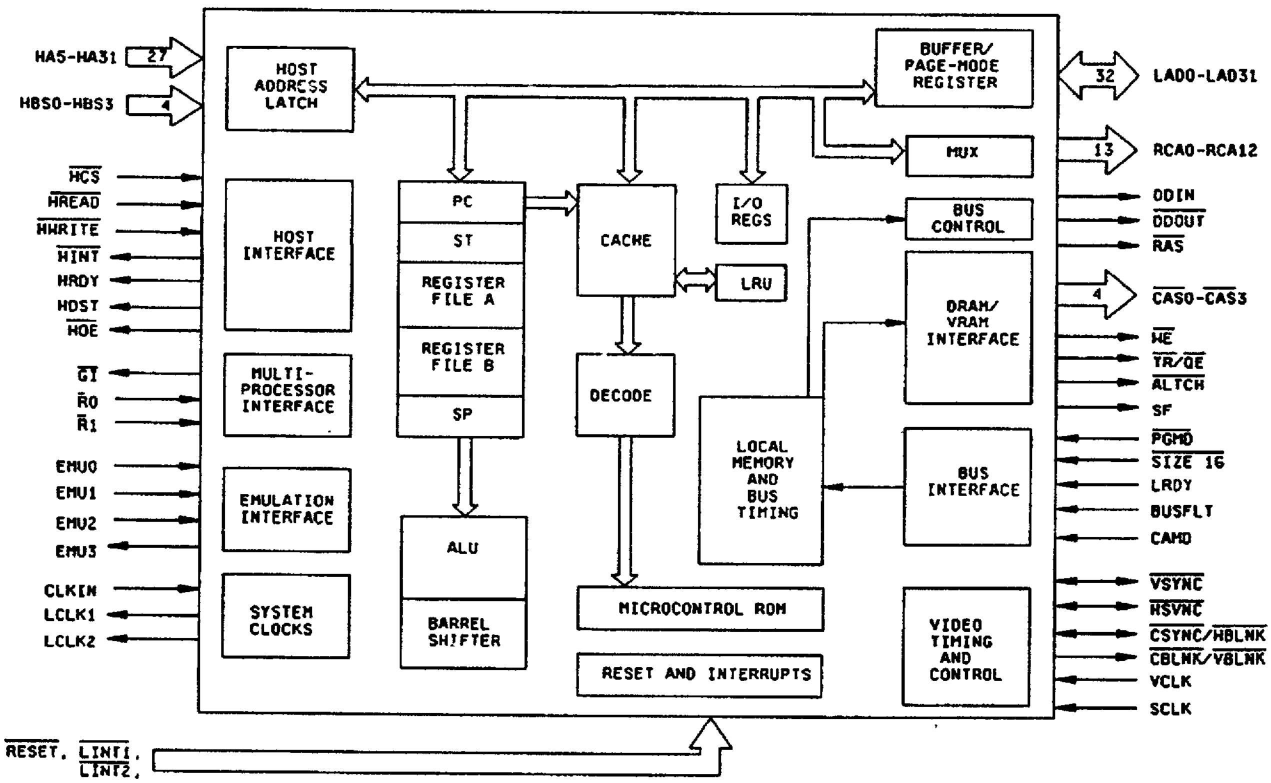
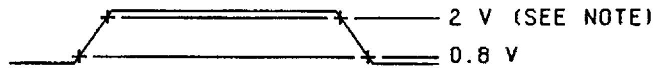


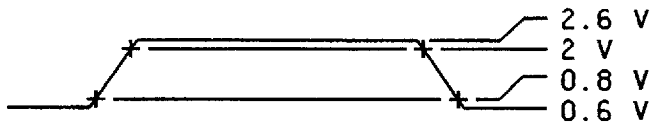
FIGURE 2. Functional block diagram.

Signal transition levels



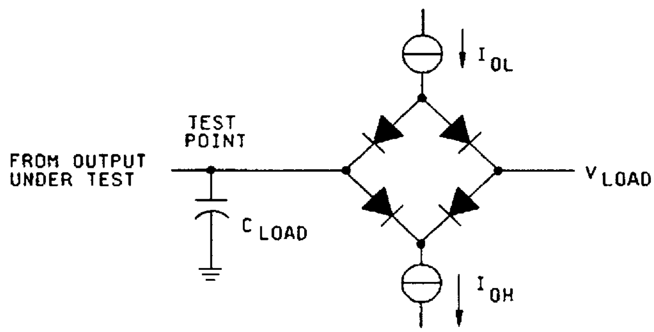
NOTE: 2.2 V for BUSFLT, VCLK, LRDY $\overline{PGMD}$, $\overline{SIZE16}$. 3 V for CLKIN.

TTL-level inputs



Note: For timing measurements, a V_{OL} trip level of 1.0 V is used at 25°C and 125°C, and 1.5 V is used at -55°C.

TTL-level output



NOTE: I_{OL} = 2 mA (all outputs)
I_{OH} = 400 µA (all outputs)
V_{LOAD} = 1.5 V
C_{LOAD} = 80 pF typical load circuit capacitance

Test load circuit

FIGURE 3. Load circuit and waveforms.

CLKIN and $\overline{RESET}$ timing requirements

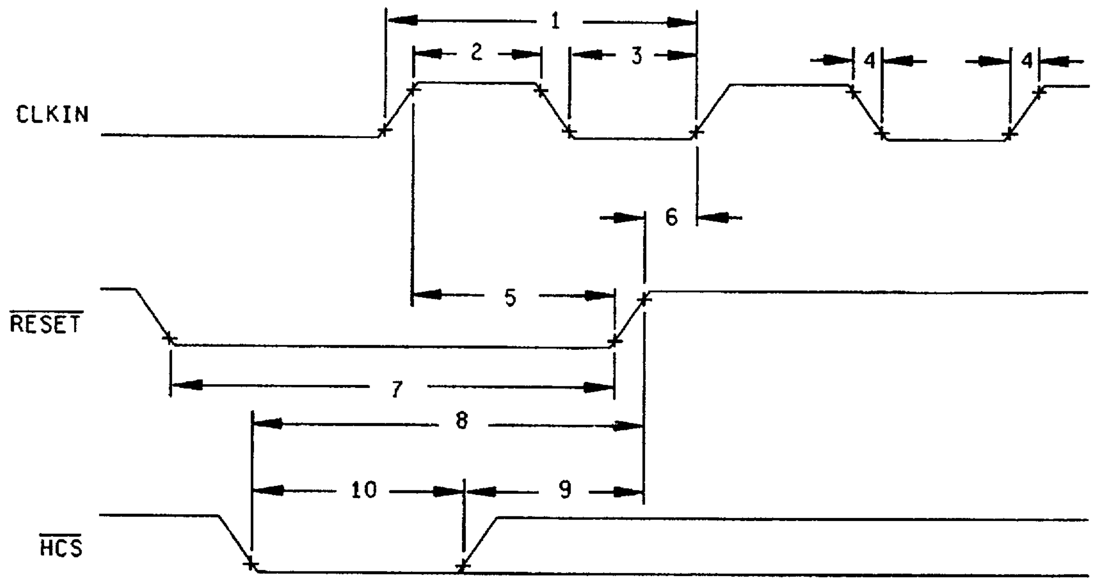
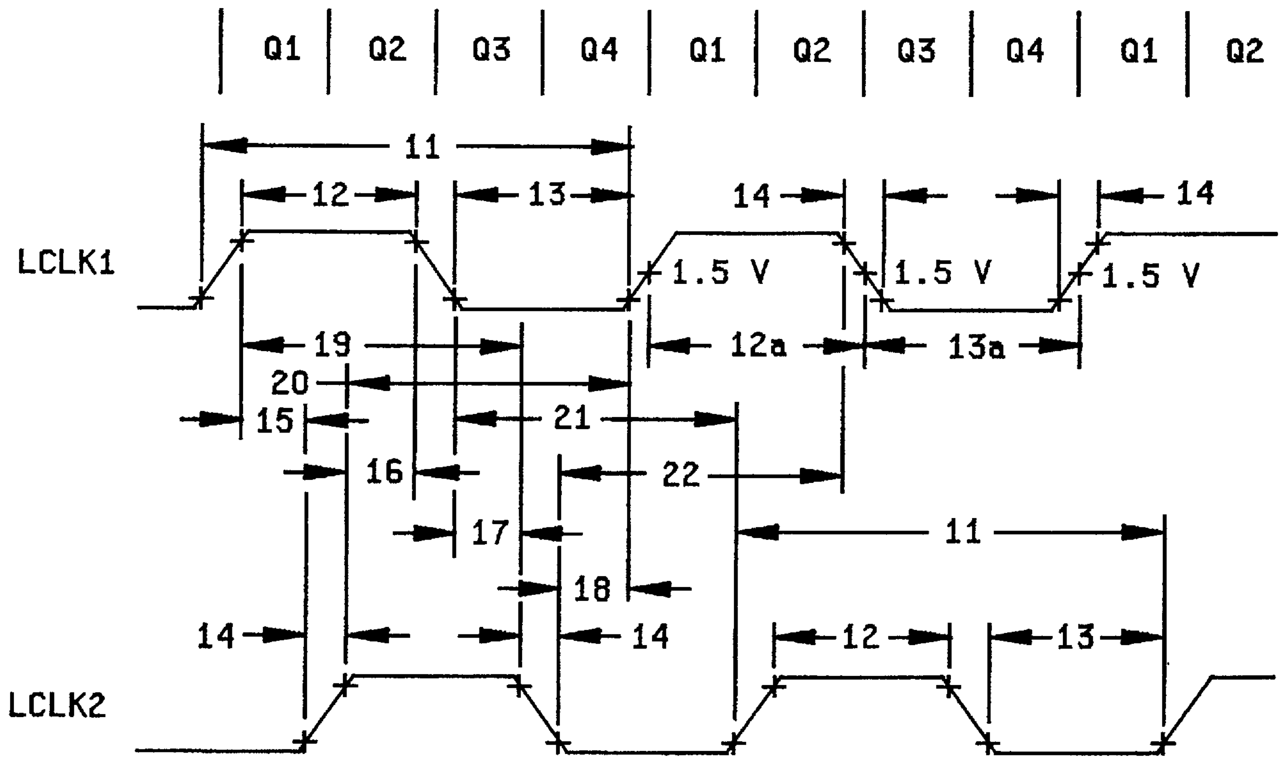


FIGURE 3. Load circuit and waveforms - Continued.

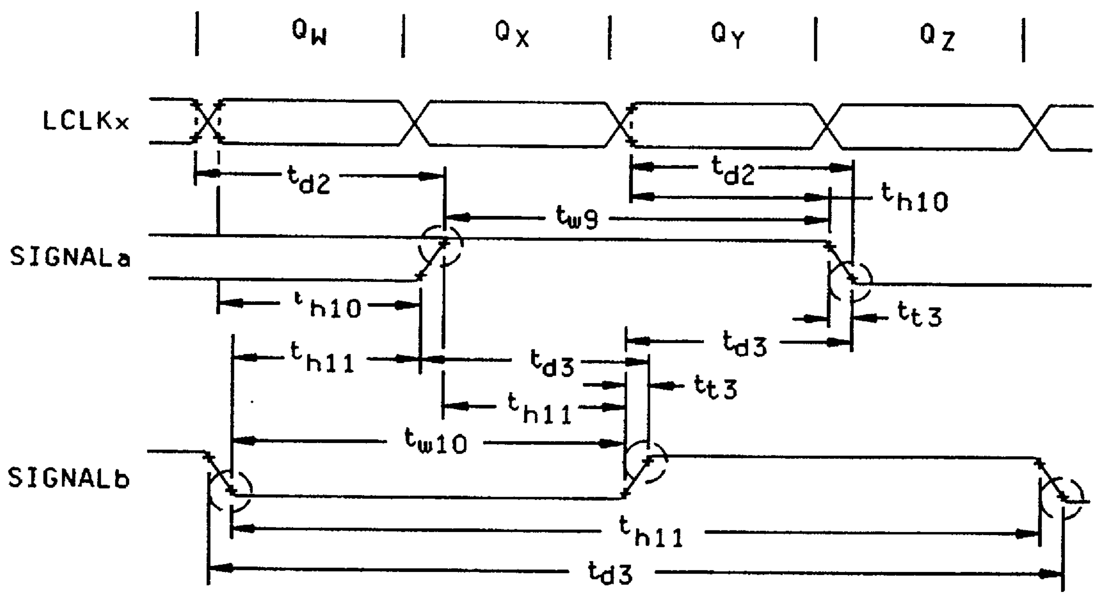
Local bus timing: Output clocks



Note: Although LCLK1 and LCLK2 are derived from CLKIN, no timing relationship between CLKIN and the local clocks is to be assumed, except the period of the local clocks is four times the period of CLKIN.

FIGURE 3. Load circuit and waveforms - Continued.

Output signal characteristics



indicates the point at which the signal has attained a valid level.

FIGURE 3. Load circuit and waveforms - Continued.

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Host interface timing requirements

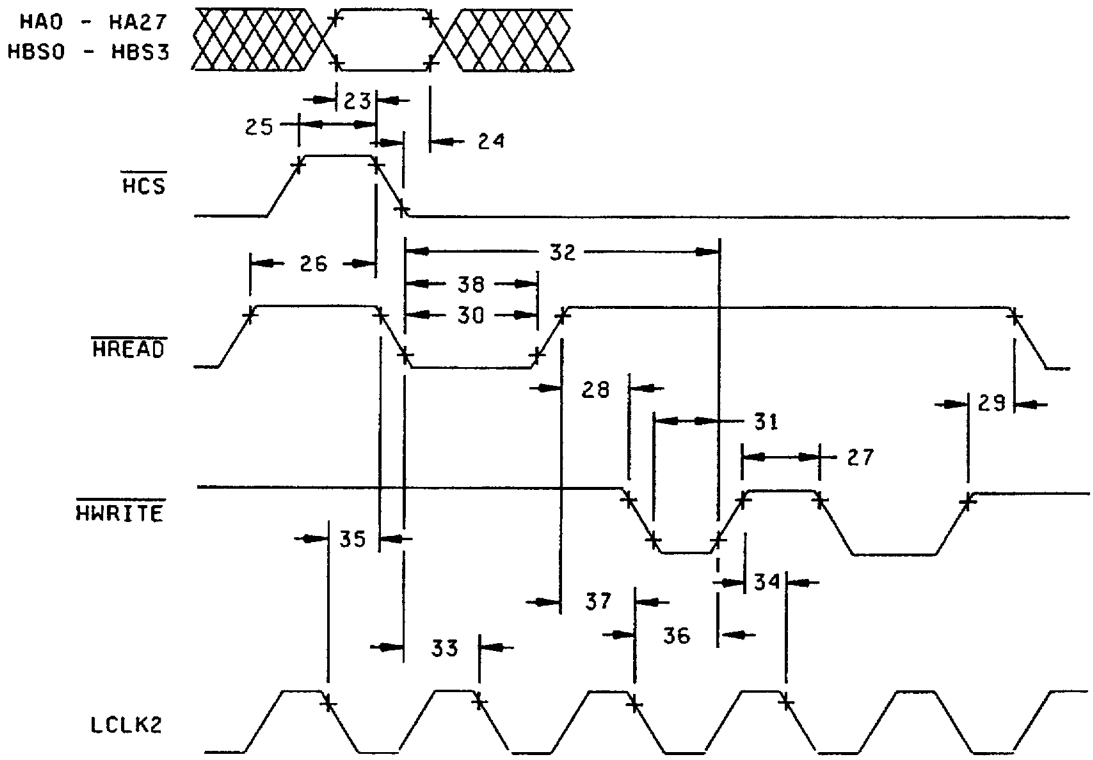


FIGURE 3. Load circuit and waveforms - Continued.

Host interface timing responses (random read cycle)

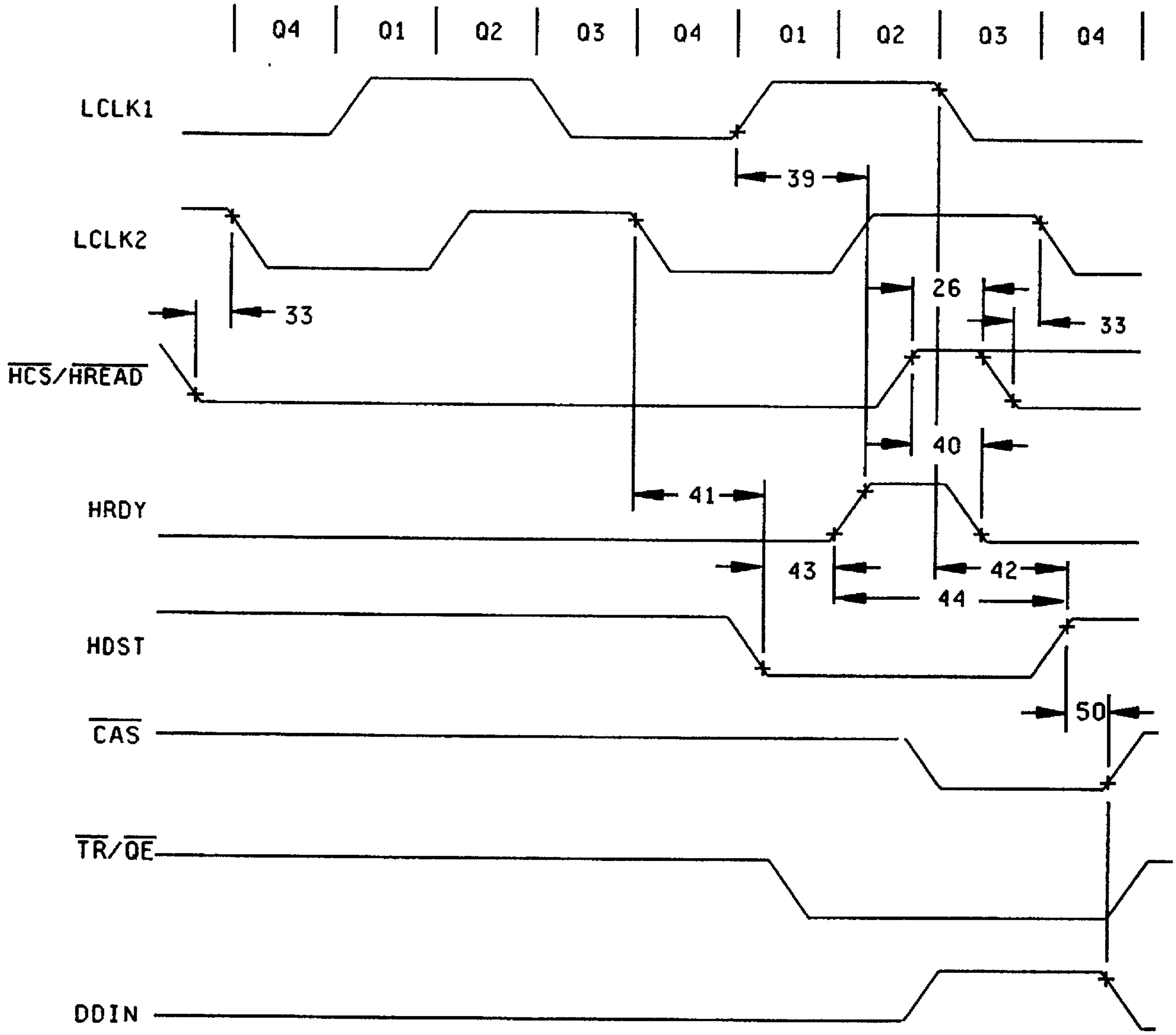
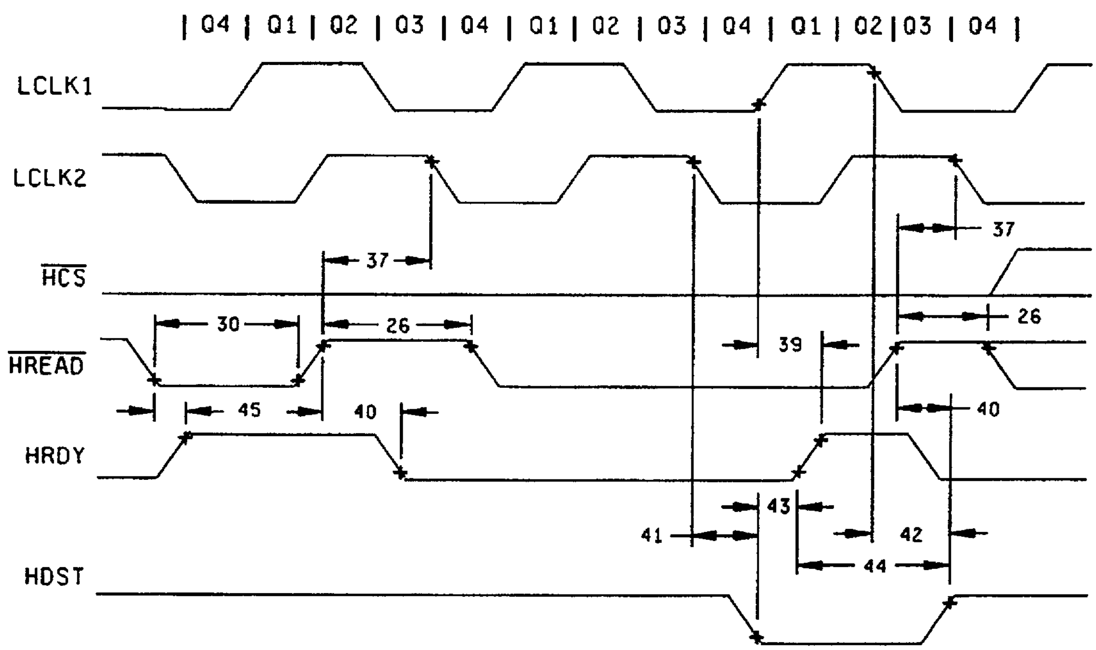


FIGURE 3. Load circuit and waveforms - Continued.

Host interface timing (block read cycle)



Note: Although HCS, HREAD, and HWRITE may be totally asynchronous to the device, cycle reponses to the signals are determined by local memory cycles.

FIGURE 3. Load circuit and waveforms - Continued.

Host interface timing responses (write cycle)

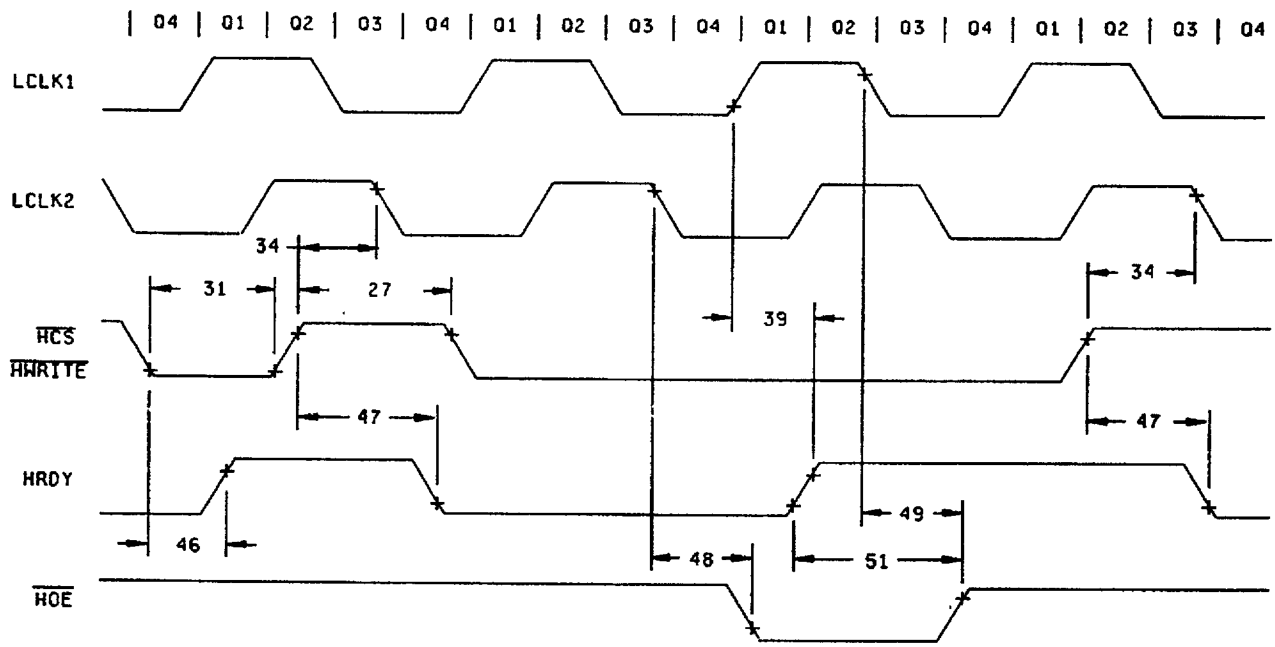


FIGURE 3. Load circuit and waveforms - Continued.

Local bus timing: Bus control inputs

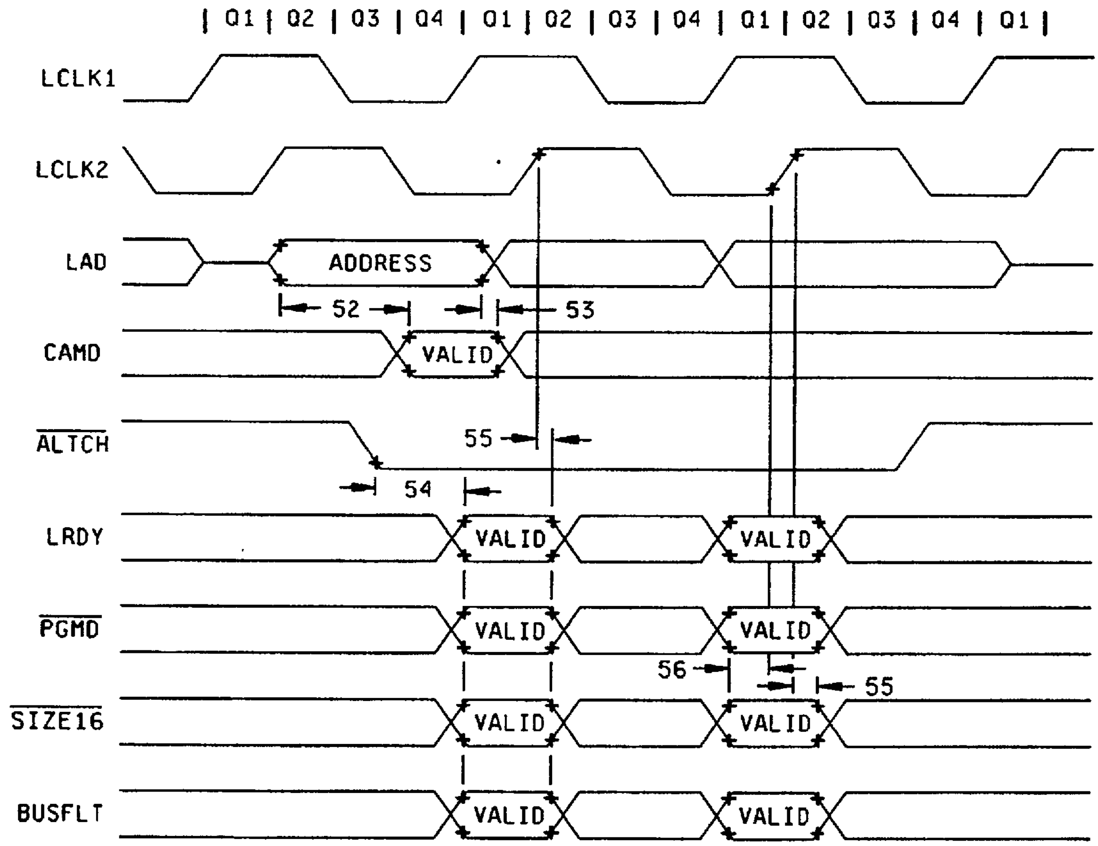


FIGURE 3. Load circuit and waveforms - Continued.

Local bus timing

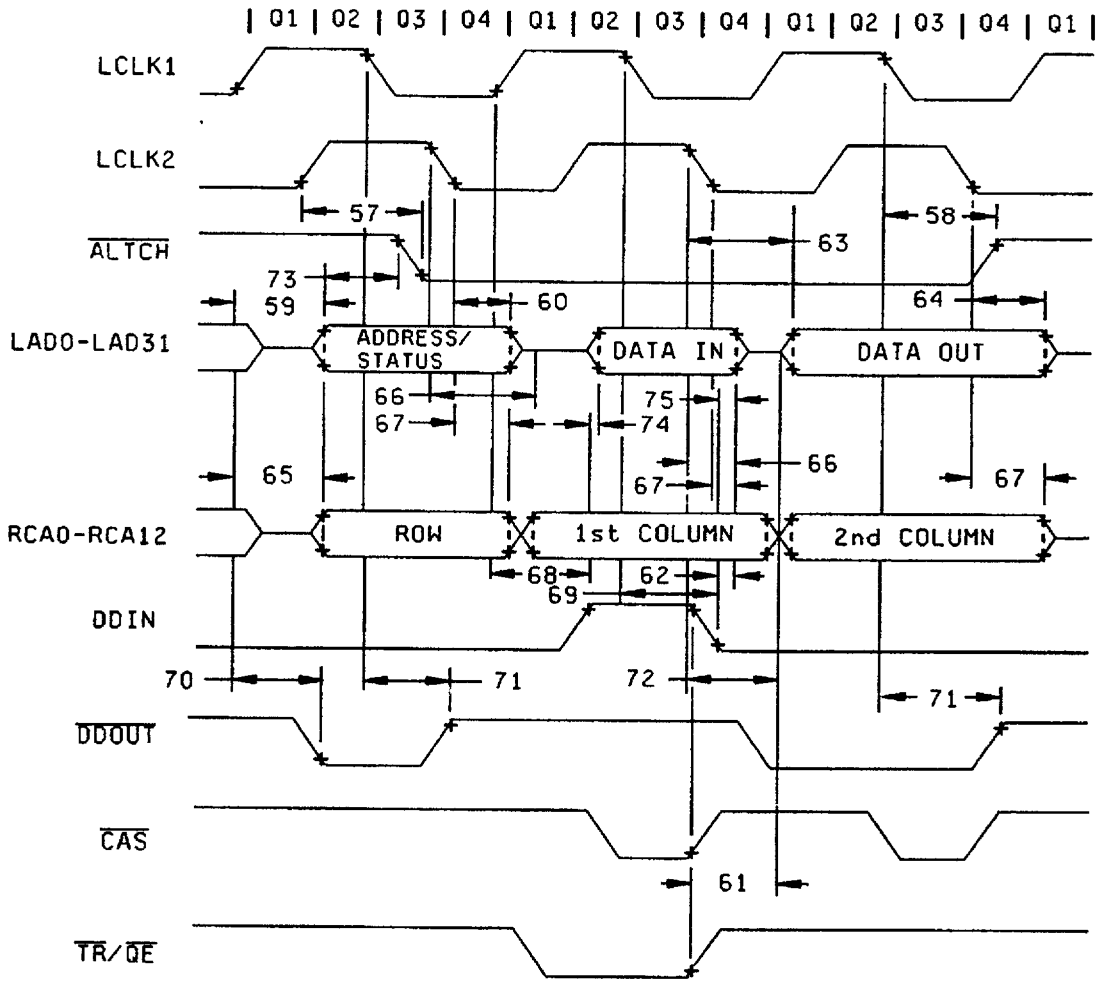


FIGURE 3. Load circuit and waveforms - Continued.

Local bus timing

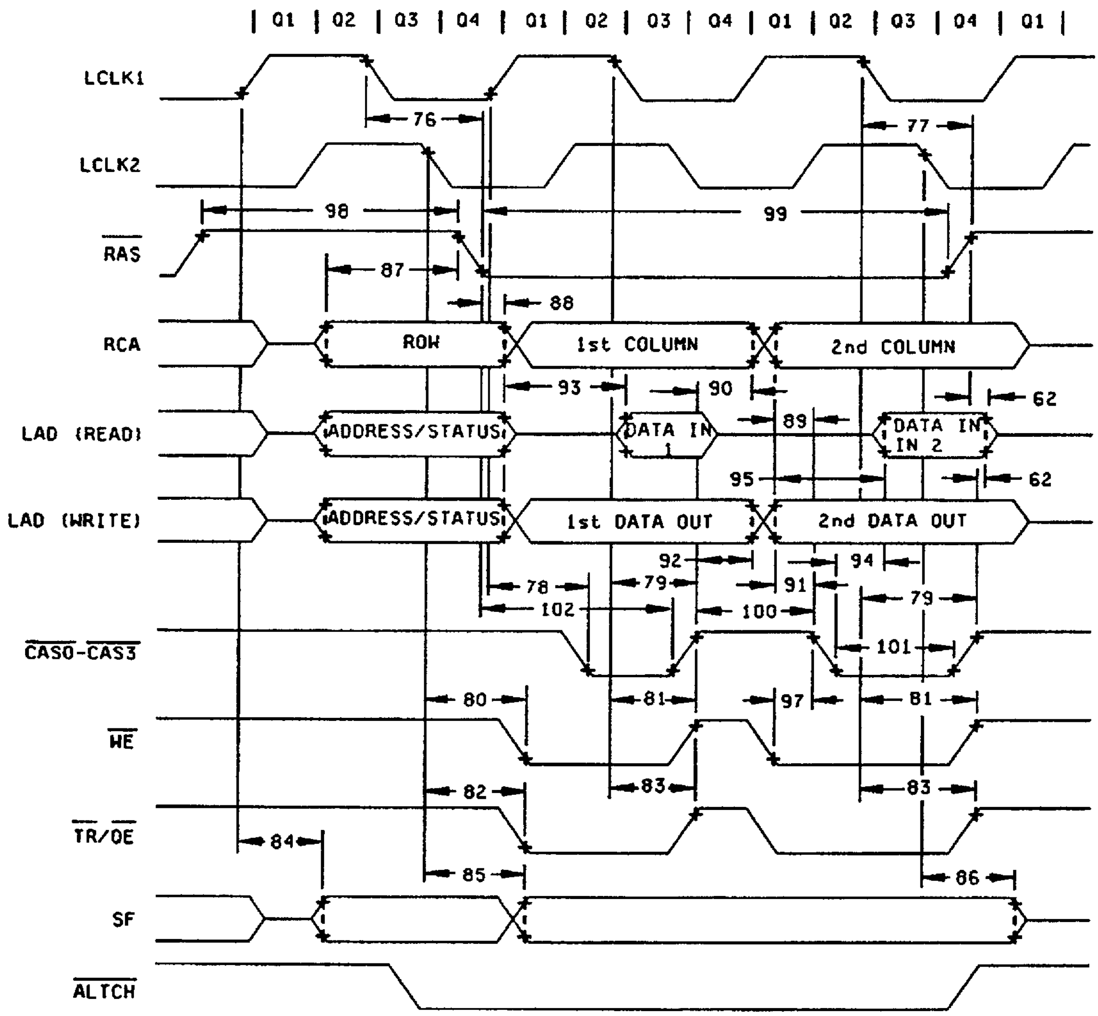


FIGURE 3. Load circuit and waveforms - Continued.

$\overline{CAS}$-before-$\overline{RAS}$ refresh: $\overline{RAS}$ and $\overline{CAS0}$-$\overline{CAS3}$

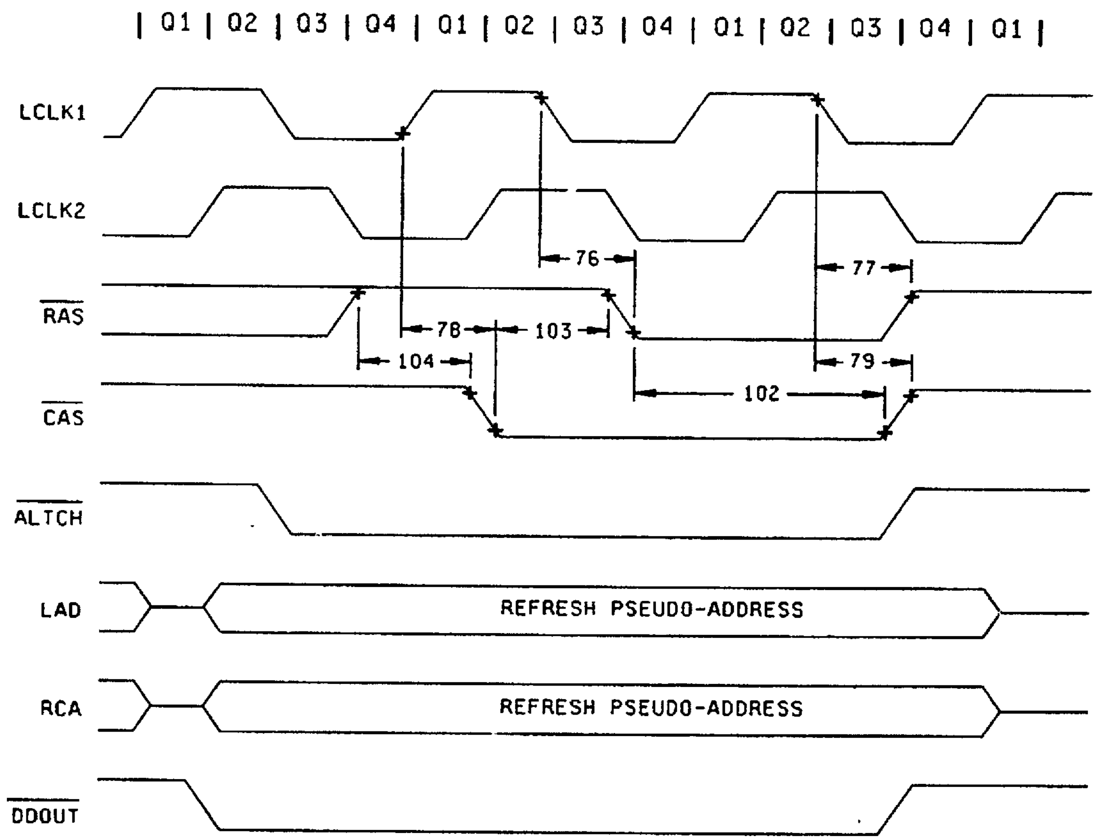
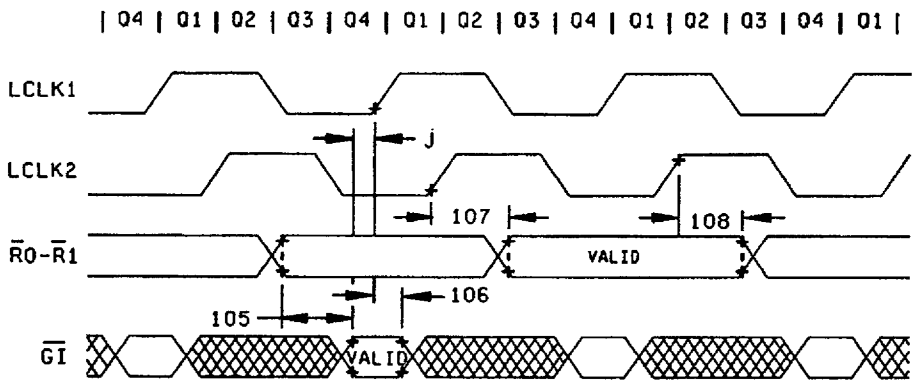


FIGURE 3. Load circuit and waveforms - Continued.

Multiprocessor interface timing: $\overline{GI}$, $\overline{ALTCH}$, $\overline{RAS}$, $\overline{R0}$, and $\overline{R1}$



Note: For the device to gain control of the local bus during a given cycle, its $\overline{GI}$ pin must be low at the start of Q1 (indicating that the bus arbitration logic is granting the bus to this processor).

FIGURE 3. Load circuit and waveforms - Continued.

Multiprocessor interface timing: High-impedance signals

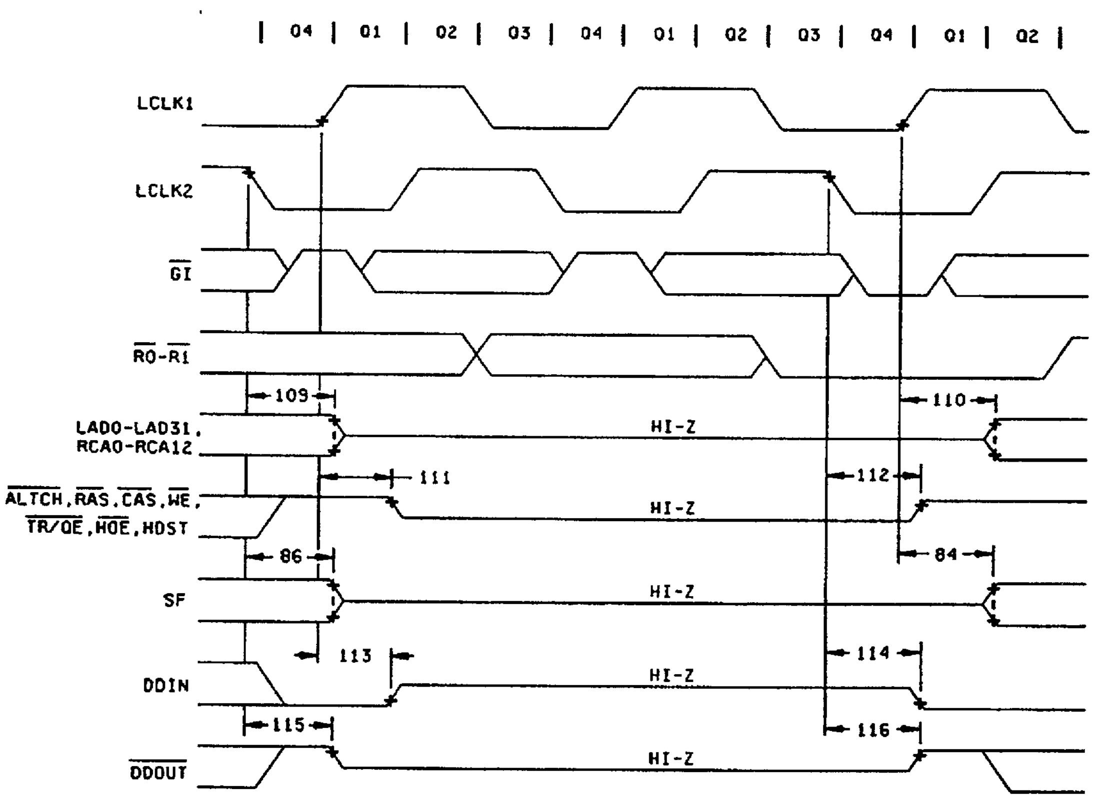
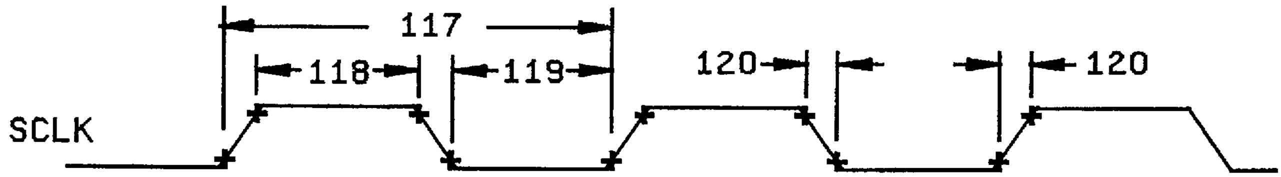


FIGURE 3. Load circuit and waveforms - Continued.

Video shift clock timing: SCLK



Video interface timing: VCLK and video outputs

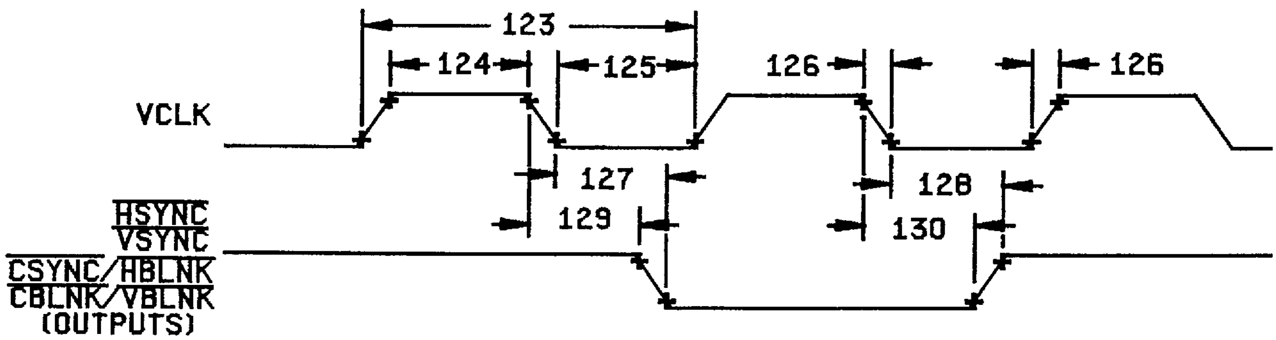
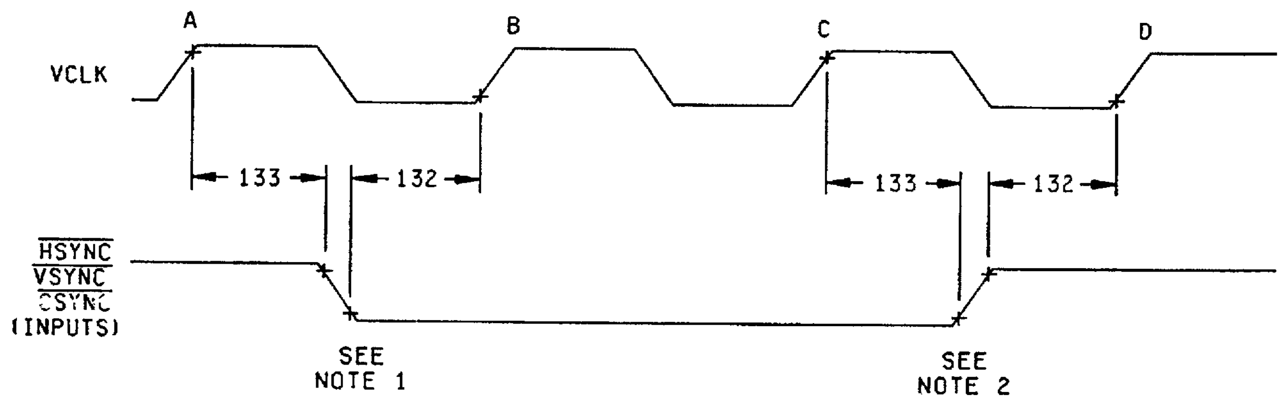


FIGURE 3. Load circuit and waveforms - Continued.

Video interface timing: External sync inputs



Notes:

1. If the falling edge of the sync signal occurs more than $t_{h(VCKH-SV)}$ after VCLK edge A and at least t_{SU} (SL-VCKH before edge B, the transition will be detected at edge B instead of edge A.

2. If thefallind edge of the sync signal occurs more than $t_{h(VCKH-SV)}$ after VCLK edge C and at least $t_{SU(SH-VCKH+1)}$ before edge D, the transition will be detected at edge D instead of edge C.

Interrupt timing: $\overline{\text{LINT1}}$ and $\overline{\text{LINT2}}$

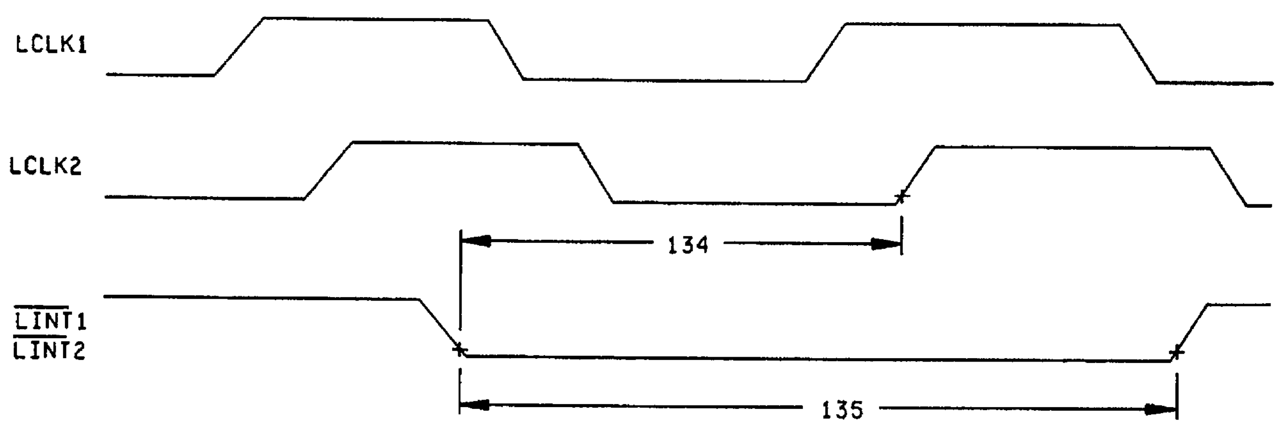
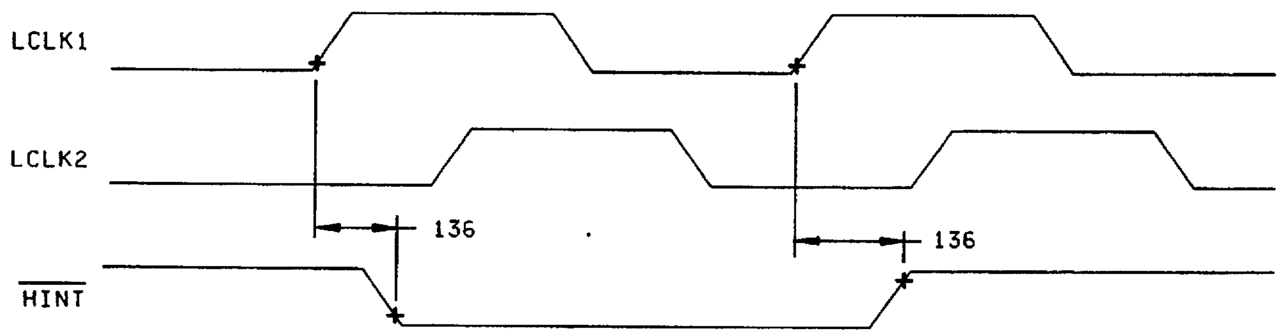


FIGURE 3. Load circuit and waveforms - Continued.

Host interupt timing: $\overline{HINT}$



Emulator interface timing

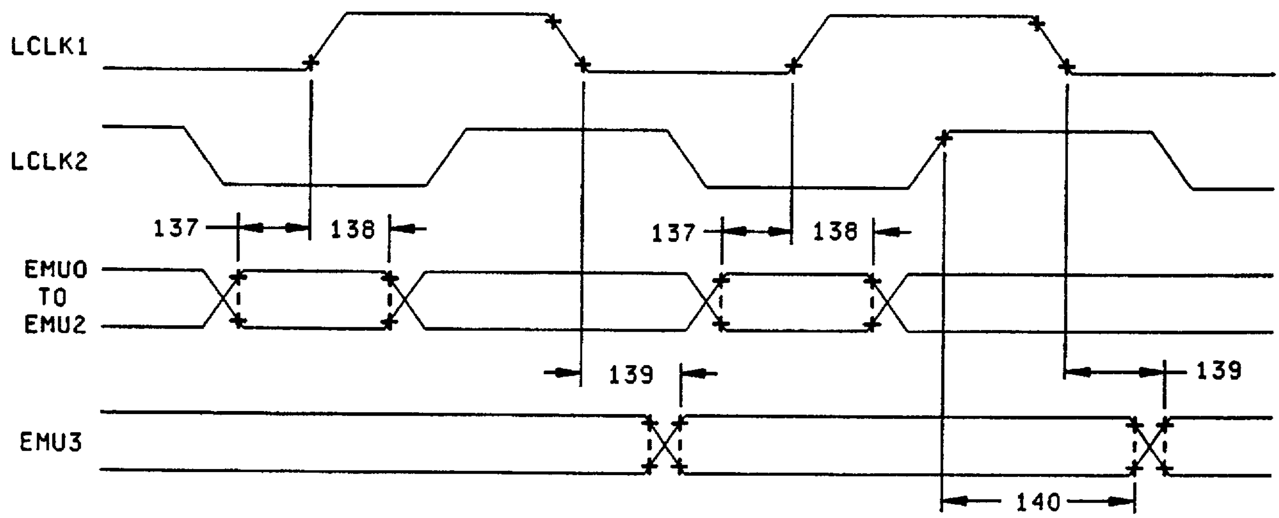


FIGURE 3. Load circuit and waveforms - Continued.

4.2 Screening. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. For device classes Q and V, screening shall be in accordance with MIL-I-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-I-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in appendix B of MIL-I-38535.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-I-38535. Inspections to be performed shall be those specified in MIL-I-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Quality conformance inspection for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein) and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4). Technology conformance inspection for classes Q and V shall be in accordance with MIL-I-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-I-38535 permits alternate in-line control testing. For device classes Q and V only, the electrical subgroup requirements specified in Table II herein are the baseline requirements but may be modified in the device manufactureres approved QM plan.

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the functionality of the device. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).

c. Subgroup 4 (C_{IN} and C_{OUT}) shall be measured only for the initial test and after process or design process or design changes which may affect capacitance. A minimum sample size of five devices with zero rejects shall be required.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, TM 5005, table I)	Subgroups (in accordance with MIL-I-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1, 2, 3		1, 2, 3
Final electrical parameters (see 4.2)	1, 2, 3, 7, 8, 1/ 9, 10, 11	1, 2, 3, 7, 1/ 8, 9, 10, 11	1, 2, 3, 7 2/ 8, 9, 10, 11
Group A test requirements (see 4.4)	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7 8, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3	1, 2, 3
Group D end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3	1, 2, 3
Group E end-point electrical parameters (see 4.4)	- - -	- - -	- - -

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1 and 7.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB, in accordance with MIL-I-38535, and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes Q and V shall be M, D, R, and H and for device class M shall be M and D.

a. End-point electrical parameters shall be as specified in table II herein.

b. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-I-38535, appendix A, for the RHA level being tested. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-I-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-STD-883 (see 3.1 herein) for device class M and MIL-I-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and which SMD's are applicable to that system. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DESC-EC, telephone (513) 296-6047.

6.4 Comments. Comments on this drawing should be directed to DESC-EC, Dayton, Ohio 45444-5270, or telephone (513) 296-5377.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-I-38535 and MIL-STD-1331 and as follows.

LOCAL MEMORY INTERFACE

NAME	I/O	DESCRIPTION
$\overline{\text{ALTCH}}$	O	Address latch. The high-to-low transitions of $\overline{\text{ALTCH}}$ can be used to capture the address and status present on the LAD signals. A transparent latch will maintain the current address and status as long as ALTCH remains low.
BUSFLT	I	Bus fault. External logic asserts BUSFLT high to the device to indicate that an error or fault has occurred on the current bus cycle. BUSFLT is also used with LRDY to generate externally requested bus cycle retries so that the entire memory address is presented again on the LAD pins. In the emulation mode, BUSFLT is used for write protecting mapped memory (by disabling $\overline{\text{CAS}}$ outputs for the current cycle).
DDIN	O	Data bus direction in enable. This active-high output is used to drive the active-high output-enables on bidirectional transceivers. The transceivers buffer data input and output on the LAD0-LAD31 pins when the device is interfaced to several memories.
$\overline{\text{DDOUT}}$	O	Data bus direction output-enable. This active-low signal drives the active-low output-enables on bidirectional transceivers. The transceivers buffer data input and output on the LAD0-LAD31 pins.

LAD0-LAD31	I/O	32-bit multiplexed local address/data bus. At the beginning of a memory cycle, the word address is output on LAD4-LAD31 and the cycle status is output on LAD0-LAD3. After the address is presented, LAD0-LAD31 are used for transferring data within the system. LAD0 is the LSB and LAD31 is the MSB.
LRDY	I	Local ready. External circuitry drives this signal low to inhibit the device from completing a local-memory cycle it has initiated. While LRDY remains low the device will wait, unless the device loses bus priority or is given an external RETRY request (through the BUSFLT signal). Wait states are generated in increments of one full LCLK1 cycle. LRDY can be driven low to extend local-memory read and write cycles, VRAM serial-data-register transfer cycles, and DRAM refresh cycle. During internal cycles, the device ignores LRDY.
$\overline{\text{PGMD}}$	I	Page mode. The memory decode logic asserts this signal low if the currently addressed memory supports burst (page mode) accesses. Burst accesses occur as a series of CAS cycles from a single $\overline{\text{RAS}}$ cycle to memory. LRDY is used with BUSFLT to describe the cycle termination status for a memory cycle. PGMD is also used in emulation mode for mapping memory.
$\overline{\text{SIZE16}}$	I	Bus size. The memory decode logic may pull this signal low if the currently addressed memory or port supports only 16-bit transfers. SIZE16 can also be used to determine which 16 bits of the data bus are used for a data transfer. In the emulation mode, $\overline{\text{SIZE16}}$ is used to select the size of mapped memory.
		DRAM and VRAM CONTROL
CAMD	I	Column-address mode. This input dynamically shifts the column address on the RCA0-RCA12 bus to allow the mixing of DRAM and VRAM address matrices using the same multiplexed address RCA0-RCA12 signals.
$\overline{\text{CAS0}}$-$\overline{\text{CAS3}}$	O	4 column-address strobes. The $\overline{\text{CAS}}$ outputs drive the $\overline{\text{CAS}}$ inputs of DRAMs and VRAMs. These signals strobe the column address on RCA0-RCA12 to the memory. The four $\overline{\text{CAS}}$ strobes provide byte write-access to the memory.
$\overline{\text{RAS}}$	O	Row-address strobe. The $\overline{\text{RAS}}$ output drives the $\overline{\text{RAS}}$ inputs of DRAMs and VRAMs. This signal strobes the row address on RCA0-RCA12 to memory.
RCA0-RCA12	O	13 multiplexed row-address/column-address signals. At the beginning of a memory-access cycle, the row address for DRAMs is present on RCA0-RCA12. The row address contains the most significant address bits for the memory. As the cycle progresses, the memory column address is placed on RCA0-RCA12. The addresses that are actually output during row and column times depend on the memory configuration (set by RCM0 and RCM1 in the CONFIG register) and the state of CAMD during the access. RCA0 is the LSB and RCA12 is the MSB.
SF	O	Special-function pin. This is the special-function signal to 1 M VRAMs that allows the use of block write, load write mask, load color mask, and write using write mask. This signal is also used to differentiate instructions and addresses for the coprocessor as part of the coprocessor interface.
$\overline{\text{TR/QE}}$	O	Transfer/output-enable. This signal drives the $\overline{\text{TR/QE}}$ input of VRAMs. During a local-memory read cycle, TR/QE functions as an active-low output-enable to gate from memory to LAD0-LAD31. During special VRAM function cycles, TR/QE controls the type of cycle that is performed.
$\overline{\text{WE}}$	O	Write enable. The active low $\overline{\text{WE}}$ output drives the $\overline{\text{WE}}$ inputs of DRAMs and VRAMs. $\overline{\text{WE}}$ can also be used as the active-low write-enable to static memories and other devices connected to the local interface of the device. During a local-memory read cycle, WE remains inactive high while CAS is strobed active low. During a local-memory write cycle, WE is strobed active low before CAS. During VRAM serial-data-register transfer cycles, the state of WE at the falling edge of RAS controls the direction of the transfer.

HOST INTERFACE

HA5-HA31	I	27 host-address input signals. A host can access a long word by placing the address on these lines. HA5-HA31 correspond to the LAD5-LAD31 signals that output the address to the local memory.
HBS0-HBS3	I	4 host byte-selects. The byte-selects identify which bytes within the long word are being selected.
HCS	I	Host chip select. A host drives this signal low to latch the current host address present on HA5-HA31 and the host byte-selects on HBS0-HBS3. This signal also enables host access cycles to the device I/O registers or local memory. During the low-to-high transition of RESET, the level on the HCS input determines whether the device is halted (HCS is high for host-present mode) or whether it begins executing it's reset service routine (HCS is low for self-bootstrap mode).
HDST	O	Host data latch strobe. The rising edge of this signal latches data from the device local address space to the external host data latch on host read access. It can be used in conjunction with HRDY to indicate that data is valid in the external data latch.
HINT	O	Host interrupt. This signal allows the device to interrupt a host by setting the INTOUT bit in the HSTCTLL I/O register. This signal can also be used to interrupt the host if a BUSFLT or RETRY occurs due to a host access cycle.
HOE	O	Host data latch output-enable. This signal enables data from host data latches to the device local address space on host write cycles. HOE can be used in conjunction with HRDY to indicate data has been written to memory from the external data latch.
HRDY	O	Host ready. This signal is normally low and goes high to indicate that the device is ready to complete a host-initiated read or write cycle. If the device is ready to accept the access request, HRDY is driven high and the host can proceed with the access. A host can use HRDY logically combined with HDST and HOE to determine when the local bus access cycles have completed.
HREAD	I	Host read strobe. This signal is driven low during a read request from a host processor. This notifies the device that the host is requesting access to the I/O registers or to local memory. HREAD should not be asserted at the same time the HWRITE is asserted.
HWRITE	I	Host write strobe. This signal is driven low to indicate a write request by a host processor. This identifies the device that a write request is pending. The rising edge of HWRITE is used to indicate that the host has latched data to be written in the external data transceivers. HWRITE should not be asserted at the same time HREAD is asserted.

SYSTEM CONTROL

CLKIN	I	Clock Input. This system input clock generates the LCLK1 and LCLK2 outputs, to which all processor functions in the device are synchronous. A separate asynchronous input clock (VCLK) controls the video timing and video registers.
LCLK1, LCLK2	O	Local output clocks. These two clocks are 90 degrees out of phase with each other. They provide convenient synchronous control of external circuitry to the internal timing. All signals output from the device (except the CRT timing signals) are synchronous to these clocks.
LINT1, LINT2	I	Local inteterupt requests. Interrupts from external devices are transmitted to this device on LINT1 and LINT2. Each local interrupt signal activates the request from one of two interrupt request level. An external device generates an interrupt request by driving the appropriate interrupt request pin to its active (low) state. The signal should remain low until the device recognizes it. These signals can be applied asynchronously to the device as they are synchronized internally before use.

RESET	I	System reset. During normal operation, RESET is driven low to reset the device. When RESET is asserted low, the device's internal registers are set to an initial known state and all output and bidirectional pins are driven either to inactive levels or to a high-impedance state. The device's behavior following reset depends on the level of the HCS input just before the low-to-high transition of RESET. If HCS is low, the device begins executing the instructions pointed to by the reset vector. If HCS is high, the device is halted until a host processor writes a 0 to the HLT bit in the HSTCTLL register.
		POWER
V_{CC} 1/	I	Nominal 5-volt power supply inputs. 5 pins on QFP; 9 pins on PGA.
V_{SS} 1/	I	Electrical ground inputs. 9 pins on QFP; 17 pins on PGA.
EMU0-2	I	Emulation pins 0-2.
EMU3	0	Emulation pin 3.
		MULTIPROCESSOR INTERFACE
GI	I	Bus grant input. External bus arbitration logic drives GI low to enable the device to gain access to the local-memory bus. The device must release the bus if GI is high so that another device can access the bus.
R1, R0	0	Bus request and control. These two signals indicate a request for use of the bus in a multiprocessor system; they are decoded as shown below:

R1	R0	Bus request type
L	L	High-priority bus request
L	H	Bus cycle termination
H	L	Low priority bus request
H	H	No bus request pending

A high-priority bus request provides for VRAM serial-data-register transfer cycles (midline or blanked), DRAM refresh (when 12 or more refresh cycles are pending), or a host-initiated access. The external arbitration logic should grant the request as soon as possible by asserting GI low.

A low-priority bus request is used to provide for CPU-requested access and DRAM refresh (when less than 12 refresh cycles are pending).

Bus cycle termination status is provided so that the arbitration logic can determine that the device currently accessing the bus is completing an access and other devices may compete for the next bus cycle. A no bus request pending status is output when the currently active device does not require the bus on subsequent cycles.

VIDEO INTERFACE

CBLNK/VBLNK	0	Composite blanking/vertical blanking. This signal can be programmed to select one of two blanking functions: Composite blanking for blanking the display during both horizontal and vertical retrace in composite-sync video mode. Vertical blanking for blanking the display during vertical retrace in separate-sync-video mode. Immediately following reset, this signal is configured as a CBLNK output.

1/ For proper device operation, all V_{CC} and V_{SS} pins must be connected externally.

CSYNC/HBLNK I/O Composite sync/horizontal blanking. This signal can be programmed to select one of two functions:

Composite sync (either input or output as set by a control bit in the DPYCTL register) in composite-sync video mode:

Input: Extracts HSYNC and VSYNC from externally generated horizontal sync pulses.

Output: Generates active-low composite-sync pulses from either externally generated HSYNC and VSYNC signals or signals generated by the device's on-chip video timers.

Horizontal blank (output only) for blanking the display during horizontal retrace in separate-sync-video mode.

Immediately following reset, this signal is configured as a CSYNC input.

HSYNC I/O Horizontal sync. HSYNC is the horizontal sync signal that controls external video circuitry. This signal can be programmed to be either an input or an output by modifying a control bit in the DPYCTL register.

As an output, HSYNC is the active-low horizontal sync signal generated by the device's on-chip video timers.

As an input, HSYNC synchronizes the devices's video-control registers to externally generated horizontal sync pulses. The actual synchronization can be programmed to begin at any VCLK cycle; this allows for any external pipelining of signals.

Immediately following reset, HSYNC is configured as an input.

SCLK I Serial data clock. This signal is the same as the signal that drives VRAM serial data registers. This allow the device to track the VRAM serial data register count, providing serial register transfer and midline reload cycles. (SCLK may be asynchronous to VCLK; however, it typically has a frequency that is a multiple of the VCLK frequency).

VCLK I Video clock. This clock is derived from a multiple of the video system's dotclock and is used internally to drive the video timing logic.

VSYNC I/O Vertical sync. VSYNC is the vertical sync signal that controls external video circuitry. This signal can be programmed to be either an input or an output by modifying a control bit in the DPYCTL register.

As an output, VSYNC is the active-low vertical sync signal generated by the device's on-chip video timers.

As an input, VSYNC synchronizes the devices's video-control registers to externally generated vertical sync pulses. The actual synchronization can be programmed to begin at any horizontal line; this allows for any external pipelining of signals.

Immediately following reset, VSYNC is configured as an input.

6.6 One part - one part number system. The one part - one part number system described below has been developed to allow for transitions between identical generic devices covered by the three major microcircuit requirements documents (MIL-H-38534, MIL-I-38535, and 1.2.1 of MIL-STD-883) without the necessity for the generation of unique PIN's. The three military requirements documents represent different class levels, and previously when a device manufacturer upgraded military product from one class level to another, the benefits of the upgraded product were unavailable to the Original Equipment Manufacturer (OEM), that was contractually locked into the original unique PIN. By establishing a one part number system covering all three documents, the OEM can acquire to the highest class level available for a given generic device to meet system needs without modifying the original contract parts selection criteria.

Military documentation format	Example PIN under new system	Manufacturing source listing	Document listing
New MIL-H-38534 Standardized Military Drawings	5962-XXXXXZZ(H or K)YY	QML-38534	MIL-BUL-103
New MIL-I-38535 Standardized Military Drawings	5962-XXXXXZZ(Q or V)YY	QML-38535	MIL-BUL-103
New 1.2.1 of MIL-STD-883 Standardized Military Drawings	5962-XXXXXZZ(M)YY	MIL-BUL-103	MIL-BUL-103

6.7 Sources of supply.

6.7.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DESC-EC and have agreed to this drawing.

6.7.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-EC.

1/ For proper device operation, all V_{CC} and V_{SS} pins must be connected externally.