

REVISIONS

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PMIC N/A				PREPARED BY Larry T. Gauder				DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444																									
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				SIZE A	CAGE CODE 67268				5962-91738																								
				SHEET	1	OF				15																							

DESC FORM 193
JUL 91

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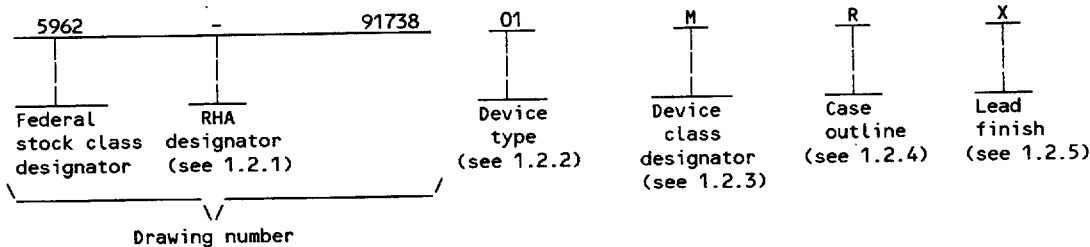
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1. SCOPE

1.1 Scope. This drawing forms a part of a one part - one part number documentation system (see 6.6 herein). Two product assurance classes consisting of military high reliability (device classes Q, and M) and space application (device class V), and a choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). Device class M microcircuits represent non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices". When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:



1.2.1 RHA designator. Device classes M RHA marked devices shall meet the MIL-I-38535 appendix A specified RHA levels and shall be marked with the appropriate RHA designator. Device classes Q and V RHA marked devices shall meet the MIL-I-38535 specified RHA levels and shall be marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	54F573	Octal D-type transparent latches

1.2.3 Device class designator. The device class designator shall be a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883
Q or V	Certification and qualification to MIL-I-38535

1.2.4 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
R	GDIP1-T20 or CDIP2-T20	20	dual-in-line package
S	GDFP2-F20 or CDFP3-F20	20	flat package
2	CQCC1-N20	20	square chip carrier package

1.2.5 Lead finish. The lead finish shall be as specified in MIL-STD-883 (see 3.1 herein) for class M or MIL-I-38535 for classes Q and V. Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-91738
		REVISION LEVEL	SHEET 2

1.3 Absolute maximum ratings. 1/

Supply voltage range (V_{CC})	- - - - -	-0.5 V dc to +7.0 V dc
Input voltage range (V_{IN})	- - - - -	-0.5 V dc to +7.0 V dc
Output current (I_{OUT})	- - - - -	40 mA
Storage temperature range	- - - - -	-65°C to +150°C
Lead temperature (soldering, 10 seconds)	- - - - -	+300°C
Junction temperature (T_J)	- - - - -	+175°C
Maximum power dissipation (P_D): 2/	- - - - -	302.5 mW
Thermal resistance, junction-to-case (Θ_{JC})	- - - - -	See MIL-STD-1835

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	- - - - -	4.5 V dc to 5.5 V dc
High level input voltage (V_{IH})	- - - - -	2.0 V
Low level input voltage (V_{IL})	- - - - -	0.8 V
Maximum input clamp current, (I_{IK})	- - - - -	-18 mA
Maximum high level output current, (I_{OH})	- - - - -	-3 mA
Maximum low level output current, (I_{OL})	- - - - -	20 mA
Input rise and fall times, (t_r , t_f)	- - - - -	2.5 ns
Case operating temperature range (T_C)	- - - - -	-55°C to +125°C

1.5 Digital logic testing for device classes Q and V.

Fault coverage measurement of manufacturing
logic tests (MIL-STD-883, test method 5012) - - - - - 3/ percent

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, bulletin, and handbook. Unless otherwise specified, the following specification, standards, bulletin, and handbook of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-I-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Microcircuit Case Outlines.

- 1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ Maximum power dissipation is defined as $V_{CC} \times I_{CC}$ and must withstand the added P_D due to the short circuit output test, e.g., I_{OS} .
3/ Values will be added when they become available.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-91738
		REVISION LEVEL	SHEET 3

DESC FORM 193A
JUL 91

■ 9004708 0004432 304 ■

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

HANDBOOK

MILITARY

MIL-HDBK-780 - Standardized Military Drawings.

(Copies of the specification, standards, bulletin, and handbook required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device class M shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein. The individual item requirements for device classes Q and V shall be in accordance with MIL-I-38535, the device manufacturer's Quality Management (QM) plan, and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-STD-883 (see 3.1 herein) for device class M and MIL-I-38535 for device classes Q and V herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.4 Logic diagram. The logic diagram shall be as specified on figure 3.

3.2.5 Test circuit and switching waveforms. The test circuit and switching waveforms shall be as specified on figure 4.

3.2.6 Radiation exposure circuit. The radiation exposure circuit shall be as specified when available.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. Marking for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein). In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103. Marking for device classes Q and V shall be in accordance with MIL-I-38535.

3.5.1 Certification/compliance mark. The compliance mark for device class M shall be a "C" as required in MIL-STD-883 (see 3.1 herein). The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-I-38535.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-91738
		REVISION LEVEL	SHEET 4

DESC FORM 193A
JUL 91

9004708 0004433 240

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions -55°C ≤ T _C ≤ +125°C unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
High level output voltage	V _{OH}	V _{CC} = 4.5 V V _{IH} = 2.0 V V _{IL} = 0.8 V	1, 2, 3	2.4		V
				2.5		
Low level output voltage	V _{OL}	V _{CC} = 4.5 V V _{IH} = 2.0 V V _{IL} = 0.8 V I _{OL} = 20 mA	1, 2, 3		0.5	V
Off-state output current, High level voltage applied	I _{OZH}	V _{CC} = 5.5 V V _{OUT} = 2.7 V	1, 2, 3		50	μA
Off-state output current, Low level voltage applied	I _{OZL}	V _{CC} = 5.5 V V _{OUT} = 0.5 V	1, 2, 3		-50	
Input clamp voltage	V _{IK}	V _{CC} = 4.5 V I _I = -18 mA	1, 2, 3		-1.2	V
Input current at maximum input voltage	I _I	V _{CC} = 5.5 V V _{IN} = 7.0 V	1, 2, 3		100	μA
High level input current	I _{IH}	V _{CC} = 5.5 V V _I = 2.7 V	1, 2, 3		20	μA
Low level input current	I _{IL}	V _{CC} = 5.5 V V _I = 0.5 V	1, 2, 3		-0.6	mA
Short circuit output current	I _{OS}	V _{CC} = 5.5 V V _{OUT} = 0.0 V	1, 2, 3	-60	-150	mA
Supply current	I _{CCZ}	V _{CC} = 5.5 V OE = 4.5 V D = E = GND	1, 2, 3		60	mA
Functional test		See 4.4.1b V _{CC} = 4.5 V and 5.5 V	7, 8			

See footnote at end of table.

STANDARDIZED
MILITARY DRAWING
DEFENSE ELECTRONICS SUPPLY CENTER
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SIZE
A

5962-91738

REVISION LEVEL

SHEET
5

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions -55°C ≤ T _C ≤ +125°C unless otherwise specified	Group A subgroups	Limits		Unit
				Min	Max	
Propagation delay latch enable to output	t _{PLH1}	V _{CC} = 5.0 V C _L = 50 pF R _L = 500Ω See figure 4.	9	3.0	11.5	ns
			10,11	3.7	13.5	
	t _{PHL1}		9	2.2	7.0	ns
			10, 11	1.5	9.0	
Propagation delay data to output	t _{PLH2}		9	2.0	8.0	ns
			10, 11	1.5	9.0	
	t _{PHL2}		9	1.2	6.0	ns
			10, 11	1.0	8.0	
Enable time to high level	t _{PZH}		9	1.2	11.0	ns
			10, 11	1.0	13.0	
Enable time to low level	t _{PZL}		9	1.2	8.5	
			10, 11	1.0	10.0	
Disable time from high level	t _{PHZ}		9	1.2	6.5	
			10, 11	1.0	8.5	
Disable time from low level	t _{PLZ}		9	1.2	6.0	
			10, 11	1.0	7.0	
Latch enable pulse width <u>2</u> /	t _w (H)		9, 10, 11	6.0		ns
Set up time, data to latch enable ↓ <u>2</u> /	t _s		9, 10, 11	2.0		
Hold time, data to latch enable ↓ <u>2</u> /	t _h		9, 10, 11	5.0		

1/ Not more than one output should be shorted at a time. For testing I_{OS}, the use of high speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.

2/ Guaranteed, if not tested to the limits specified in table I, herein.

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MILITARY DRAWING
DEFENSE ELECTRONICS SUPPLY CENTER
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SIZE
A

5962-91738

REVISION LEVEL

SHEET
6

Device type	01
Case outline	R, S, and 2
Terminal number	Terminal symbol
1	\overline{OE}
2	D ₀
3	D ₁
4	D ₂
5	D ₃
6	D ₄
7	D ₅
8	D ₆
9	D ₇
10	GND
11	E
12	Q ₇
13	Q ₆
14	Q ₅
15	Q ₄
16	Q ₃
17	Q ₂
18	Q ₂
19	Q ₀
20	V _{CC}

FIGURE 1. Terminal connections.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-91738
		REVISION LEVEL	SHEET 7

DESC FORM 193A
JUL 91

■ 9004708 0004436 T5T ■

Inputs			Outputs
\overline{OE}	E	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

H = High voltage level.

L = Low voltage level.

Z = High impedance.

X = Irrelevant.

Q_0 = Level of Q before the indicated steady state input conditions were established.

FIGURE 2. Truth table.

STANDARDIZED
MILITARY DRAWING
DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

SIZE
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5962-91738

REVISION LEVEL

SHEET
8

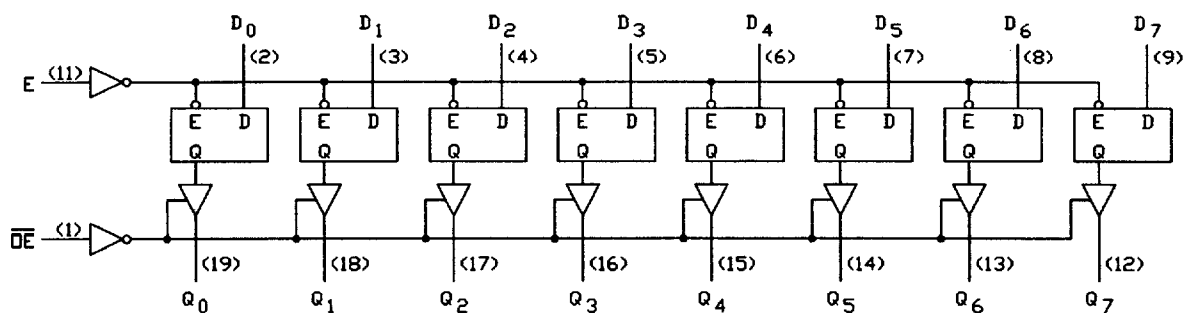


FIGURE 3. Logic diagram.

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SIZE
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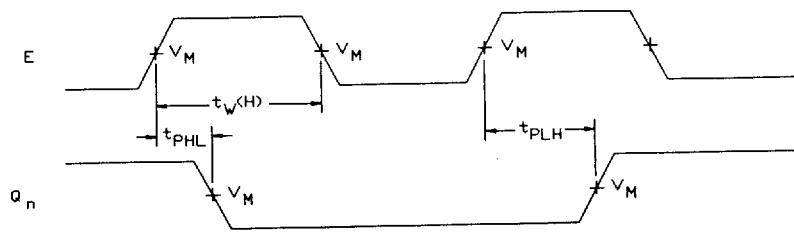
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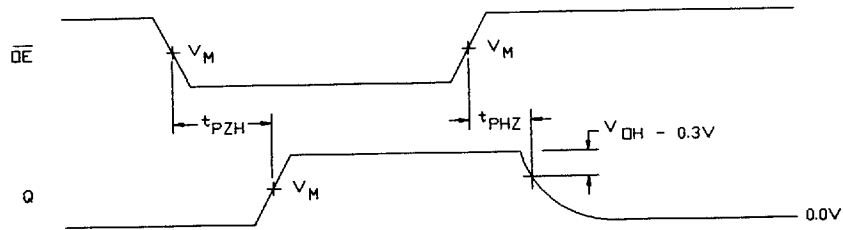
SHEET
9

DESC FORM 193A
JUL 91

9004708 0004438 822



LATCH ENABLE TO OUTPUT DELAYS AND
LATCH ENABLE PULSE WIDTH



3-STATE OUTPUT ENABLE TIME TO HIGH LEVEL
AND OUTPUT DISABLE TIME FROM HIGH LEVEL

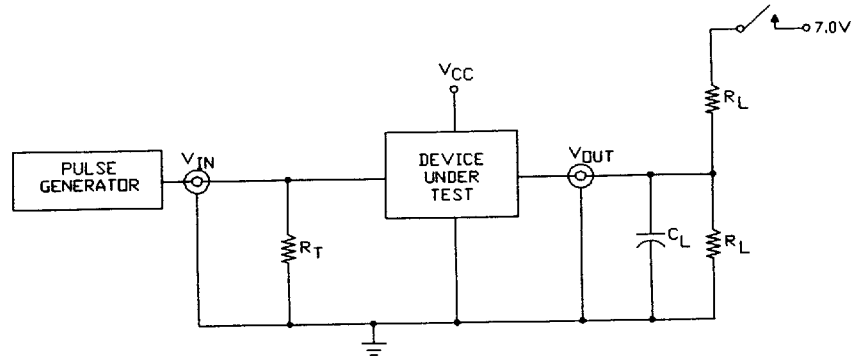


FIGURE 4. Test circuit and switching waveforms.

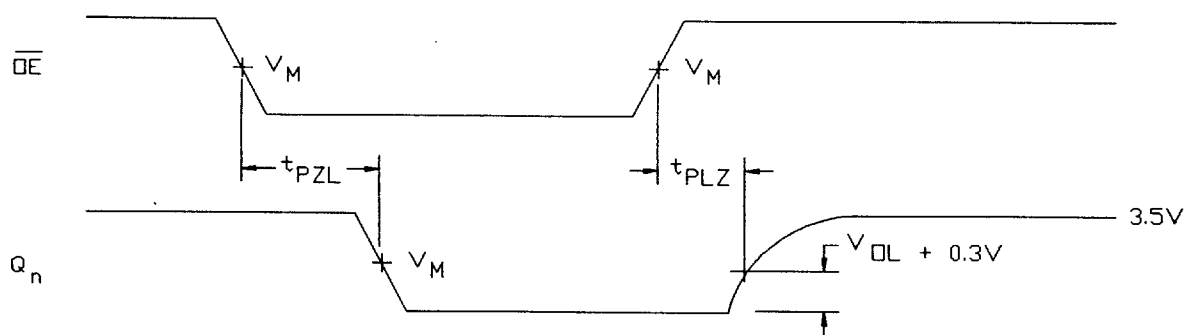
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MILITARY DRAWING
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DAYTON, OHIO 45444

SIZE
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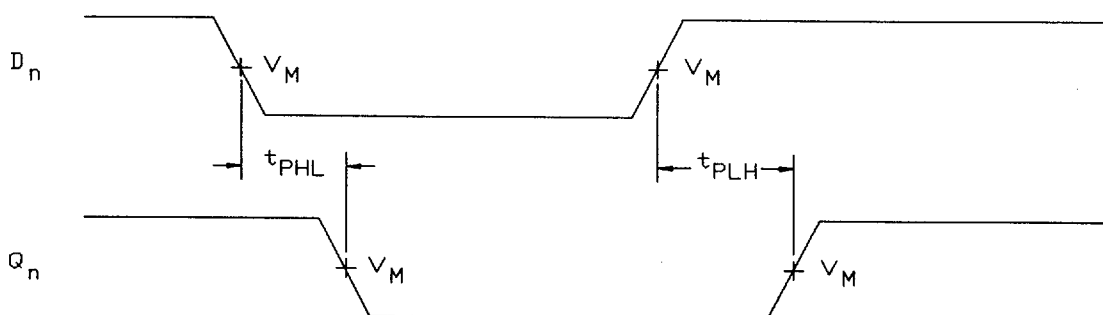
5962-91738

REVISION LEVEL

SHEET
10



3-STATE OUTPUT ENABLE TIME TO LOW LEVEL
AND OUTPUT DISABLE TIME FROM LOW LEVEL



PROPAGATION DELAY DATA TO Q OUTPUTS

NOTES:

1. Pulse generator characteristics:
PRR = 1 MHz, $t_r = t_f \leq 2.5$ ns duty cycle = 50 percent.
2. $C_L = 50$ pF.
3. $R_L = 500\Omega$.
4. C_L includes probe and jig capacitance.
5. R_T = Termination resistance should be equal to Z_{OUT} of pulse generator.
6. $V_M = 1.5$ V

FIGURE 4. Test circuit and switching waveforms - Continued.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-91738
		REVISION LEVEL	SHEET 11

DESC FORM 193A
JUL 91

9004708 0004440 480

3.6 Certificate of compliance. For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.7.2 herein). For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.7.1 herein). The certificate of compliance submitted to DESC-EC prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device class M, the requirements of MIL-STD-883 (see 3.1 herein), or for device classes Q and V, the requirements of MIL-I-38535 and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required for device class M in MIL-STD-883 (see 3.1 herein) or for device classes Q and V in MIL-I-38535 shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DESC-EC of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-973.

3.9 Verification and review for device class M. For device class M, DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 30 (see MIL-I-38535, appendix A).

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device class M, sampling and inspection procedures shall be in accordance with MIL-STD-883 (see 3.1 herein). For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-I-38535 and the device manufacturer's QM plan.

4.2 Screening. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. For device classes Q and V, screening shall be in accordance with MIL-I-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(2) $T_A = +125^{\circ}\text{C}$, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except that interim electrical tests prior to burn-in are optional at the discretion of the manufacturer.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-I-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in appendix B of MIL-I-38535.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-91738
		REVISION LEVEL	SHEET 12

DESC FORM 193A
JUL 91

9004708 0004441 317

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-I-38535. Inspections to be performed shall be those specified in MIL-I-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Quality conformance inspection for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein) and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4). Technology conformance inspection for classes Q and V shall be in accordance with MIL-I-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-I-38535 permits alternate in-line control testing.

4.4.1 Group A inspection.

- a. Tests shall be as specified in table II herein.
- b. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

- a. Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.
- b. $T_A = +125^{\circ}\text{C}$, minimum.
- c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-I-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes Q, and V shall be M, D, R, and H and for device class M shall be M and D.

- a. End-point electrical parameters shall be as specified in table II herein.
- b. For device class M the devices shall be subjected to radiation hardness assured tests as specified in MIL-I-38535, appendix A, for the RHA level being tested. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-I-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at $T_A = +25^{\circ}\text{C} \pm 5^{\circ}\text{C}$, after exposure, to the subgroups specified in table II herein.
- c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-STD-883 (see 3.1 herein) for device class M and MIL-I-38535 for device classes Q and V.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-91738
		REVISION LEVEL	SHEET 13

DESC FORM 193A
JUL 91

9004708 0004442 253

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, TM 5005, table I)	Subgroups (in accordance with MIL-I-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1	1	1
Final electrical parameters (see 4.2)	1,2,3,7, 8,9,10,11 1/	1,2,3,7, 8,9,10,11 1/	1,2,3,7, 8,9,10,11 2/
Group A test requirements (see 4.4)	1,2,3,7, 8,9,10,11	1,2,3,7, 8,9,10,11	1,2,3,7, 8,9,10,11
Group C end-point electrical parameters (see 4.4)	1,2,3,	1,2,3, 7,8	1,2,3, 7,8
Group D end-point electrical parameters (see 4.4)	1,2,3,	1,2,3, 7,8	1,2,3, 7,8
Group E end-point electrical parameters (see 4.4)		1,7,9	1,7,9

1/ PDA applies to subgroup 1.

2/ PDA applies to subgroups 1 and 7.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and which SMD's are applicable to that system. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DESC-EC, telephone (513) 296-6047.

6.4 Comments. Comments on this drawing should be directed to DESC-EC, Dayton, Ohio 45444-5270, or telephone (513) 296-8525.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-I-38535 and MIL-STD-1331.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-91738
		REVISION LEVEL	SHEET 14

6.6 One part - one part number system. The one part - one part number system described below has been developed to allow for transitions between identical generic devices covered by the three major microcircuit requirements documents (MIL-H-38534, MIL-I-38535, and 1.2.1 of MIL-STD-883) without the necessity for the generation of unique PIN's. The three military requirements documents represent different class levels, and previously when a device manufacturer upgraded military product from one class level to another, the benefits of the upgraded product were unavailable to the Original Equipment Manufacturer (OEM), that was contractually locked into the original unique PIN. By establishing a one part number system covering all three documents, the OEM can acquire to the highest class level available for a given generic device to meet system needs without modifying the original contract parts selection criteria.

<u>Military documentation format</u>	<u>Example PIN under new system</u>	<u>Manufacturing source listing</u>	<u>Document listing</u>
New MIL-H-38534 Standardized Military Drawings	5962-XXXXXXZ(H or K)YY	QML-38534	MIL-BUL-103
New MIL-I-38535 Standardized Military Drawings	5962-XXXXXXZ(Q or V)YY	QML-38535	MIL-BUL-103
New 1.2.1 of MIL-STD-883 Standardized Military Drawings	5962-XXXXXXZ(M)YY	MIL-BUL-103	MIL-BUL-103

6.7 Sources of supply.

6.7.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DESC-EC and have agreed to this drawing.

6.7.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-EC.

STANDARDIZED MILITARY DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-91738
		REVISION LEVEL	SHEET 15

DESC FORM 193A
JUL 91

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