REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																			
SHEET																			
REV																			
SHEET	15	16	17	18	19	20	21	22											

REV STATUS OF SHEETS	REV														
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

STANDARDIZED MILITARY DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

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DRAWING APPROVAL DATE
93-03-26

REVISION LEVEL

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, MEMORY, DIGITAL, CMOS 2K x 16-BIT STATE MACHINE UVEPROM, MONOLITHIC SILICON

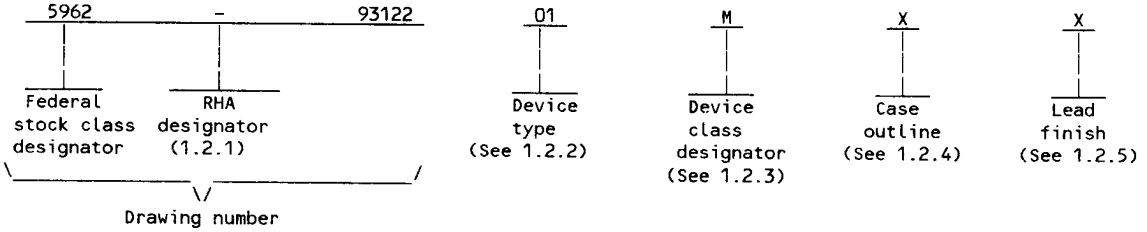
SIZE	CAGE CODE	5962-93122
A	67268	

SHEET 1 OF 22

1. SCOPE

1.1 Scope. This drawing forms a part of a one part - one part number documentation system (see 6.6 herein). Two product assurance classes consisting of military high reliability (device classes B, Q, and M) and space application (device classes S and V) and a choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). Device class M microcircuits represent non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices". When available, a choice of radiation hardness assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:



1.2.1 Radiation hardness assurance (RHA) designator. Device classes M, B, and S RHA marked devices shall meet the MIL-M-38510 specified RHA levels and shall be marked with the appropriate RHA designator. Device classes Q and V RHA marked devices shall meet the MIL-I-38535 specified RHA levels and shall be marked with the appropriate RHA designator A dash (-) indicates a non-RHA device.

1.2.2 Device types. The device types shall identify the circuit function as follows:

Device type	Generic number 1/	Circuit function	Access Time
01		2K x 16-bit State Machine UV EPROM	15 ns
02		2K x 16-bit State Machine UV EPROM	12 ns
03		2K x 16-bit State Machine UV EPROM	15 ns
04		2K x 16-bit State Machine UV EPROM	12 ns

1.2.3 Device class designator. The device class designator shall be a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883
B or S	Certification and qualification to MIL-M-38510
Q or V	Certification and qualification to MIL-I-38535

1.2.4 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835, and as follows:

Outline letter	Descriptive designator	Terminals	Package style 2/
X	CDIP3-T28 or GDIP4-T28	28	Dual-in line
Y	GQCC1-J28	28	"J" Lead chip carrier
Z	GQCC1-J44	44	"J" Lead chip carrier
U	CQCC1-N44	44	Square leadless chip carrier
3	CQCC1-N28	28	Square leadless chip carrier

1/ Generic numbers are listed on the Standardized Military Drawing Source Approval Bulletin and will also be listed in MIL-BUL-103.
2/ Lid shall be transparent to permit ultraviolet light erasure.

1.2.5 Lead finish. The lead finish shall be as specified in MIL-M-38510 for classes M, B, and S or MIL-I-38535 for classes Q and V. Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference.

1.3 Absolute maximum ratings. 3/

Supply voltage range to ground potential (V_{CC})	-0.5 V dc to +7.0 V dc
DC voltage applied to the outputs in the high Z state	-0.5 V dc to +7.0 V dc
DC input voltage	-3.0 V dc to +7.0 V dc
Maximum power dissipation	1.0 W 4/
Lead temperature (soldering, 10 seconds)	+260°C
Thermal resistance, junction-to-case (Θ_{JC})	See MIL-STD-1835
Junction temperature (T_J)	+175°C
Storage temperature range	-65°C to +150°C
Temperature under bias	-55°C to +125°C
Endurance	25 cycles/byte, minimum
Data retention	10 years, minimum

1.4 Recommended operating conditions.

Supply voltage (V_{CC})	+4.5 V dc minimum to +5.5 V dc maximum
Ground voltage (GND)	0 V dc
Input high voltage (V_{IH})	2.0 V dc to 6.0 V dc
Input low voltage (V_{IL})	-3.0 V dc to 0.8 V dc 5/
Case operating temperature range (T_C)	-55°C to +125°C

1.5 Logic testing for device classes Q or V.

Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012)	xx percent 6/

2. APPLICABLE DOCUMENTS

2.1 Government specifications, standards, bulletin, and handbook. Unless otherwise specified, the following specifications, standards, bulletin, and handbook of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATIONS

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.
MIL-I-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

MILITARY

MIL-STD-480 - Configuration Control-Engineering Changes, Deviations and Waivers.
MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-1835 - Microcircuit Case Outlines.

3/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
4/ Must withstand the added P_D due to short circuit test (e.g., I_{OS}).
5/ Negative undershoots of -5.0 V dc are allowed with a pulse width < 10 ns.
6/ When a Qualified Manufacturers' List (QML) source exists, a value will be provided.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

HANDBOOK

MILITARY

MIL-HDBK-780 - Standardized Military Drawings.

(Copies of the specifications, standards, bulletin, and handbook required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Non-Government publications. The following documents form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents which are DoD adopted are those listed in the issue of the DODISS cited in the solicitation. Unless otherwise specified, the issues of documents not listed in the DODISS are the issues of the documents cited in the solicitation.

AMERICAN SOCIETY FOR TESTING AND MATERIALS (ASTM)

ASTM Standard F1192-88 - Standard Guide for the Measurement of Single Event Phenomena from Heavy Ion Irradiation of Semiconductor Devices.

(Applications for copies of ASTM publications should be addressed to the American Society for Testing and Materials, 1916 Race Street, Philadelphia, Pennsylvania 19103).

ELECTRONICS INDUSTRIES ASSOCIATION (EIA)

JEDEC Standard No. 17 - A Standardized Test Procedure for the characterization of LATCH-UP in CMOS Integrated Circuits.

(Applications for copies should be addressed to the Electronics Industries Association, 2001 Pennsylvania Street, N.W., Washington, DC 20006.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device class M shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein. The individual item requirements for device classes B and S shall be in accordance with MIL-M-38510 and as specified herein. For device classes B and S, a full electrical characterization table for each device type shall be included in this SMD. The individual item requirements for device classes Q and V shall be in accordance with MIL-I-38535, the device manufacturer's Quality Management (QM) plan, and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 for device classes M, B, and S and MIL-I-38535 for device classes Q and V and herein.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth tables. The truth tables shall be as specified on figure 2.

3.2.3.1 Unprogrammed devices. The truth table for unprogrammed devices for contracts involving no altered item drawing shall be as specified on figure 2. When required in screening (see 4.2 herein), or qualification conformance inspection groups A, B, C, or D (see 4.4 herein), the devices shall be programmed by the manufacturer prior to test. A minimum of 50 percent of the total number of bits shall be programmed or at least 25 percent of the total number of bits to any altered item drawing.

3.2.3.2 Programmed devices. The truth table for programmed devices shall be as specified by an attached altered item drawing.

3.3 Electrical performance characteristics and post irradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and post irradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. Marking for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein). In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103. Marking for device classes B and S shall be in accordance with MIL-M-38510. Marking for device classes Q and V shall be in accordance with MIL-I-38535.

3.5.1 Certification/compliance mark. The compliance mark for device class M shall be a "C" as required in MIL-STD-883 (see 3.1 herein). The certification mark for device classes B and S shall be a "J" or "JAN" as required in MIL-M-38510. The certification mark for device classes Q and V shall be a "QML" as required in MIL-I-38535.

3.6 Certificate of compliance. For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.7.3 herein). For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.7.2 herein). The certificate of compliance submitted to DESC-ECS prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device class M, the requirements of MIL-STD-883 (see 3.1 herein), or for device classes Q and V, the requirements of MIL-I-38535 and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required for device class M in MIL-STD-883 (see 3.1 herein) or device classes B and S in MIL-M-38510 or for device classes Q and V in MIL-I-38535 shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M notification to DESC-ECC of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-480.

3.9 Verification and review for device class M. For device class M, DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device classes M, B, and S. Device classes M, B, and S devices covered by this drawing shall be in microcircuit group number 42 (see MIL-M-38510, appendix E).

3.10.1 Processing options. Since the device is capable of being programmed by either the manufacturer or the user to result in a wide variety of configurations, two processing options are provided for selection in the contract using an altered item drawing.

3.10.2 Unprogrammed device delivered to the user. All testing shall be verified through group A testing as defined in 3.2.3.1 and table IIA. It is recommended that users perform subgroups 7 and 9 after programming to verify the specific program configuration.

3.10.3 Manufacturer-programmed device delivered to the user. All testing requirements and quality assurance provisions herein, including the requirements of the altered item drawing, shall be satisfied by the manufacturer prior to delivery.

3.11 Erasure of EPROMS. When specified, devices shall be erased in accordance with the procedures and characteristics specified in 4.5 herein.

3.12 Verification of erasure or programmed EPROMs. When specified, devices shall be verified as either programmed to the specified pattern or erased. As a minimum, verification shall consist of performing a functional test (subgroup 7) to verify that all bits are in the proper state. Any bit that does not verify to be in the proper state shall constitute a device failure, and shall be removed from the lot.

3.13 Endurance. A reprogrammability test shall be completed as part of the vendors reliability monitors, this reprogrammability test shall be done only for initial characterization and after any design or process changes which may affect the reprogrammability of the device. This test shall consist of 25 program/erase cycles on 25 devices with the following conditions:

(1) All devices selected for testing shall be programmed per 3.2.3.2 herein (see 4.6).

(2) Verify pattern (see 3.12).

(3) Erase (see 3.11).

(4) Verify pattern erasure (see 3.12).

3.14 Serialization for device class S and V. All device class S devices shall be serialized in accordance with MIL-M-38510. Class V shall be serialized in accordance with MIL-I-38535.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device class M, sampling and inspection procedures shall be in accordance with section 4 of MIL-M-38510 to the extent specified in MIL-STD-883 (see 3.1 herein). For device classes B and S, sampling and inspection procedures shall be in accordance with MIL-M-38510 and method 5005 of MIL-STD-883, except as modified herein. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-I-38535 and the device manufacturer's QM plan.

4.2 Screening. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. For device classes B and S, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to qualification and quality conformance inspection. For device classes Q and V, screening shall be in accordance with MIL-I-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes M, B, and S.

a. Delete the sequence specified as initial (pre-burn-in) electrical parameters through interim (post-burn-in) electrical parameters of method 5004 and substitute lines 1 through 6 of table IIA herein.

b. Prior to burn-in, the devices shall be programmed (see 4.6 herein) with a checkerboard pattern or equivalent (manufacturers at their option may employ an equivalent pattern provided it is a topologically true alternating bit pattern). The pattern shall be read before and after burn-in. Devices having bits not in the proper state after burn-in shall constitute a device failure and shall be included in the Percent Defective Allowable (PDA) calculation and shall be removed from the lot (see 4.2.3 herein).

c. For device class M, the burn-in test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or qualifying activity upon request. For device classes B and S, the test circuit shall be submitted to the qualifying activity. For device classes M, B, and S, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(1) Static burn-in for device class S (method 1015 of MIL-STD-883, test condition A).

(a) All inputs shall be connected to GND. Outputs may be open or connected to 4.5 V minimum. Resistors R1 are optional on both inputs and outputs, and required on outputs connected to V_{CC} ±0.5 V. R1 = 220 ohms to 47 kohms. For static II burn-in, reverse all input connections (i.e. V_{SS} to V_{CC}).

(b) V_{CC} = 4.5 V minimum.

(c) Ambient temperature (T_A) shall be +125°C minimum.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device types	Limit		Unit
					Min	Max	
Output high voltage	V_{OH}	V_{CC} = 4.5 V, I_{OH} = -2.0 mA V_{IN} = V_{IH}, V_{IL}	1,2,3	All	2.4		V
Output low voltage	V_{OL}	V_{CC} = 4.5 V, I_{OL} = 6.0 mA V_{IN} = V_{IH}, V_{IL}	1,2,3	All		0.4	V
Input high voltage 1/	V_{IH}		1,2,3	All	2.0		V
Input low voltage 1/	V_{IL}		1,2,3	All		0.8	V
Input leakage current	I_{IX}	V_{CC} = 5.5 V V_{IN} = V_{CC} to GND	1,2,3	All	-10	+10	µA
Output leakage current	I_{OZ}	V_{CC} = 5.5 V V_{OUT} = V_{CC} to GND	1,2,3	All	-40	+40	µA
Output short circuit current 2/ 3/	I_{OS}	V_{CC} = 5.5 V, V_{OUT} = GND	1,2,3	All	-20	-90	mA
Power supply current	I_{CC}	V_{CC} = 5.5 V, I_{OUT} = 0 mA 4/	1,2,3	All		90	mA
Input capacitance 3/	C_{IN}	V_{CC} = 5.0 V, V_{IN} = 0 V, T_A = 25°C, f = 1 MHz, (see 4.4.1e)	4	All		10	pF
Output capacitance 3/	C_{OUT}	V_{CC} = 5.0 V, V_{OUT} = 0 V, T_A = 25°C, f = 1 MHz (see 4.4.1e)	4	All		10	pF
Functional tests		See 4.4.1c	7,8A,8B	All			
Clock period	t_{CP}	See figures 3 and 4 and 5/	9,10,11	01,03	15		ns
				02,04	12		

See footnotes at end of table.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limit		Unit
					Min	Max	
Clock high	t_{CH}	See figures 3 and 4 and note 5/	9,10,11	01,03	6.5		ns
				02,04	5		
Clock low	t_{CL}		9,10,11	01,03	6.5		ns
				02,04	5		
Address setup to CLK 6/	t_{AS}		9,10,11	01,03	4 or 8		ns
				02,04	3 or 7		
Address hold from CLK 3/ 6/	t_{AH}		9,10,11	01,03	4 or 1		ns
				02,04	3 or 0		
Address setup to CLK with input bypassed	t_{ABS}		9,10,11	01,03	15		ns
				02,04	12		
Address hold from CLK with input bypassed 3/	t_{ABH}		9,10,11	All	0		ns
Chip select setup to CLK 6/	t_{CSS}		9,10,11	01,03	4 or 8		ns
				02,04	3 or 7		
Chip select hold from CLK 6/	t_{CSH}		9,10,11	01,03	4 or 1		ns
				02,04	3 or 0		
Asynchronous $\overline{INIT}$ to output valid with output bypassed	t_{IPD}		9,10,11	01,03		25	ns
				02,04		21	
Output CLK to registered output valid	t_{CKO1}		9,10,11	01,03		11	ns
				02,04		9	
Output CLK to output valid with output bypassed	t_{CKO2}		9,10,11	01,03		21	ns
				02,04		18	
Data hold from CLK	t_{DH}		9,10,11	All	2		ns
CLK to output valid	t_{COV}		9,10,11	01,03		11	ns
				02,04		9	

See footnotes at end of table.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limit		Unit
					Min	Max	
CLK to high Z output 3/ 7/	t_{COZ}	See figures 3 and 4 and note 5/	9,10,11	01,03		11	ns
				02,04		9	
CS to output valid with input bypassed	t_{CSV}		9,10,11	01,03		15	ns
				02,04		12	
CS to high Z output with input bypassed 3/ 7/	t_{CSZ}		9,10,11	01,03		15	ns
				02,04		12	
$\overline{OE}$ to output valid	t_{OEV}		9,10,11	01,03		11	ns
				02,04		9	
$\overline{OE}$ to high Z output 3/ 7/	t_{OEZ}		9,10,11	01,03		11	ns
				02,04		9	
$\overline{INIT}$ setup to CLK 6/	t_{IS}		9,10,11	01,03	4 or 8		ns
				02,04	3 or 7		
$\overline{INIT}$ hold from CLK 6/	t_{IH}		9,10,11	01,03	4 or 1		ns
				02,04	3 or 0		
$\overline{INIT}$ setup to CLK with input bypassed	t_{IBS}		9,10,11	01,03	15		ns
				02,04	12		
$\overline{INIT}$ hold from CLK with input bypassed	t_{IBH}		9,10,11	All	0		ns
Propagation delay with input and output bypassed	t_{PD}		9,10,11	01,03		21	ns
				02,04		18	
CLK to output valid with output bypassed	t_{ICO}		9,10,11	01,03		21	ns
				02,04		18	

See footnotes at end of table.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A subgroups	Device type	Limit		Unit
					Min	Max	
Asynchronous $\overline{INIT}$ pulse width	t_{IW}	See figures 3 and 4 and note 5/	9,10,11	01,03	15		ns
				02,04	12		
Asynchronous $\overline{INIT}$ to data valid	t_{IDV}		9,10,11	01,03		15	ns
				02,04		12	
Asynchronous $\overline{INIT}$ recovery to clock	t_{ICR}		9,10,11	01,03	15		ns
				02,04	12		

1/ These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
2/ For test purposes, not more than one output at a time should be shorted. Short circuit test duration should not exceed one second.
3/ Tested initially and after any design or process changes that affect that parameter, and therefore shall be guaranteed to the limits specified in table I.
4/ Add 1mA/MHz for AC power component.
5/ AC tests are performed with input rise and fall times of 3 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V, and the output load in figure 3, Circuit A, unless otherwise noted.
6/ The device can be programmed to have either a 3 ns setup and 3 ns hold time or a 7 ns setup and 0 ns hold time for devices 02,04 on the chip select, address, and $\overline{INIT}$ inputs. Devices 01,03 have either a 4 ns setup and 4 ns hold time or a 8 ns setup and 1 ns hold time.
7/ See figure 3, Circuit B, for waveform and output load.

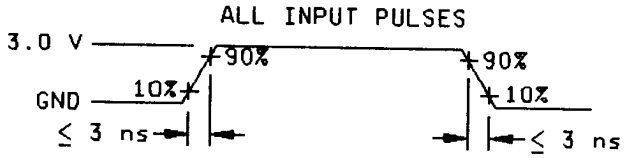
Device Types	01, 02	03, 04
Case Outlines	X,Y,3	U,Z
Terminal Number	Terminal Symbol	
1	$\overline{INIT}$	V_{SS}
2	A_0	$\overline{INIT}$
3	A_1	CS
4	A_2	$\overline{OE}$
5	A_3	A_0
6	A_4	A_1
7	V_{CC}	A_2
8	V_{SS}	V_{CC}
9	A_5	A_3
10	A_6	A_4
11	A_7	V_{CC}
12	A_8	V_{SS}
13	A_9	A_5
14	A_{10}	V_{SS}
15	D_7	A_6
16	D_6	A_7
17	D_5	A_8
18	D_4	A_9
19	D_3	A_{10}
20	V_{SS}	V_{CC}
21	V_{CC}	D_{15}
22	V_{SS}	V_{CC}
23	D_2	D_{14}
24	D_1	D_{13}
25	D_0	D_{12}
26	CLK	D_{11}
27	CS	D_{10}
28	$\overline{OE}$	V_{SS}
29	---	V_{SS}
30	---	V_{CC}
31	---	D_9
32	---	D_8
33	---	D_7
34	---	D_6
35	---	V_{CC}
36	---	V_{SS}
37	---	D_5
38	---	D_4
39	---	D_3
40	---	D_2
41	---	D_1
42	---	D_0
43	---	V_{SS}
44	---	CLK

Figure 1. Terminal connections.

$\overline{INIT}$	$\overline{OE}$	CS	CLK	A_0-A_{10}	OUTPUTS
X	X	X	X	X	HIGH Z

X = Don't care
Z = High impedance state

Figure 2. Truth tables (unprogrammed).

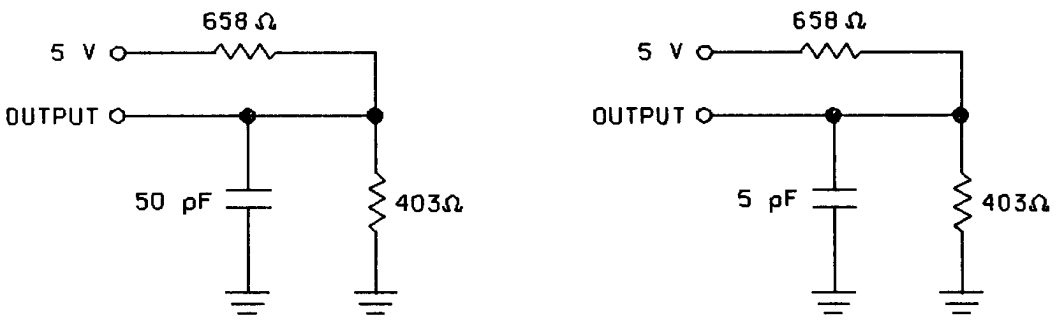


AC test conditions

Input pulse levels	GND to 3.0 V
Input rise and fall levels	≤ 3 ns
Input timing reference levels	1.5 V
Output reference levels	1.5 V

Figure 3. Output load circuit and test conditions.

Output load circuit



Circuit A
Output Load

Circuit B (High Z)
Output Load

NOTE: Including scope and jig. (minimum values)

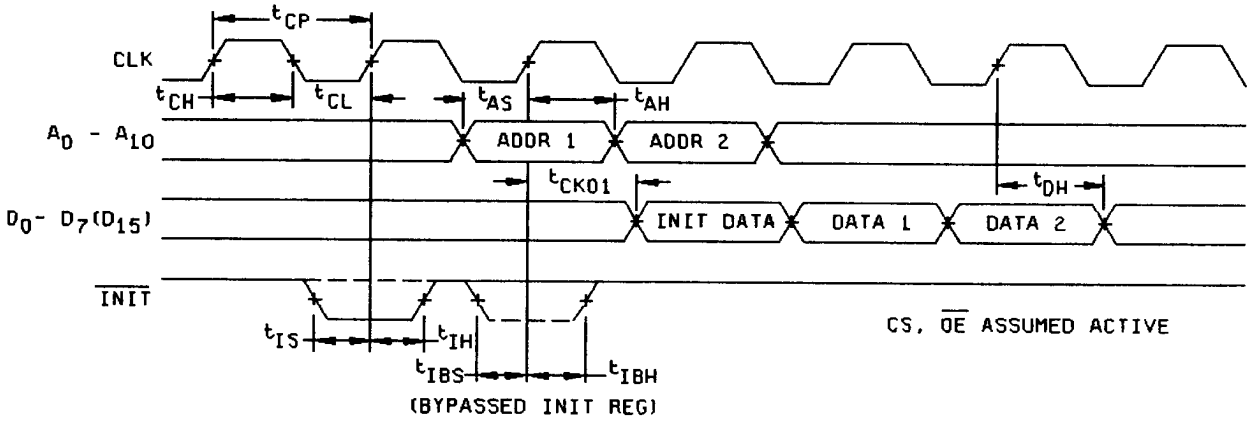
Output waveform measurement level

HIGH Z OUTPUT	0.5 V, V_{OH}, C_L = 5 pF; V_X = 0.0 V	R_{th} PIN — V_X
HIGH Z OUTPUT	0.5 V, V_{OL}, C_L = 5 pF; V_X = 2.6 V	R_{th} PIN — V_X
OUTPUT ENABLE	V_X = 0.0 V, 1.5 V, V_{OH}, C_L = 50 pF	333Ω PIN — V_X
OUTPUT ENABLE	V_X = 2.6 V, 1.5 V, V_{OL}, C_L = 50 pF	500Ω PIN — V_X

Note: R_{th} = Thevenin Equivalent.

Figure 3. Output load circuit and test conditions - continued.

Registered input and output (combined with $\overline{INIT}$)



Bypassed address and $\overline{INIT}$ registers

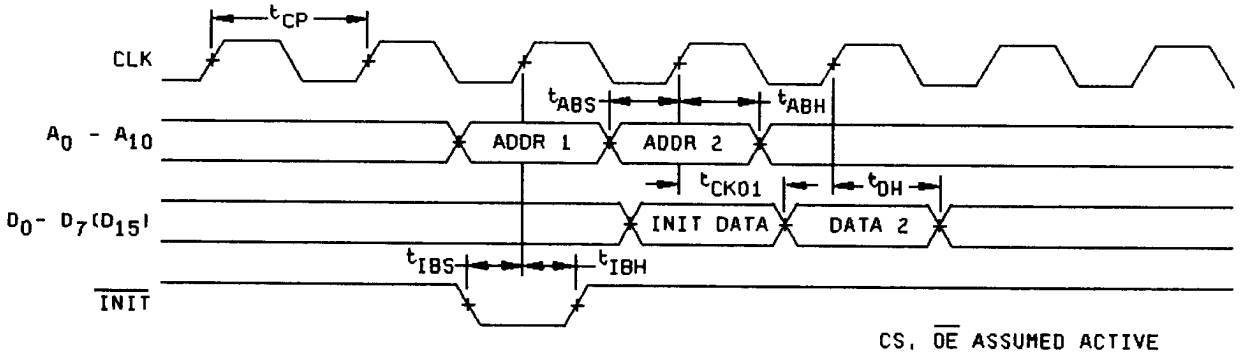
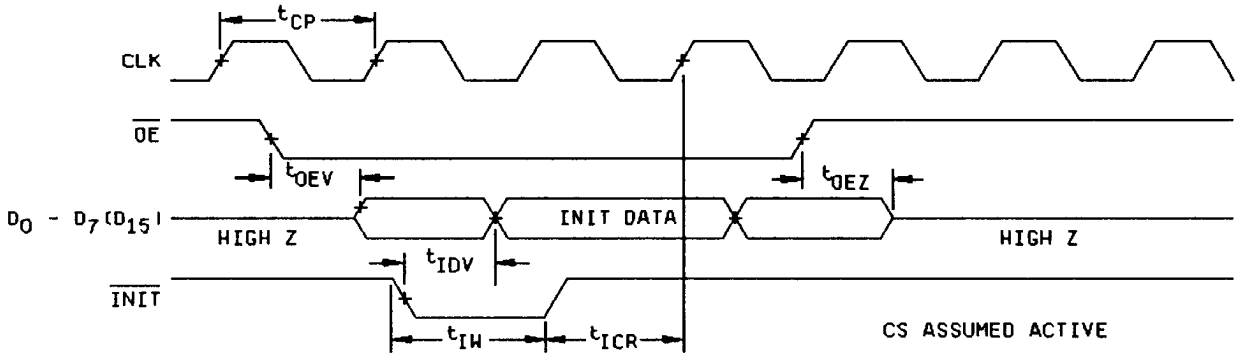


FIGURE 4. Switching waveforms.

Asynchronous $\overline{INIT}$ and $\overline{OE}$



Single and double-registered chip select

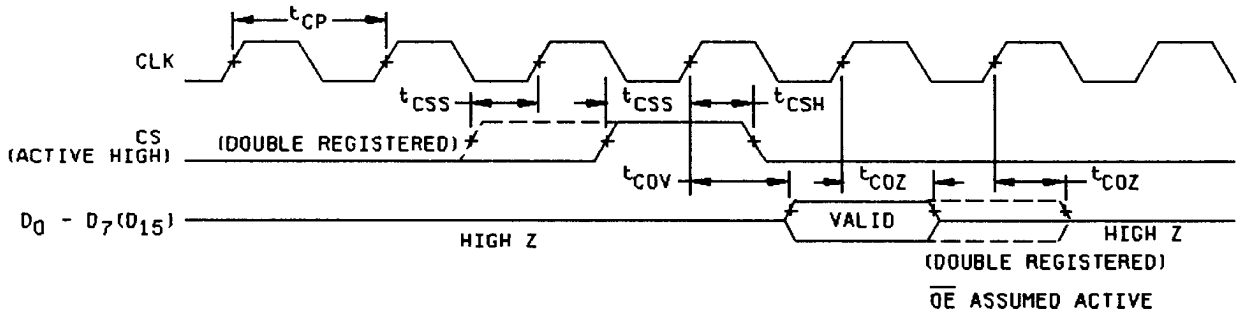
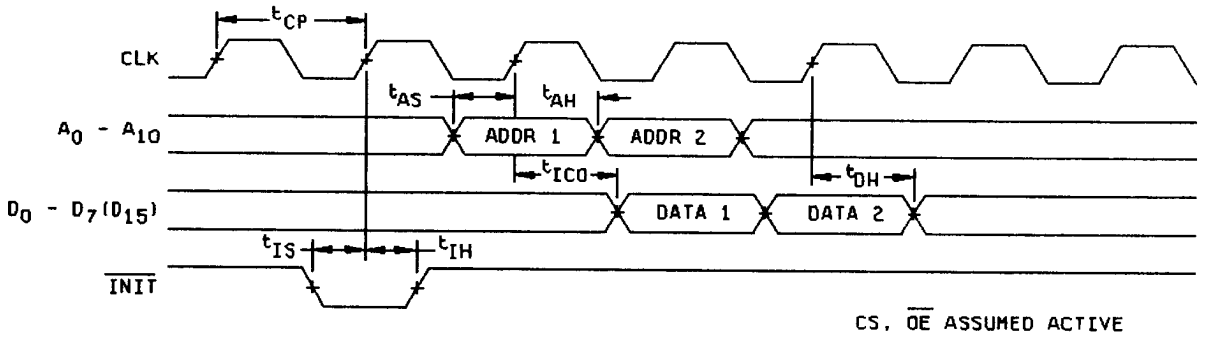
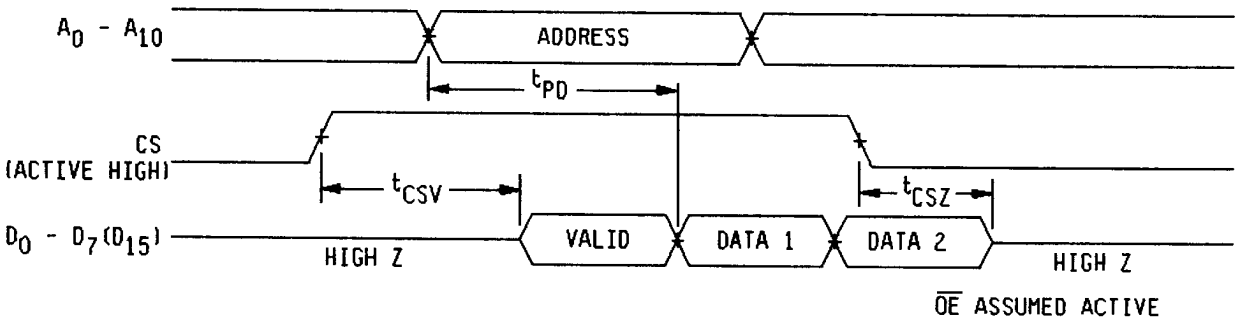


FIGURE 4. Switching waveforms - continued.

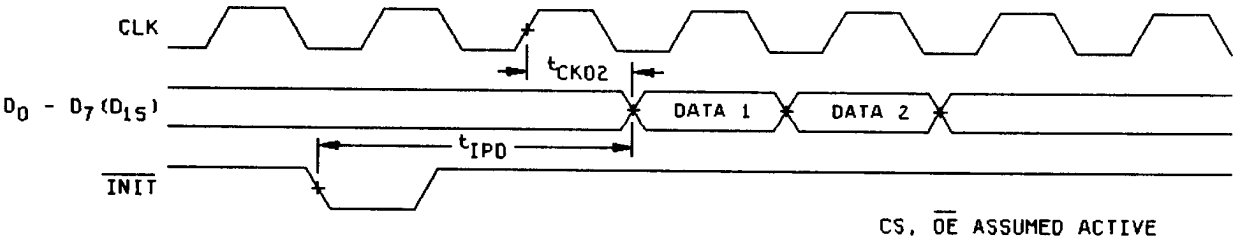
Bypassed output register 1/



Bypassed input and output register (CS and address)



Asynchronous $\overline{INIT}$ and bypassed output register 2/



1/ Even though the register is bypassed, $\overline{INIT}$ continues to set the output register (for the feedback purposes).
2/ Output registers configured as feedback to the array and bypassed with respect to the output.

FIGURE 4. Switching waveforms - continued.

(d) Test duration for the static test shall be 48 hours minimum. The 48 hour burn-in shall be broken into two sequences of 24 hours each (Static I and Static II) followed by interim electrical measurements.

(2) Dynamic burn-in for device classes M, B, and S (method 1015 of MIL-STD-883, test condition D; for circuit, see 4.2.1c herein).

d. Interim and final electrical parameters shall be as specified in table IIA herein.

e. For class S and B devices, post dynamic burn-in electrical parameter measurements may, at the manufacturer's option, be performed separately or included in the final electrical parameter requirements.

f. A data retention stress test shall be included as part of the screening procedure and shall consist of the following steps: (Steps 1 through 4 may be performed at the wafer level. The maximum storage temperature shall not exceed +200°C for packaged devices or +300°C for unassembled devices.)

Margin test method.

(1) Program at +25°C greater than 95 percent of the bit locations, including the slowest programming bit. The remaining bits shall provide a worst case speed pattern.
(2) Bake, unbiased, for 72 hours at +140°C or for 32 hours at +150°C or for 8 hours at +200°C or for 2 hours at +300°C for unassembled devices only.
(3) Perform margin test using Vm = +5.55 V at +25°C using loose timing (i.e., t_{AS} = 1μs).
(4) Erase (see 3.11).
(5) Program at +25°C with a 50 percent pattern (checkerboard or equivalent).
(6) Perform margin test using Vm = +5.75 V and Vm = +4.40 V at +25°C with loose timing.
(7) Perform dynamic burn-in in accordance with 4.2.1c(2).
(8) Perform electrical tests at T_C = +25°C, including margin test at Vm = +5.55 V and loose timing (i.e., t_{AS} = 2μs).
(9) Perform electrical tests at T_C = -55°C, including margin test at Vm = +5.55 V and loose timing (See (8)).
(10) Perform electrical tests at T_C = +125°C, including margin test at Vm = +5.55 V and loose timing (See (8)).
(11) Erase (see 3.11), except devices submitted for groups A, B, C, and D testing.
(12) Verify erasure (see 3.12).

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition, and test temperature or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-I-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in appendix B of MIL-I-38535.

4.2.3 Percent defective allowable (PDA).

a. The PDA for class S devices shall be 5 percent for static burn-in and 5 percent for dynamic burn-in, based on the exact number of devices submitted to each separate burn-in.

b. The PDA for class B devices shall be in accordance with MIL-M-38510 for dynamic burn-in.

c. Static burn-in I and II failures shall be cumulative for determining PDA.

d. Those devices whose measured characteristics, after burn-in, exceed the specified delta limits or electrical parameter limits specified in table I, subgroup 1, are defective and shall be removed from the lot. The verified failures divided by the total number of devices in the lot initially submitted to burn-in shall be used to determine the percent defective for the lot and the lot shall be accepted or rejected based on the specified PDA.

e. The PDA for device classes Q and V shall be in accordance with MIL-I-38535 for dynamic burn-in.

4.3 Qualification inspection.

4.3.1 Qualification inspection for device classes B and S. Qualification inspection for device classes B and S shall be in accordance with MIL-M-38510. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5). Qualification data for subgroups 7, 8A, and 8B shall be attributes only.

4.3.1.1 Qualification extension for device class B and S. When authorized by the qualifying activity, if a manufacturer qualifies one device type which is identical (i.e., same die), to other device types on this drawing, the slower device types many be part I qualified, upon the request of the manufacturer, without any further testing. The faster device types may be part I qualified by performing only group A qualification testing.

4.3.2 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-I-38535. Inspections to be performed shall be those specified in MIL-I-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5).

4.4 Conformance inspection. Quality conformance inspection for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein) and as specified herein. Quality conformance inspection for device classes B and S shall be in accordance with MIL-M-38510 and as specified herein. Inspections to be performed for device classes M, B, and S shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.5). Technology conformance inspection for classes Q and V shall be in accordance with MIL-I-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-I-38535 permits alternate in-line control testing.

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 5 and 6 of table I method 5005 of MIL-STD-883 shall be omitted.

c. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table. For device classes B and S, subgroups 7 and 8 tests shall be sufficient to verify the truth table as approved by the qualifying activity. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device, these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).

d. O/V (latch-up) tests shall be measured only for initial qualification and after any design or process changes which may affect the performance of the device. For device class M procedures and circuits shall be maintained under document revision level control by the manufacturer and shall be made available to the preparing activity or acquiring activity upon request. For device classes B and S, the procedures and circuits shall be maintained under document revision control by the manufacturer and shall be made available to the qualifying activity upon request. For device classes Q and V, procedures and circuits shall be under the control of the device manufacturer's technical review board (TRB) in accordance with MIL-I-38535 and shall be made available to the preparing activity or acquiring activity upon request. Testing shall be on all pins, on five devices with zero failures. Latch-up test shall be considered destructive. Information contained in JEDEC Standard number 17 may be used for reference.

e. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for initial qualification and after any process or design changes which may affect input or output capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency of 1 MHz. Sample size is 15 devices with no failures, and all input and output terminals tested.

f. All devices selected for testing shall be programmed with a checkerboard pattern or equivalent. After completion of all testing, the devices shall be erased and verified, (except devices submitted for groups B, C, and D testing).

4.4.2 Group B inspection. The group B inspection end-point electrical parameters shall be as specified in table IIA herein. For device class S steady-state life tests, the test circuit shall be submitted to the qualifying activity.

a. For device class S, steady-state life test circuits shall be conducted using test condition D and the circuit described in 4.2.1c herein, or equivalent as approved by the qualifying activity.

b. For device class S only, end-point electrical parameters shall be as specified in table IIA herein. Delta limits shall apply only to subgroup 5 of group B inspections and shall consist of tests specified in table IIB herein.

c. All devices selected for class S electrical testing shall be programmed with a checkerboard pattern or equivalent. After completion of all testing the devices shall be erased and verified, (except devices submitted to group C and D).

4.4.3 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein. Delta limits shall apply only to subgroup 1 of group C inspections and shall consist of tests specified in table IIB herein.

4.4.3.1 Additional criteria for device classes M and B. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. The devices selected for testing shall be programmed with a checkerboard pattern. After completion of all testing, the devices shall be erased and verified (except devices submitted for group D testing).

b. Test condition D. For device class M, the test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. For device class B, the test circuit shall be submitted to the qualifying activity. For device classes M and B, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

c. T_A = +125°C, minimum.

d. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.3.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition, and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-I-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

4.4.4 Group D inspection. For group D inspection, end-point electrical parameters shall be as specified in table IIA herein. The devices selected for testing shall be programmed with a checkerboard pattern. After completion of all testing, the devices shall be erased and verified.

4.4.5 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes B, S, Q, and V shall be M, D, R, and H and for device class M shall be M and D.

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes M, B, and S, the devices shall be subjected to radiation hardness assured tests as specified in MIL-M-38510 for the RHA level being tested. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-I-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I as T_A = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

c. When specified in the purchase order or contract, a copy of the RHA limits shall be supplied.

4.5 Erasing procedure. The recommended erasure procedure for the device is exposure to shortwave ultraviolet light which has a wavelength of 2537 angstroms (Å). The integrated dose (i.e., UV intensity x exposure time) for erasure should be a minimum of 25 Ws/cm^2. The erasure time with this dosage is approximately 35 minutes using a ultraviolet lamp with a 12,000 $\mu W/cm^2$ power rating. The device should be placed within one inch of the lamp tubes during erasure. The maximum integrated dose the device can be exposed to without damage is 7258 Ws/cm^2 (1 week at 12,000 $\mu W/cm^2$). Exposure of EPROMs to high intensity UV light for long periods may cause permanent damage.

4.6 Programming procedure. The programming procedures shall be as specified by the device manufacturer and shall be made available upon request.

TABLE IIA. Electrical test requirements. 1/ 2/ 3/ 4/ 5/ 6/ 7/

Line no.	Test requirements	Subgroups (per method 5005, table I)			Subgroups (per MIL-I-38535, table III)	
		Device class M	Device class B	Device class S	Device class Q	Device class V
1	Interim electrical parameters (see 4.2)		1,7,9 or 2,8A,10	1,7,9 or 2,8A,10		1,7,9 or 2,8A,10
2	Static burn-in (method 1015)	Not required	Not required	Required	Not required	Required
3	Same as line 1			1*,7* Δ 8/		1*,7* Δ 8/
4	Dynamic burn-in (method 1015)	Required	Required	Required	Required	Required
5	Same as line 1			1*,7* Δ 8/		1*,7* Δ8/
6	Final electrical test parameters (programmed devices)	1*,2,3, 7*,8A,8B, 9,10,11	1*,2,3, 7*,8A,8B, 9,10,11	1*,2,3, 7*,8A,8B, 9,10,11	1*,2,3, 7*,8A,8B, 9,10,11	1*,2,3, 7*,8A,8B, 9,10,11
7	Group A test requirements	1,2,3,4**, 7,8A,8B,9, 10,11	1,2,3,4**, 7,8A,8B,9, 10,11	1,2,3,4**, 7,8A,8B,9, 10,11	1,2,3,4**, 7,8A,8B,9, 10,11	1,2,3,4**, 7,8A,8B,9, 10,11
8	Group B end-point electrical parameters			1,2,3,7, 8A,8B,9, 10,11 Δ		
9	Group C end-point electrical parameters	2,3,7, 8A,8B	1,2,3,7, 8A,8B Δ		1,2,3,7, 8A,8B Δ	1,2,3,7, 8A,8B,9, 10,11 Δ
10	Group D end-point electrical parameters	2,3, 8A,8B	2,3, 8A,8B	2,3, 8A,8B	2,3, 8A,8B	2,3, 8A,8B
11	Group E end-point electrical parameters	1,7,9	1,7,9	1,7,9	1,7,9	1,7,9

1/ Blank spaces indicate tests are not applicable.
2/ Any or all subgroups may be combined when using high-speed testers.
3/ Subgroups 7 and 8 functional tests shall verify the truth table.
4/ * indicates PDA applies to subgroup 1 and 7.
5/ ** see 4.4.1e.
6/ Δ indicates delta limit shall be required where specified, and the delta values shall be computed with reference to the previous electrical parameters.
7/ See 4.7.
8/ See 4.4.1d.

TABLE IIB. Delta limits at +25°C.

Parameter 1/	Device types
	All
I_{IX}	±10 percent of specified value in table I
I_{OZ}	±10 percent of specified value in table I

1/ The above parameter shall be recorded before and after the required burn-in and life tests to determine the delta.

4.7 Delta measurements for device classes B, S, Q, and V. Delta measurements, as specified in table IIA, shall be made and recorded before and after the required burn-in screens and steady-state life tests to determine delta compliance. The electrical parameters to be measured, with associated delta limits are listed in table IIB. The device manufacturer may, at his option, either perform delta measurements or within 24 hours after burn-in perform final electrical parameter tests, subgroups 1, 7, and 9.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510 for device classes M, B, and S and MIL-I-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device classes B and Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-481 using DD Form 1693, Engineering Change Proposal (Short Form).

6.3 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and which SMD's are applicable to that system. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DESC-EC, telephone (513) 296-6047.

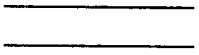
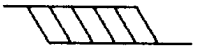
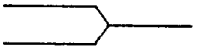
6.4 Comments. Comments on this drawing should be directed to DESC-EC, Dayton, Ohio 45444, or telephone (513) 296-5377.

6.5 Symbols, definitions, and functional descriptions.

C_{IN} . . . . . Input terminal capacitance.
C_{OUT} . . . . . Output terminal capacitance.
I_{CC} . . . . . Supply current.
I_{IX} . . . . . Input current.
I_{OZ} . . . . . Output current.
T_C . . . . . Case temperature.
V_{CC} . . . . . Positive supply voltage (5.0 V).
V_{SS} . . . . . Ground zero voltage potential.

6.5.1 Timing limits. The table of timing values shows either a minumum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

6.5.2 Waveforms.

WAVEFORM SYMBOL	INPUT	OUTPUT
	MUST BE VALID	WILL BE VALID
	CHANGE FROM H TO L	WIIL CHANGE FROM H TO L
	CHANGE FROM L TO H	WILL CHANGE FROM L TO H
	DON'T CARE ANY CHANGE PERMITTED	CHANGING STATE UNKNOWN
		HIGH IMPEDANCE

6.6 One part - one part number system. The one part - one part number system described below has been developed to allow for transitions between identical generic devices covered by the four major microcircuit requirements documents (MIL-M-38510, MIL-H-38534, MIL-I-38535, and 1.2.1 of MIL-STD-883) without the necessity for the generation of unique PIN's. The four military requirements documents represent different class levels, and previously when a device manufacturer upgraded military product from one class level to another, the benefits of the upgraded product were unavailable to the Original Equipment Manufacturer (OEM), who was contractually locked into the original unique PIN. By establishing a one part number system covering all four documents, the OEM can procure to the highest class level available for a given generic device to meet system needs without modifying the original contract parts selection criteria.

Military documentation format	Example PIN under new system	Manufacturing source listing	Document listing
New MIL-M-38510 Military Detail Specifications (in the SMD format)	5962-XXXXXZZ(B or S)YY	QPL-38510 (Part 1 or 2)	MIL-BUL-103
New MIL-H-38534 Standardized Military Drawings	5962-XXXXXZZ(H or K)YY	QML-38534	MIL-BUL-103
New MIL-I-38535 Standardized Military Drawings	5962-XXXXXZZ(Q or V)YY	QML-38535	MIL-BUL-103
New 1.2.1 of MIL-STD-883 Standardized Military Drawings	5962-XXXXXZZ(M)YY	MIL-BUL-103	MIL-BUL-103

6.7 Sources of supply.

6.7.1 Sources of supply for device classes B and S. Sources of supply for device classes B and S are listed in QPL-38510.

6.7.2 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DESC-EC and have agreed to this drawing.

6.7.3 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-EC.