REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Updated boilerplate. Added device types 04 - 07 to drawing. - glg	99-08-02	Raymond Monnin

REV																			
SHEET																			
REV	A	A	A	A	A	A	A	A											
SHEET	15	16	17	18	19	20	21	22											

REV STATUS OF SHEETS															
REV	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

PMIC N/A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY
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DRAWING APPROVAL DATE
94-10-25

REVISION LEVEL
A

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43216-5000

MICROCIRCUIT, MEMORY, DIGITAL, CMOS,
32K x 9 FIFO, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	67268	5962-93152

SHEET 1 OF 22

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:

5962	-	93152	01	Q	X	X
Federal stock class designator	RHA designator (see 1.2.1)		Device type (see 1.2.2)	Device class designator (see 1.2.3)	Case outline (see 1.2.4)	Lead finish (see 1.2.5)

Drawing number

1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number 1/	Circuit function	Access time
01	7C464	32K X 9 cascadable FIFO	40 ns
02	7C464	32K X 9 cascadable FIFO	25 ns
03	7C464	32K X 9 cascadable FIFO	20 ns
04	7C464A 2/	32K X 9 cascadable FIFO	40 ns
05	7C464A 2/	32K X 9 cascadable FIFO	25 ns
06	7C464A 2/	32K X 9 cascadable FIFO	20 ns
07	7C464A 2/	32K X 9 cascadable FIFO	15 ns

1.2.3 Device class designator. The device class designator shall be a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	GDIP1-T28 or CDIP2-T28	28	Dual-in-line
Y	CQCC1-N32	32	Rectangular leadless chip carrier

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1/ Generic numbers are also listed on the Standard Microcircuit Drawing Source Approval Bulletin at the end of this document and will also be listed in MIL-HDBK-103 and QML-38535 (see 6.6.2 herein).
2/ Based on the most recent die revision, these new device types are readily cascadable with similar product from other vendors. They are not however, cascadable with previous device types (01-03).

1.3 Absolute maximum ratings. 3/

Supply voltage range to ground potential (V_{CC})	-0.5 V dc to +7.0 V dc
DC voltage range applied to outputs in high-Z state	-0.5 V dc to +7.0 V dc
DC input voltage range (V_{IN})	-3.0 V dc to +7.0 V dc
DC output current	20 mA
Maximum power dissipation	1.0 W
Lead temperature (soldering, 10 seconds)	+260EC
Thermal resistance, junction-to-case (2_{JC})	See MIL-STD-1835
Junction temperature (T_J)	+175EC
Storage temperature range (T_{STG})	-65EC to +150EC
Temperature under bias range	-55EC to +125EC

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	+4.5 V dc minimum to +5.5 V dc maximum
Ground voltage (GND)	0 V dc
Input high voltage (V_{IH})	2.2 V dc minimum
Input low voltage (V_{IL})	0.8 V dc maximum
Case operating temperature range (T_C)	-55EC to +125EC

1.5 Digital logic testing for device classes Q and V.

Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012)	100 percent

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, bulletin, and handbook. Unless otherwise specified, the following specification, standards, bulletin, and handbook of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Interface Standard for Microcircuit Case Outlines.

HANDBOOKS

DEPARTMENT OF DEFENSE

MIL-HDBK-103 - List of Standard Microcircuit Drawings (SMD's).
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

3/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issue of the documents which are DoD adopted are those listed in the issue of the DODISS cited in the solicitation. Unless otherwise specified, the issues of documents not listed in the DODISS are the issues of the documents cited in the solicitation.

AMERICAN SOCIETY FOR TESTING AND MATERIALS (ASTM)

ASTM Standard F1192-88 - Standard Guide for the Measurement of Single Event Phenomena from Heavy Ion Irradiation of Semiconductor Devices.

(Applications for copies of ASTM publications should be addressed to the American Society for Testing and Materials, 1916 Race Street, Philadelphia, PA 19103).

ELECTRONICS INDUSTRIES ASSOCIATION (EIA)

JEDEC Standard EIA/JESD78 - IC Latch-Up Test.

(Applications for copies should be addressed to the Electronics Industries Association, 2500 Wilson Blvd., Arlington, VA 22201).

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.4 Die overcoat. Polyimide and silicone coatings are allowable as an overcoat on the die for alpha particle protection only. Each coated microcircuit inspection lot (see inspection lot as defined in MIL-PRF-38535) shall be subjected to and pass the internal moisture content test at 5000 ppm (see method 1018 of MIL-STD-883). The frequency of the internal water vapor testing shall not be decreased unless approved by the preparing activity for class M. The TRB will ascertain the requirements as provided by MIL-PRF-38535 for classes Q and V. Samples may be pulled any time after seal.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-973.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 105 (see MIL-PRF-38535, appendix A).

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Delete the sequence specified as initial (preburn-in) electrical parameters through interim (postburn-in) electrical parameters of method 5004 and substitute lines 1 through 6 of table IIA herein.

b. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(1) Dynamic burn-in (method 1015 of MIL-STD-883, test condition D) using the circuit referenced (see 4.2.1b herein).

c. Interim and final electrical parameters shall be as specified in table IIA herein.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ -55EC # T_C # +125EC 4.5 V # V_{CC} # 5.5 V unless otherwise specified	Group A subgroups	Device types	Limits Min	Limits Max	Unit
Output high voltage	V_{OH}	V_{CC} = 4.5 V, I_{OH} = -2.0 mA V_{IN} = V_{IH}, V_{IL}	1, 2, 3	All	2.4		V
Output low voltage	V_{OL}	V_{CC} = 4.5 V, I_{OL} = 8.0 mA V_{IN} = V_{IH}, V_{IL}	1, 2, 3	All		0.4	V
Input high voltage 2/	V_{IH}		1, 2, 3	All	2.2		V
Input low voltage 2/	V_{IL}		1, 2, 3	All		0.8	V
Input leakage current	I_{IX}	V_{IN} = 5.5 V to GND	1, 2, 3	All	-10	10	µA
Output leakage current	I_{OZ}	V_{CC} = 5.5 V, R = V_{IH}, V_{OUT} = 5.5 V and GND	1, 2, 3	All	-10	10	µA
Operating supply current	I_{CC1}	V_{CC} = 5.5 V, I_{OUT} = 0 mA f = $1/t_{RC}$	1, 2, 3	01		75	mA
				02		95	
				03		110	
				04		75	
		V_{CC} = 5.5 V, I_{OUT} = 0 mA f = 20 MHz	1, 2, 3	05		95	
				06		110	
				07		60	
Standby current	I_{CC2}	V_{CC} = 5.5 V, I_{OUT} = 0 mA All inputs = V_{IH} Min.	1, 2, 3	01-03		30	mA
				04-07		12	
Power down current	I_{CC3}	V_{CC} = 5.5 V, I_{OUT} = 0 mA All inputs = V_{CC} -0.2 V	1, 2, 3	01-03		25	mA
				04-07		8	
3/ Input capacitance	C_{IN}	V_{CC} = 5.0 V, V_{IN} = 0 V T_A = +25EC, f = 1 MHz See 4.4.1e	4	All		10	pF
3/ Output capacitance	C_{OUT}	V_{CC} = 5.0 V, V_{OUT} = 0 V T_A = +25EC, f = 1 MHz See 4.4.1e	4	All		12	pF
Functional tests		See 4.4.1c	7,8A,8B	All			

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ -55EC # T_C # +125EC 4.5 V # V_{CC} # 5.5 V unless otherwise specified	Group A subgroups	Device types	Limits Min	Limits Max	Unit
Read cycle time	t_{RC}	See figure 3	9, 10, 11	01,04	50		ns
				02,05	35		
				03,06	30		
				07	25		
Access time	t_A		9, 10, 11	01,04		40	ns
				02,05		25	
				03,06		20	
				07		15	
Read recovery time	t_{RR}		9, 10, 11	All	10		ns
Read low to low-Z 3/ 4/	t_{LZR}		9, 10, 11	All	3		ns
Read high to data valid	t_{DVR}		9, 10, 11	All	3		ns
Read high to high-Z 3/ 4/	t_{HZR}		9, 10, 11	01,04		25	ns
				02,05		18	
				03,06,07		15	
Read pulse width 5/	t_{PR}		9, 10, 11	01,04	40		ns
				02,05	25		
				03,06	20		
				07	15		
Write cycle time	t_{WC}		9, 10, 11	01,04	50		ns
				02,05	35		
				03,06	30		
				07	25		
Write pulse width 5/	t_{PW}		9, 10, 11	01,04	40		ns
				02,05	25		
				03,06	20		
				07	15		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ -55EC # T_C # +125EC 4.5 V # V_{CC} # 5.5 V unless otherwise specified	Group A subgroups	Device types	Limits Min	Limits Max	Unit
Write high to low-Z 3/ 4/ 6/	t_{HWZ}	See figure 3	9, 10, 11	All	5		ns
Write recovery time	t_{WR}		9, 10, 11	All	10		ns
Data setup time	t_{SD}		9, 10, 11	01,04	20		ns
				02,05	15		
				03,06	12		
				07	9		
Data hold time	t_{HD}		9, 10, 11	All	0		ns
Master reset cycle time	t_{MRSC}		9, 10, 11	01,04	50		ns
				02,05	35		
				03,06	30		
				07	25		
Master reset pulse width 5/	t_{PMR}		9, 10, 11	01,04	40		ns
				02,05	25		
				03,06	20		
				07	15		
Master reset recovery time	t_{RMR}		9, 10, 11	All	10		ns
Read high to master reset high 7/	t_{RPW}		9, 10, 11	01,04	40		ns
				02,05	25		
				03,06	20		
				07	15		
Write high to master reset high 7/	t_{WPW}		9, 10, 11	01,04	40		ns
				02,05	25		
				03,06	20		
				07	15		
Retransmit cycle time	t_{RTC}		9, 10, 11	01,04	50		ns
				02,05	35		
				03,06	30		
				07	25		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ -55EC # T_C # +125EC 4.5 V # V_{CC} # 5.5 V unless otherwise specified	Group A subgroups	Device types	Limits Min	Limits Max	Unit
Retransmit pulse width 4/	t_{PRT}	See figure 3	9, 10, 11	01,04	40		ns
				02,05	25		
				03,06	20		
				07	15		
Retransmit recovery time	t_{RTR}		9, 10, 11	All	10		ns
Master reset to empty flag low	t_{EFL}		9, 10, 11	01,04		50	ns
				02,05		35	
				03,06		30	
				07		25	
Master reset to half-full flag high	t_{HFH}		9, 10, 11	01,04		50	ns
				02,05		35	
				03,06		30	
				07		25	
Master reset to full flag high	t_{FFH}		9, 10, 11	01,04		50	ns
				02,05		35	
				03,06		30	
				07		25	
Read low to empty flag low	t_{REF}		9, 10, 11	01,04		40	ns
				02,05		25	
				03,06		20	
				07		15	
Read high to full flag high	t_{RFF}		9, 10, 11	01,04		40	ns
				02,05		25	
				03,06		20	
				07		15	
Write high to empty flag high	t_{WEF}		9, 10, 11	01,04		40	ns
				02,05		25	
				03,06		20	
				07		15	
Write low to full flag low	t_{WFF}		9, 10, 11	01,04		40	ns
				02,05		25	
				03,06		20	
				07		15	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ -55EC # T_C # +125EC 4.5 V # V_{CC} # 5.5 V unless otherwise specified	Group A subgroups	Device types	Limits Min	Limits Max	Unit
Write low to half-full flag low	t_{WHF}	See figure 3	9, 10, 11	01,04		50	ns
				02,05		35	
				03,06		30	
				07		15	
Read high to half-full flag high	t_{RHF}		9, 10, 11	01,04		50	ns
				02,05		35	
				03,06		30	
				07		15	
Effective read from write high	t_{RAE}		9, 10, 11	01,04		40	ns
				02,05		25	
				02,05		20	
				07		15	
Effective read pulse width after empty flag high	t_{RPE}		9, 10, 11	01,04	40		ns
				02,05	25		
				03,06	20		
				07	15		
Effective write from read high	t_{WAF}		9, 10, 11	01,04		40	ns
				02,05		25	
				03,06		20	
				07		15	
Effective write pulse width after full flag high	t_{WPF}		9, 10, 11	01,04	40		ns
				02,05	25		
				03,06	20		
				07	15		
3/ Expansion out low delay from clock	t_{XOL}		9, 10, 11	01,04		40	ns
				02,05		25	
				03,06		20	
				07		15	
3/ Expansion out high delay from clock	t_{XOH}		9, 10, 11	01,04		50	ns
				02,03			
				05,06		35	
				07		15	

1/ AC tests are performed with input rise and fall times of 5 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V, and the output load in figure 4, circuit A, unless otherwise specified.
2/ These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
3/ Tested initially and after any design or process changes that affect that parameter, and therefore shall be guaranteed to the limits specified in table I.
4/ Transition is measured at steady state high level -500 mV or steady-state low level +500 mV on the output from the 1.5 V level on the input, with output load figure 4 circuit B.
5/ Pulse widths less than minimum are not allowed.
6/ Only applies to read data flow-through mode.
7/ Values guaranteed by design and not currently tested.

Device types	All	
Case outlines	X	Y
Terminal number	Terminal symbol	
1	$\overline{W}$	NC
2	D_8	$\overline{W}$
3	D_3	D_8
4	D_2	D_3
5	D_1	D_2
6	D_0	D_1
7	$\overline{XI}$	D_0
8	$\overline{FF}$	$\overline{XI}$
9	Q_0	FF
10	Q_1	Q_0
11	Q_2	Q_1
12	Q_3	NC
13	Q_8	Q_2
14	GND	Q_3
15	R	Q_8
16	Q_4	GND
17	Q_5	NC
18	Q_6	R
19	Q_7	Q_4
20	$\overline{XO}$/HF	Q_5
21	EF	Q_6
22	$\overline{MR}$	Q_7
23	FL/$\overline{RT}$	$\overline{XO}$/HF
24	D_7	EF
25	D_6	$\overline{MR}$
26	D_5	FL/$\overline{RT}$
27	D_4	NC
28	V_{CC}	D_7
29	---	D_6
30	---	D_5
31	---	D_4
32	---	V_{CC}

NC = no connection

FIGURE 1. Terminal connections.

Reset and retransmit
Single device configuration/width expansion mode

Mode	Inputs			Internal status	Outputs			
	$\overline{MR}$	$\overline{RT}$	$\overline{XI}$	Read pointer	Write pointer	$\overline{EF}$	$\overline{FF}$	$\overline{HF}$
Reset	0	X	0	Location zero	Location zero	0	1	1
Retransmit	1	0	0	Location zero	Unchanged	X	X	X
Read/write	1	1	0	Increment 1/	Increment 1/	X	X	X

1/ Pointer will increment if flag is high.

Reset and first load truth table
Depth expansion/compound expansion mode

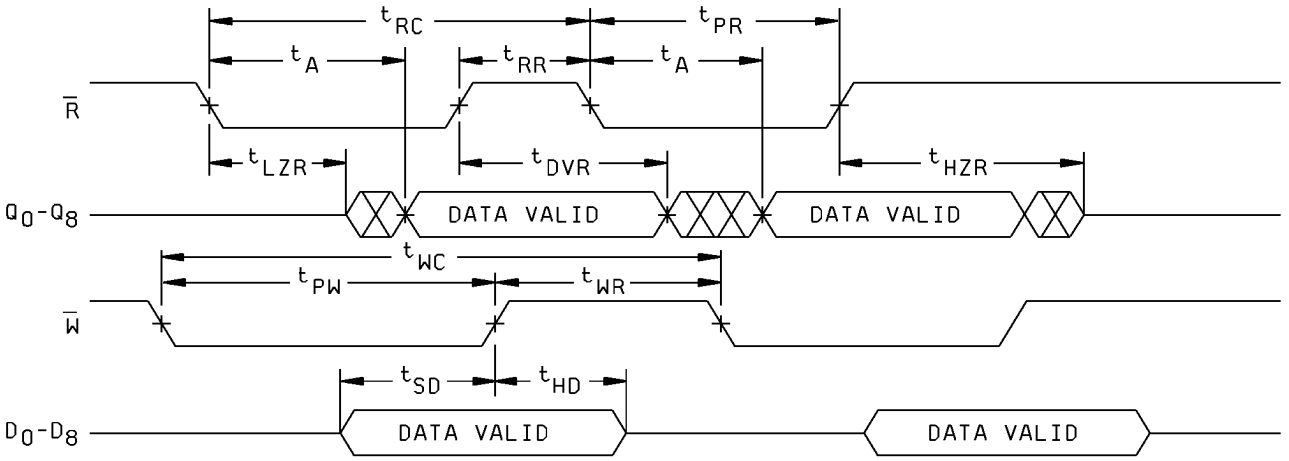
Mode	Inputs			Internal status	Outputs		
	$\overline{MR}$	$\overline{FL}$	$\overline{XI}$	Read pointer	Write pointer	$\overline{EF}$	$\overline{FF}$
Reset first device	0	0	1/	Location zero	Location zero	0	1
Reset all other devices	0	1	1/	Location zero	Location zero	0	1
Read/write	1	X	1/	X	X	X	X

1/ $\overline{XI}$ is connected to $\overline{XO}$ of previous device.

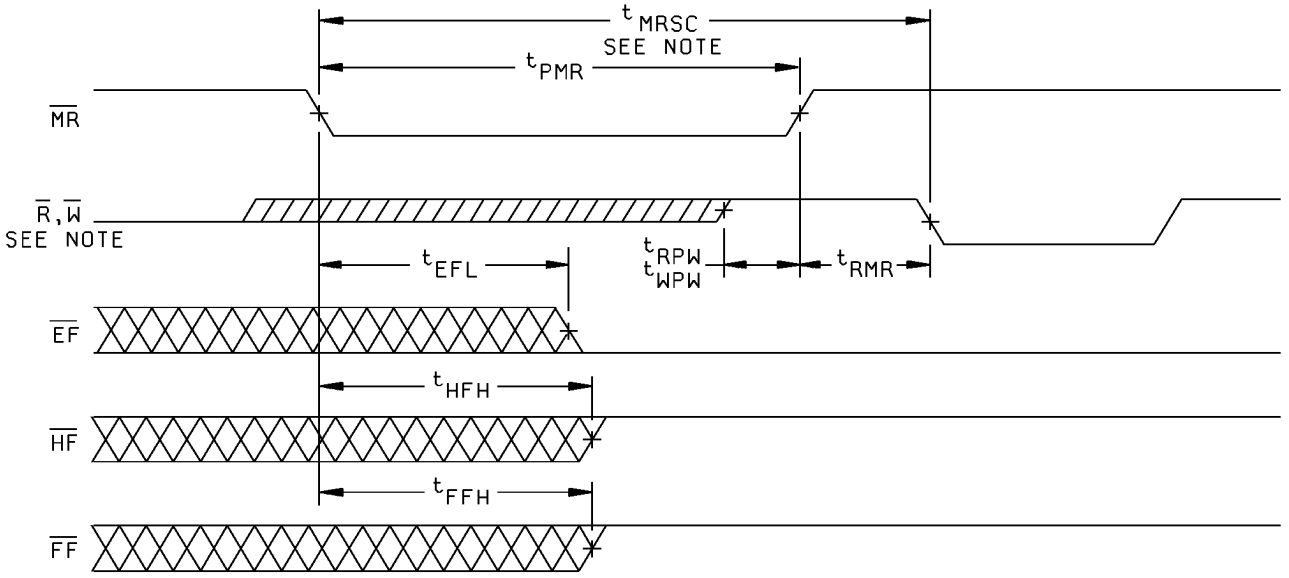
NOTE: $\overline{MR}$ = Reset input, $\overline{FL}$/$\overline{RT}$ = First load/retransmit $\overline{EF}$ = Empty flag output,
$\overline{FF}$ = Full flag output, $\overline{XI}$ = Expansion input, and $\overline{HF}$ = Half-full flag output
0 = Low level voltage
1 = High level voltage
X = Don't care

FIGURE 2. Truth tables.

Asynchronous read and write timing diagram.



Master reset timing diagram.

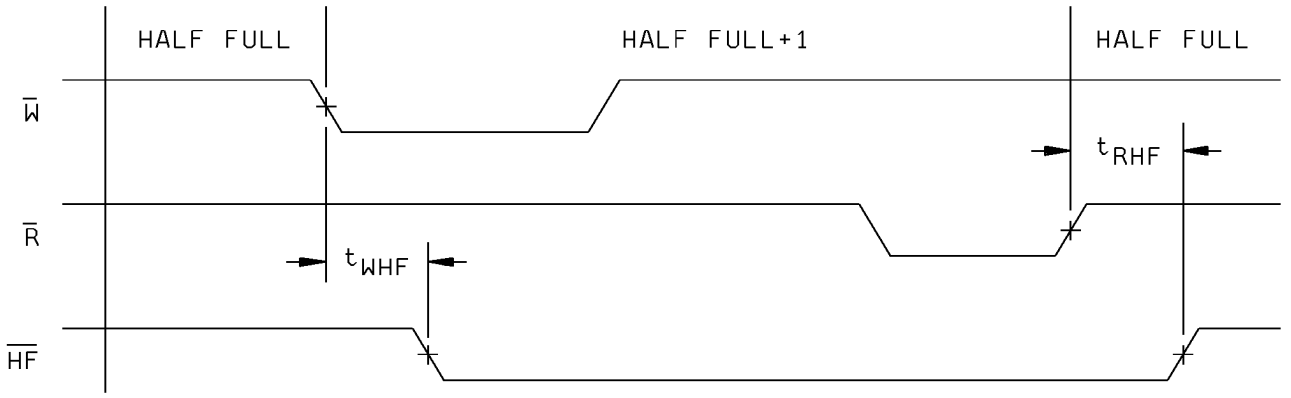


NOTES: 1. $t_{MRSC} = t_{PMR} + t_{RMR}$.

2. $\overline{W}$ and $\overline{R}$ = V_{IH} around the rising edge of $\overline{MR}$.

FIGURE 3. Switching waveforms.

Half-full flag timing diagram.



Last write to first read full flag timing diagram.

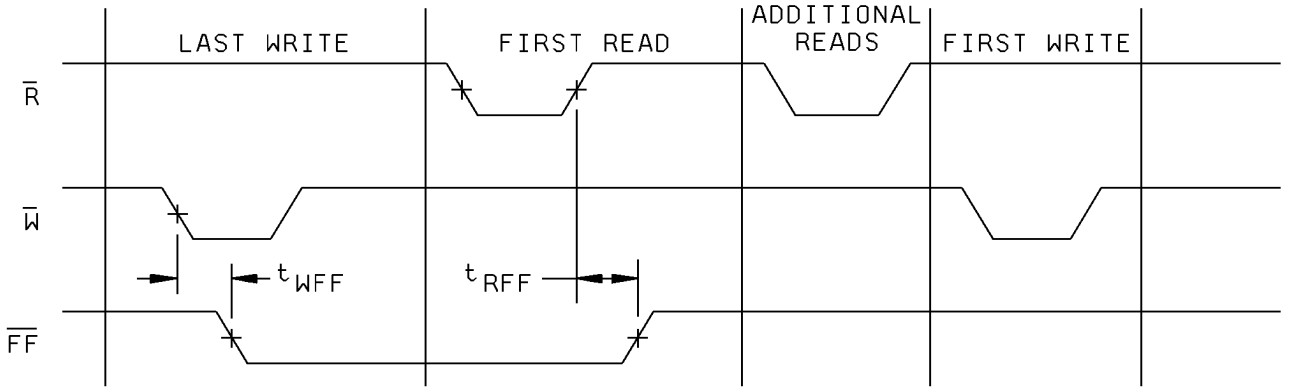
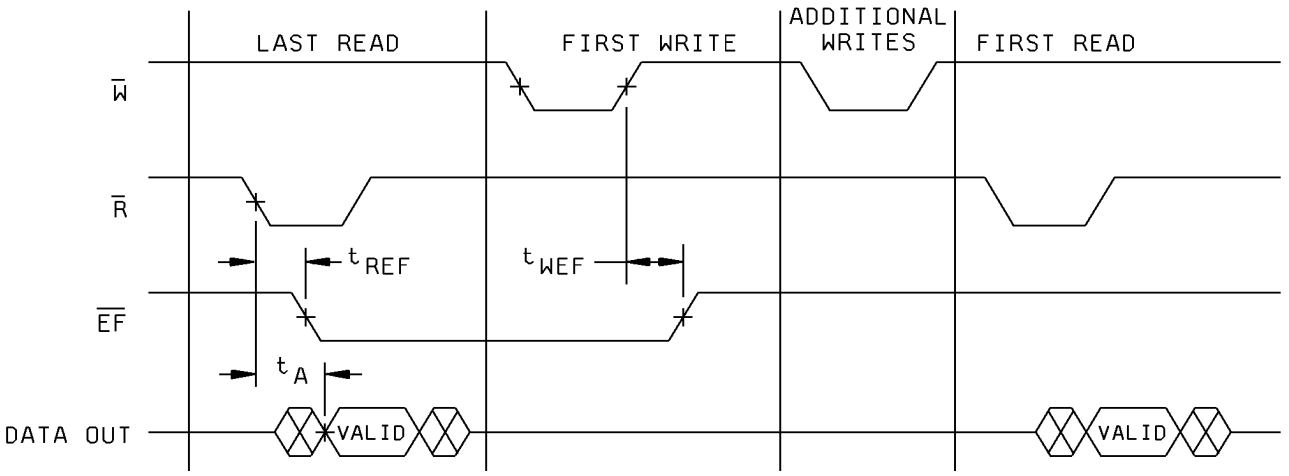
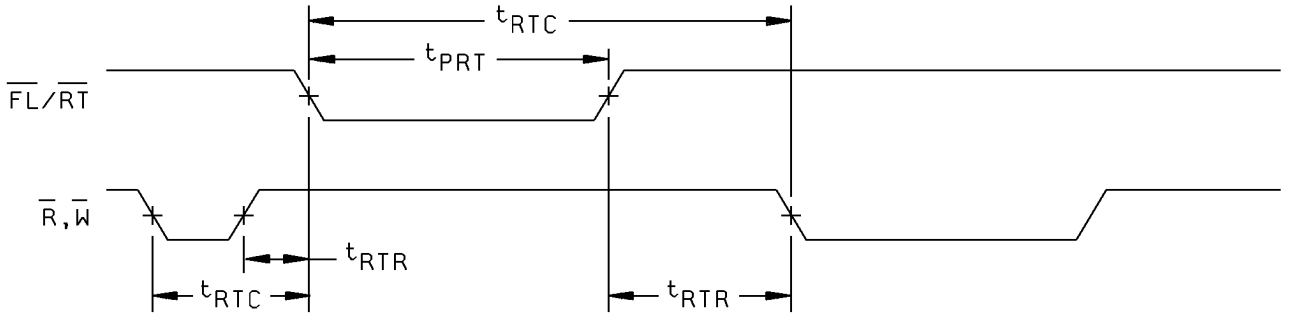


FIGURE 3. Switching waveforms - Continued.

Last read to first write empty flag timing diagram.



Retransmit timing diagram.

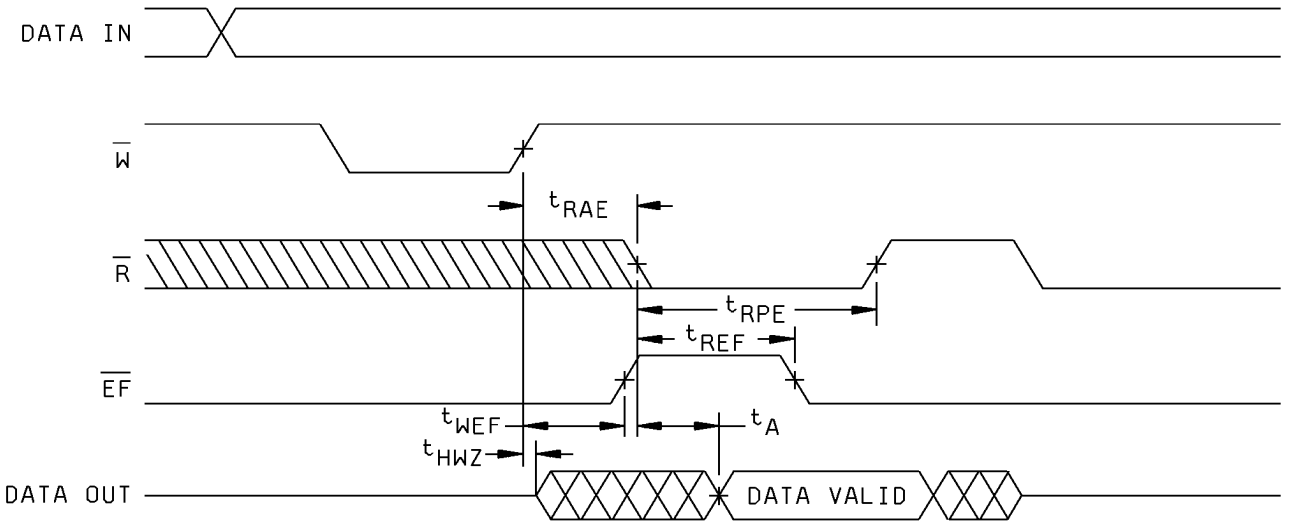


NOTES: 1. $t_{RTC} = t_{PRT} + t_{RTR}$.

2. $\overline{EF}$, $\overline{HF}$ and $\overline{FF}$ may change state during retransmit as a result of the offset of the read and write pointers, but flags will be valid at t_{RTC}, with the exception of device types 03 and 06, whoseflags will be valid after t_{RTC} + 10 ns.

FIGURE 3. Switching waveforms - Continued.

Empty flag and read data flow-through mode timing diagram.



Full flag and write data flow-through mode timing diagram

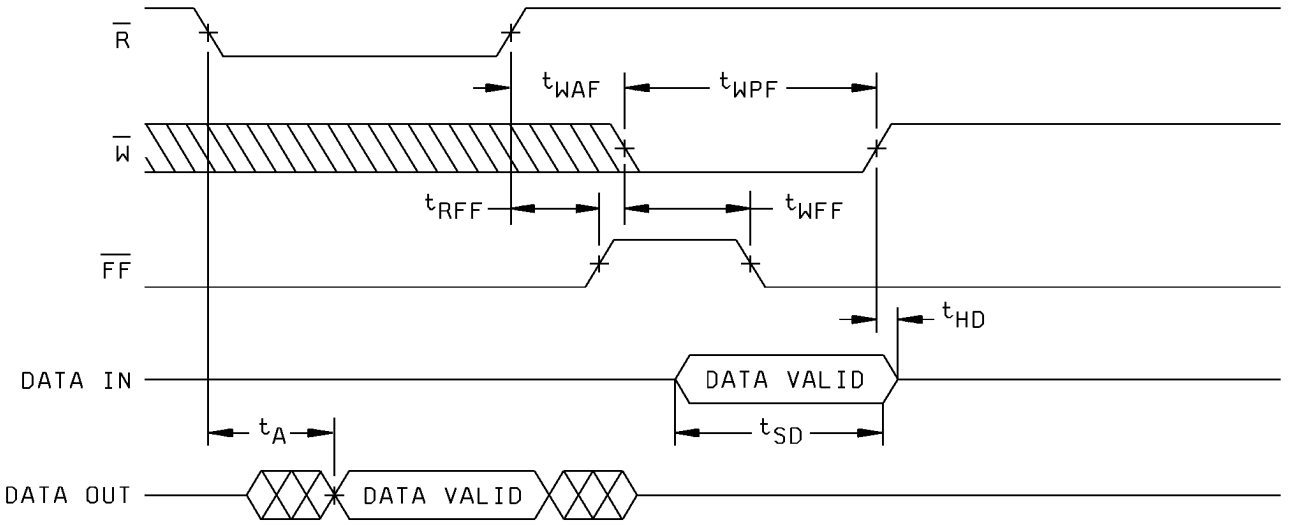
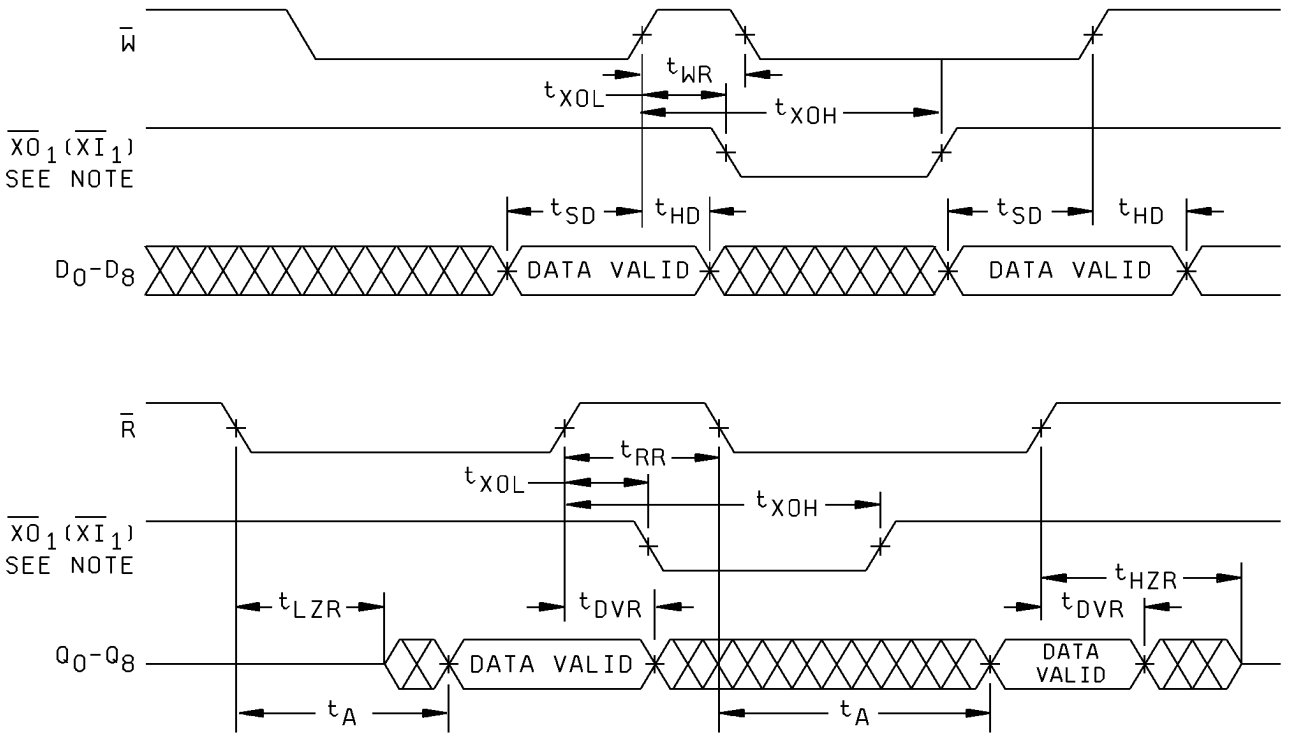


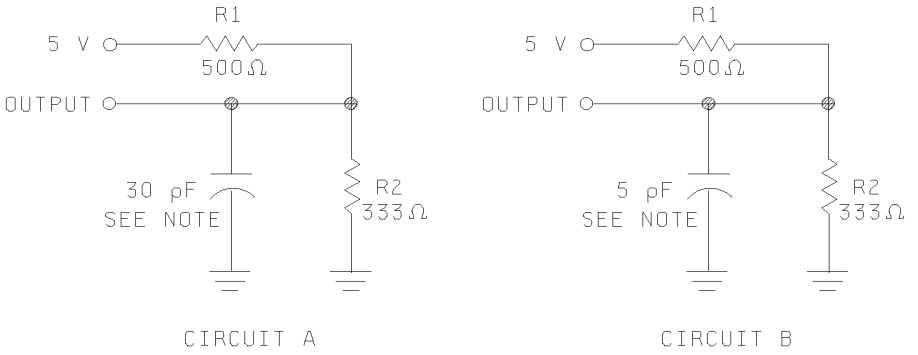
FIGURE 3. Switching waveforms - Continued.

Expansion timing diagrams.



NOTE: Expansion out of device 1 ($\overline{XO}_1$) is connected to expansion in of device 2 ($\overline{XI}_2$).

FIGURE 3. Switching waveforms - Continued.



NOTE: Including scope and jig (minimum values).

AC test conditions

Input pulse levels	GND to 3.0 V
Input rise and fall times	# 5 ns
Input timing reference levels	1.5 V
Output reference levels	1.5 V

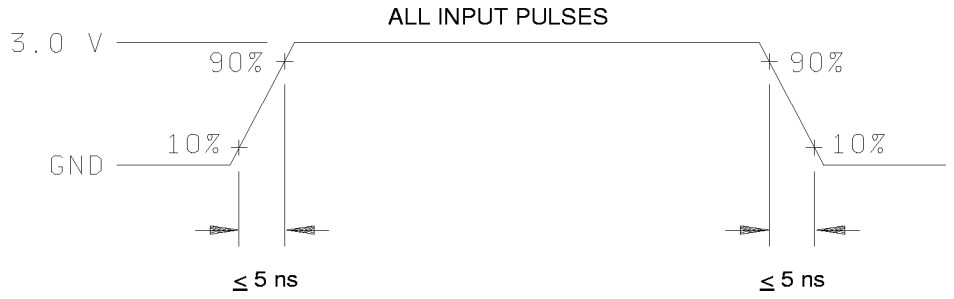


FIGURE 4. Output load circuit and test conditions.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in appendix B of MIL-PRF-38535.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-PRF-38535 permits alternate in-line control testing. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 5 and 6 of table I of method 5005 of MIL-STD-883 shall be omitted.

c. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).

d. O/V (latch-up) tests shall be measured only for initial qualification and after any design or process changes which may affect the performance of the device. For device class M, procedures and circuits shall be maintained under document revision level control by the manufacturer and shall be made available to the preparing activity or acquiring activity upon request. For device classes Q and V, performance of O/V (latch-up) testing shall be as specified in the manufacturer's QM plan, the procedures and circuits shall be under the control of the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the preparing activity or acquiring activity upon request. Testing shall be on all pins, on five devices with zero failures. Latch-up test shall be considered destructive. Information contained in JEDEC Standard EIA/JESD78 may be used for reference.

e. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for initial qualification and after any process or design changes which may affect input or output capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency of 1 MHz. Sample size is 15 devices with no failures, and all input and output terminals tested.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device class M.

a. Steady-state life test conditions, method 1005 of MIL-STD-883:

(1) Test condition D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

(2) T_A = +125EC, minimum.

(3) Test duration: 1,000 hours, except as specified in method 1005 of MIL-STD-883.

TABLE IIA. Electrical test requirements. 1/ 2/ 3/ 4/ 5/ 6/ 7/

Line no.	Test requirements	Subgroups (per method 5005, table I)	Subgroups (per MIL-I-38535, table III)	
		Device class M	Device class Q	Device class V
1	Interim electrical parameters (see 4.2)		1,7,9	1,7,9
2	Static burn-in I method 1015	Not required	Not required	Not required
3	Same as line 1			1*,7*)
4	Dynamic burn-in (method 1015)	Required	Required	Required
5	Same as line 1			1*,7*)
6	Final electrical parameters	1*,2,3,7*, 8A,8B,9,10, 11	1*,2,3,7*, 8A,8B,9,10, 11	1*,2,3,7*, 8A,8B,9,10, 11
7	Group A test requirements	1,2,3,4**,7,8A, 8B,9,10, 11	1,2,3,4**,7, 8A,8B,9,10, 11	1,2,3,4**,7, 8A,8B,9,10, 11
8	Group C end-point electrical parameters	2,3,7, 8A,8B	2,3,7, 8A,8B)	1,2,3,7, 8A,8B,9,10, 11)
9	Group D end-point electrical parameters	2,3,7, 8A,8B	2,3,7, 8A,8B	2,3,7 8A,8B
10	Group E end-point electrical parameters	1,7,9	1,7,9	1,7,9

1/ Blank spaces indicate tests are not applicable.
2/ Any or all subgroups may be combined when using high-speed testers.
3/ Subgroups 7 and 8 functional tests shall verify the truth table.
4/ * indicates PDA applies to subgroups 1 and 7.
5/ ** see 4.4.1e.
6/) indicates delta limit (see table IIB) shall be required where specified, and the delta values shall be computed with reference to the previous interim electrical parameters (see line 1). For device classes Q and V performance of delta limits shall be as specified in the manufacturer's QM plan.
7/ See 4.4.1d.

TABLE IIB. Delta limits at +25EC.

Test 1/	All device types
I_{CC2} standby	±10% of specified value in table I
I_{IX}	±10% of specified value in table I
I_{OZ}	±10% of specified value in table I

1/ The above parameters shall be recorded before and after the required burn-in and life tests to determine the delta.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes M, Q and V shall be as specified in MIL-PRF-38535. End-point electrical parameters shall be as specified in table IIA herein.

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A, for the RHA level being tested. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25EC ±5EC, after exposure, to the subgroups specified in table IIA herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

4.5 Delta measurements for device class V. Delta measurements, as specified in table IIA, shall be made and recorded before and after the required burn-in screens and steady-state life tests to determine delta compliance. The electrical parameters to be measured, with associated delta limits are listed in table IIB. The device manufacturer may, at his option, either perform delta measurements or within 24 hours after life test perform final electrical parameter tests, subgroups 1, 7, 9.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal (Short Form).

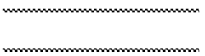
6.3 Record of users. Military and industrial users shall inform Defense Supply Center Columbus when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0525.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43216-5000, or telephone (614) 692-0674.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-STD-1331, and as follows.

C_{IN} . . . . . Input terminal capacitance.
C_{OUT} . . . . . Output and bidirectional output terminal capacitance.
GND . . . . . Ground zero voltage potential.
I_{CC} . . . . . Supply current.
I_{IX} . . . . . Input current.
I_{OZ} . . . . . Output current.
T_C . . . . . Case temperature.
V_{CC} . . . . . Positive supply voltage.

6.5.1 Waveforms.

WAVEFORM SYMBOL	INPUT	OUTPUT
	MUST BE VALID	WILL BE VALID
	CHANGE FROM H TO L	WIIL CHANGE FROM H TO L
	CHANGE FROM L TO H	WILL CHANGE FROM L TO H
	DON'T CARE ANY CHANGE PERMITTED	CHANGING STATE UNKNOWN
		HIGH IMPEDANCE

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING SOURCE APPROVAL BULLETIN

DATE: 99-08-02

Approved sources of supply for SMD 5962-93152 are listed below for immediate acquisition only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535 .

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 3/
5962-9315201MXA	2/	CY7C464-40DMB
5962-9315201MYA	2/	CY7C464-40LMB
5962-9315202MXA	2/	CY7C464-25DMB
5962-9315202MYA	2/	CY7C464-25LMB
5962-9315203MXA	2/	CY7C464-20DMB
5962-9315203MYA	2/	CY7C464-20LMB
5962-9315204QYA	2/	CY7C464A-40LMB
5962-9315205QYA	65786	CY7C464A-25LMB
5962-9315206QYA	65786	CY7C464A-20LMB
5962-9315207QYA	65786	CY7C464A-15LMB

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for the part. If the desired lead finish is not listed, contact the Vendor to determine its availability.

2/ No longer available from an approved source.

3/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
65786	Cypress Semiconductor 3901 North First Street San Jose, CA 95134-1599

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in this information bulletin.