REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																			
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SHEET	15																		

REV STATUS OF SHEETS	REV														
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

STANDARDIZED MILITARY DRAWING

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AMSC N/A

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DRAWING APPROVAL DATE
93-10-05

REVISION LEVEL

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, LINEAR, LOAD SHARE CONTROLLER, MONOLITHIC SILICON

SIZE	CAGE CODE	5962-93206
A	67268	

SHEET 1 OF 15

DESC FORM 193
JUL 91

5962-E399-93

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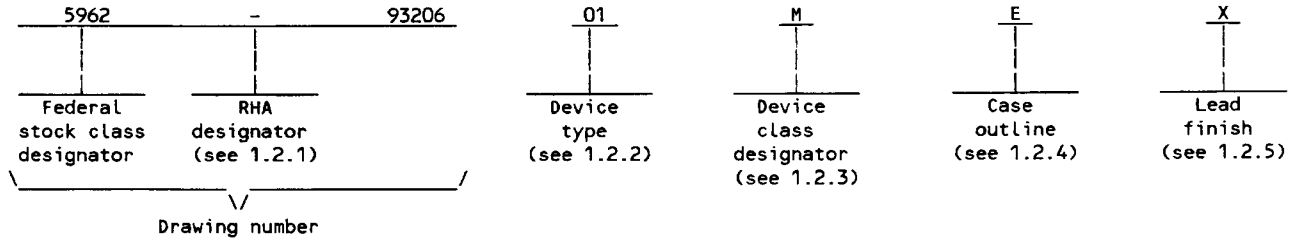
1. SCOPE

1.1 Scope. This drawing forms a part of a one part - one part number documentation system (see 6.6 herein). Two product assurance classes consisting of military high reliability (device classes Q and M) and space application (device class V), and a choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). Device class M microcircuits represent non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices". When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:



1.2.1 RHA designator. Device class M RHA marked devices shall meet the MIL-I-38535 appendix A specified RHA levels and shall be marked with the appropriate RHA designator. Device classes Q and V RHA marked devices shall meet the MIL-I-38535 specified RHA levels and shall be marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	UC1907	Load share controller

1.2.3 Device class designator. The device class designator shall be a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883
Q or V	Certification and qualification to MIL-I-38535

1.2.4 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
E	GDIP1-T16 or CDIP2-T16	16	Dual-in-line
2	CQCC1-N20	20	Square leadless chip carrier

1.2.5 Lead finish. The lead finish shall be as specified in MIL-STD-883 (see 3.1 herein) for class M or MIL-I-38535 for classes Q and V. Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference.

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1.3 Absolute maximum ratings. 1/

Supply voltage	+35 V
Opto output voltage	+35 V
Opto output current	+20 mA
Status indicate sink current	+20 mA
C/S input voltage	+35 V
Share bus voltage range	-0.3 V to +35 V
Maximum forced voltage range (zener clamped)	-0.3 V to +10 V
Maximum forced current range (zener clamped)	±10 mA
Ground amp sink current	+50 mA
V/A, C/A, B/A, D/A sink current	+20 mA
Power dissipation (P_D) (at T_A = +25°C)	1,000 mW 2/
Storage temperature range	-65°C to +150°C
Junction temperature (T_J)	+150°C
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (Θ_{JC})	See MIL-STD-1835

1.4 Recommended operating conditions.

Supply voltage range	+4.5 V to +35 V
Ambient operating temperature range (T_A)	-55°C to +125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, bulletin, and handbook. Unless otherwise specified, the following specification, standards, bulletin, and handbook of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-I-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Microcircuit Case Outlines.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

HANDBOOK

MILITARY

MIL-HDBK-780 - Standardized Military Drawings.

(Copies of the specification, standards, bulletin, and handbook required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ Derate at 10mW/°C for T_A above +50°C.

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2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device class M shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein. The individual item requirements for device classes Q and V shall be in accordance with MIL-I-38535, the device manufacturer's Quality Management (QM) plan, and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-STD-883 (see 3.1 herein) for device class M and MIL-I-38535 for device classes Q and V and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. Marking for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein). In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103. Marking for device classes Q and V shall be in accordance with MIL-I-38535.

3.5.1 Certification/compliance mark. The compliance mark for device class M shall be a "C" as required in MIL-STD-883 (see 3.1 herein). The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-I-38535.

3.6 Certificate of compliance. For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.7.2 herein). For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.7.1 herein). The certificate of compliance submitted to DESC-EC prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device class M, the requirements of MIL-STD-883 (see 3.1 herein), or for device classes Q and V, the requirements of MIL-I-38535 and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required for device class M in MIL-STD-883 (see 3.1 herein) or for device classes Q and V in MIL-I-38535 shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DESC-EC of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-973.

3.9 Verification and review for device class M. For device class M, DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 110 (see MIL-I-38535, appendix A).

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device class M, sampling and inspection procedures shall be in accordance with MIL-STD-883 (see 3.1 herein). For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-I-38535 and the device manufacturer's QM plan.

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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ $V_{IN} = +15$ V unless otherwise specified	Group A subgroups	Device type	Limits 1/		Unit
					Min	Max	
Voltage amp section							
Input voltage	V_{IN}	V/A out = 1 V	1	01	1.975	2.025	V
			2,3		1.960	2.040	
Line regulation	V_{LN}	V_{IN} = 4.5 V to 35 V	1,2,3	01		15	mV
Load regulation	V_{LD}	I_L reference = 0.0 mA to -10 mA	1,2,3	01		10	mV
Long term stability 2/		T_A = +125°C, 1,000 hours	2	01		25	mV
Total output variation		line, load temperature	1,2,3	01	1.960	2.040	
Input adjust range	V_{IA}	A/A from max high to max low	1,2,3	01	85	115	mV
Input bias current	I_{IB}		1,2,3	01	-1		µA
Open loop gain	A_V	V/A out = 0.75 to 1.5 V	4,5,6	01	65		dB
Unity gain bandwidth 2/	UGBW	T_A = +25°C	4	01	700		kHz
Output sink current	I_{SK}	(+)SENSE = 2.2 V, V/A out = 1 V	1,2,3	01	6		mA
Output source current	I_{SC}	(+)SENSE = 1.8 V, V/A out = 1 V	1,2,3	01	400		µA
Output voltage high	V_{OH}	(+)SENSE = 2.2 V, I_L = -400µA	1,2,3	01	1.85		V
Output voltage low	V_{OL}	(+)SENSE = 1.8 V, I_L = +1 mA	1,2,3	01		.40	V

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$, $V_{IN} = +15$ V unless otherwise specified	Group A subgroups	Device type	Limits 1/ Min	Limits 1/ Max	Unit
Reference section							
Output voltage	V_{OUT}		1	01	1.970	2.030	V
			2,3		1.955	2.045	
Short circuit current	I_{OS}	V_{REF} = 0.0 V	1,2,3	01	-15	-60	mA
Ground amp section							
Output voltage	V_{OUT}		1,2,3	01	200	300	mV
Common mode variation	V_{CMV}	(-)SENSE from 0.0 V to 2 V	1,2,3	01		5	mV
Load regulation	V_{LD}	I_L = 0.0 mA to 20 mA	1	01		10	mV
			2,3			15	
Adjust amp section							
Input offset voltage	V_{OS}	A/A out = 1.5 V, V_{CM} = 0.0 V	1,2,3	01	40	60	mV
Input bias current	I_{IB}		1,2,3	01	-2		µA
Open loop gain	A_V	1.5 V ≤ A/A out ≤ 2.25 V	4,5,6	01	65		dB
Transconductance	g_M	I_{OUT} = -10 µA to +10 µA, V_{OUT} = 1.5 V	4,5,6	01	1.7	4.5	mho
Output sink current	I_{SK}	V_{ID} = 0.0 V, A/A out = 1.5 V	1,2,3	01	55	225	µA
Output source current	I_{SC}	V_{ID} = 250 mV, A/A out = 1.5 V	1,2,3	01	110	350	µA

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$, $V_{IN} = +15$ V unless otherwise specified	Group A subgroups	Device type	Limits 1/		Unit
					Min	Max	
Adjust amp section - Continued.							
Output voltage high	V_{OH}	V_{ID} = 250 mV, I_{OUT} = -50 µA	1,2,3	01	2.20	2.90	V
Output voltage low	V_{OL}	V_{ID} = 0.0 V, I_{OUT} = 50 µA	1,2,3	01	0.75	1.15	V
Common mode rejection ratio	CMRR	V_{CM} = 0.0 V to 10 V	4,5,6	01	70		dB
Output gain to V/A		V_{OUT} A/A = 1.5 V to 2 V ▲ (+)SENSE/▲ A/A out	4,5,6	01	50	64	mV/V
Current amp section							
Gain	A	V_{CM} = 0.0 V, V_{ID} = 50 mV to 100 mV	4,5,6	01	19.2	20.1	V/V
Output voltage	V_{OUT}	$+V_{C/A} = -V_{C/A}$ = 0.0 V	1 2,3	01	210 180	290 330	mV
Input offset change with common mode input			1,2,3	01		600	µV/V
Output voltage high	V_{OH}	V_{ID} = 1 V	1,2,3	01	10		V
Output voltage low	V_{OL}	V_{ID} = -1 V, I_L = 1 mA	1,2,3	01		450	mV
Power supply rejection ratio	PSRR	V_{IN} = 4.5 V to 35 V, V_{CM} = 0.0 V	4,5,6	01	60		dB

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ $V_{IN} = +15$ V unless otherwise specified	Group A subgroups	Device type	Limits 1/		Unit
					Min	Max	
Drive amp section. R_{SET} = 500Ω to artifical ground and opto drive = 15 V							
Voltage gain	A	V/A out = 0.5 V to 1V	4,5,6	01	2.3	2.6	V/V
I_{SET} output voltage high	V_{SETH}	(+)SENSE = 2.2 V	1,2,3	01	3.8	4.4	V
I_{SET} output voltage low	V_{SETL}	(+)SENSE = 1.8 V	1,2,3	01		300	mV
Opto output voltage range	V_{VR}		1,2,3	01	4	35	V
Zero current input threshold voltage	V_Z		1,2,3	01	1.55	1.75	V
Buffer amp section							
Input offset voltage	V_{OS}	Input = 1 V	1,2,3	01		5	mV
Output off impedence	Z_O	Input = 1 V, output = 1.5 V to 2.0 V	1,2,3	01	5	20	kΩ
Output source current	I_S	Input =1 V, output = 0.5 V	1,2,3	01	6		mA
Power supply rejection ratio	PSRR	V_{IN} = 4.5 V to 35 V	4,5,6	01	70		dB
Common mode rejection ratio	CMRR	V_{IN} = 0.3 V to 10 V	4,5,6	01	70		dB
Under voltage lockout section							
Start-up threshold voltage	V_{TH}		1,2,3	01		4.4	V

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_A \le +125°C$ $V_{IN} = +15$ V unless otherwise specified	Group A subgroups	Device type	Limits 1/		Unit
					Min	Max	
Status indicate section							
Output voltage low	V_{OL}	A/A- = current share bus	1,2,3	01		0.5	V
Output leakage current	I_{LK}	A/A out = 1 V V_{OUT} = 35 V	1,2,3	01		5	µA
Total stand by current section							
Start-up current	I_{SU}	V_{IN} = UVLO - 0.2 V	1,2,3	01		5	mA
Operating current	I_{CC}	V_{IN} = 35 V	1,2,3	01		10	mA

1/ The algebraic convention, whereby the most negative value is a minimum and the most positive is a maximum, is used in this table.

2/ If not tested, shall be guaranteed to the limits specified in table I herein.

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Device type	01	
Case outlines	E	2
Terminal number	Terminal symbol	
1	C/S OUT	N/C
2	C/S(+)	C/S OUT
3	C/S(-)	C/S(+)
4	(-)SENSE	C/S(-)
5	POWER RETURN	(-)SENSE
6	ARTIFICAL GND	N/C
7	V_{REF}	POWER RETURN
8	I_{SET}	ARTIFICAL GROUND
9	OPTO DRIVE	V_{REF}
10	V_{CC}	I_{SET}
11	(+)SENSE	N/C
12	COMP	OPTO DRIVE
13	ADJ INPUT	V_{CC}
14	ADJ OUT	(+)SENSE
15	CURRENT SHARE BUS	COMP
16	STATUS INDICATE5	N/C
17	---	ADJ INPUT
18	---	ADJ OUT
19	---	CURRENT SHARE BUS
20	---	STATUS INDICATE

FIGURE 1. Terminal connections.

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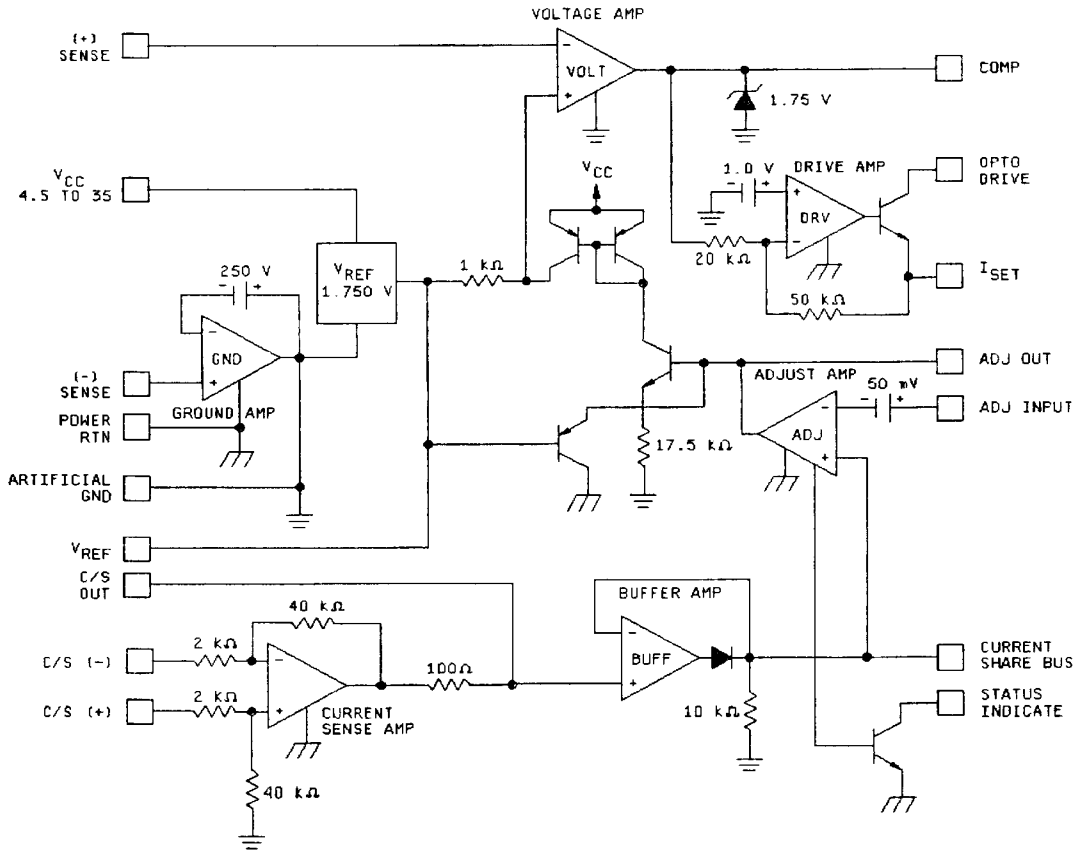

FIGURE 2. Functional block diagram.

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4.2 Screening. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. For device classes Q and V, screening shall be in accordance with MIL-I-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, D, or E. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-I-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in appendix B of MIL-I-38535.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-I-38535. Inspections to be performed shall be those specified in MIL-I-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Quality conformance inspection for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein) and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4). Technology conformance inspection for classes Q and V shall be in accordance with MIL-I-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-I-38535 permits alternate in-line control testing.

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 7, 8, 9, 10, and 11 in table I, method 5005 of MIL-STD-883 shall be omitted.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A, B, C, D, or E. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

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TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, TM 5005, table I)	Subgroups (in accordance with MIL-I-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	---	---	---
Final electrical parameters (see 4.2)	1,2,3,4,5,6 1/	1,2,3,4,5,6 1/	1,2,3, 1/ 4,5,6
Group A test requirements (see 4.4)	1,2,3,4,5,6	1,2,3,4,5,6	1,2,3,4,5,6
Group C end-point electrical parameters (see 4.4)	1,4	1,4	1,4
Group D end-point electrical parameters (see 4.4)	1,4	1,4	1,4
Group E end-point electrical parameters (see 4.4)	---	---	---

1/ PDA applies to subgroup 1.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB, in accordance with MIL-I-38535, and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes Q and V shall be M, D, R, and H and for device class M shall be M and D.

a. End-point electrical parameters shall be as specified in table II herein.

b. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-I-38535, appendix A, for the RHA level being tested. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-I-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

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5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-STD-883 (see 3.1 herein) for device class M and MIL-I-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and which SMD's are applicable to that system. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DESC-EC, telephone (513) 296-6047.

6.4 Comments. Comments on this drawing should be directed to DESC-EC, Dayton, Ohio 45444-5270, or telephone (513) 296-5377.

6.5 Abbreviations, symbols, and definitions.

(-)SENSE	Negative sense. This is s high-impedance pin intended to allow remote sensing of the system ground, bypassing any voltage drops which might appear in the power return line. This point should be considered as the "true" ground. Unless otherwise specified, all voltages are with respect to this point.
ARTIFICIAL GND	Artificial ground. This is a low impedance circuit ground which is exactly 250 millivolts above the (-)SENSE terminal. This offset allows the ground buffer amplifier negative headroom to return all the control bias and operating currents while maintaining a high impedance at the (-)SENSE input.
POWER RETURN	Power return. This should be the most negative voltage available and can range from zero to 5 V below the (-)SENSE terminal. It should be connected as close to the power source as possible so that voltage drops across the return line and current sensing impedances lie between this terminal and the (-)SENSE point.
V_{REF}	The internal voltage reference is a band-gap circuit set at 2.0 V with respect to the (-)SENSE input (1.75 V above the ARTIFICIAL GROUND), and an accuracy of ±1.5%. This circuit, as well as all the other chip functions, will work over a supply voltage range of 4.5 V to 35 V allowing operation from unregulated dc, an auxiliary voltage, or the same output voltage that it is controlling. Under voltage lockout has been included to insure proper start-up by disabling internal bias currents until the reference rises into regulation.
VOLTAGE AMPLIFIER	Voltage amplifier. This circuit is the feed back control gain stage for the power module's output voltage regulator, and overall loop compensation will normally be applied around this amplifier. Its output will swing from slightly above the ground return to an internal clamp of 2.0 V. The reference trimming is performing closed loop, and measured at (+)SENSE pin. The value is trimmed to 2 V ±1.25%.
DRIVE AMPLIFIER	This amplifier is used as an inverting buffer between the VOLTAGE AMPLIFIER's output and the medium used to couple the feedback signal to the power controller. It has a fixed voltage gain of 2.5 and is usually configured with a current-settling resistor to ground. This establishes a current-sinking output optimized to drive optical couples biased at any voltage from 4.5 V to 35 V, with current levels up to 20 mA. The polarity of this stage is such that an increasing voltage at the VOLTAGE AMPLIFIER's sense will increase the opto's current.

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CURRENT AMPLIFIER	This amplifier has differential sensing capability for use with an external shunt in the power return line.
BUFFER AMPLIFIER	This amplifier is a unidirectional buffer which drives the current share bus - the line which will interconnect all power modules paralleled for current sharing. Since the BUFFER AMPLIFIER will only source current, it insures that the module with highest output current will be the master and drive the bus with a low impedance drive capability.
ADJUST AMPLIFIER	This amplifier adjusts the individual module's reference voltage to maintain equal current sharing. The function of this amplifier is to compare its own module output current to the share bus signal - which represents the highest output current - and force an adjust command which is capable of increasing the reference voltage as seen by the voltage amplifier by as much as 100 mV.

6.6 One part - one part number system. The one part - one part number system described below has been developed to allow for transitions between identical generic devices covered by the three major microcircuit requirements documents (MIL-H-38534, MIL-I-38535, and 1.2.1 of MIL-STD-883) without the necessity for the generation of unique PIN's. The three military requirements documents represent different class levels, and previously when a device manufacturer upgraded military product from one class level to another, the benefits of the upgraded product were unavailable to the Original Equipment Manufacturer (OEM), that was contractually locked into the original unique PIN. By establishing a one part number system covering all three documents, the OEM can acquire to the highest class level available for a given generic device to meet system needs without modifying the original contract parts selection criteria.

Military documentation format	Example PIN under new system	Manufacturing source listing	Document listing
New MIL-H-38534 Standardized Military Drawings	5962-XXXXXZZ(H or K)YY	QML-38534	MIL-BUL-103
New MIL-I-38535 Standardized Military Drawings	5962-XXXXXZZ(Q or V)YY	QML-38535	MIL-BUL-103
New 1.2.1 of MIL-STD-883 Standardized Military Drawings	5962-XXXXXZZ(M)YY	MIL-BUL-103	MIL-BUL-103

6.7 Sources of supply.

6.7.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DESC-EC and have agreed to this drawing.

6.7.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-EC.

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