REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																			
SHEET																			
REV																			
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33

REV STATUS OF SHEETS	REV														
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

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DRAWING APPROVAL DATE
95-03-06

REVISION LEVEL

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, DIGITAL, CMOS SERIALLY CONTROLLED ACCESS NETWORK, PARALLEL/SERIAL CONVERTER, TTL COMPATIBLE INPUTS, CMOS OUTPUTS, MONOLITHIC SILICON

SIZE	CAGE CODE	5962-94750
A	67268	

SHEET 1 OF 33

DESC FORM 193
JUL 94

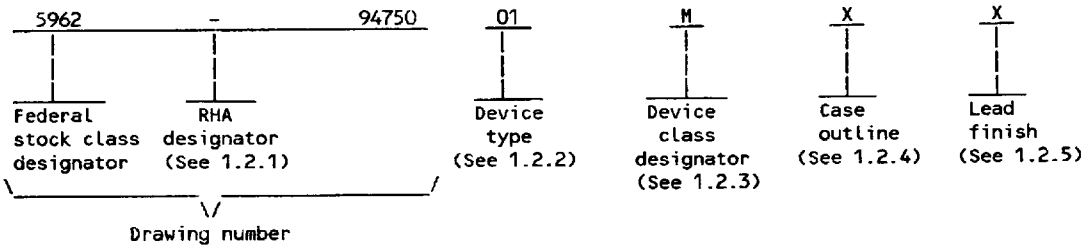
5962-E382-94

9004708 0009467 18T

1. SCOPE

1.1 Scope. This drawing forms a part of a one part - one part number documentation system (see 6.6 herein). Two product assurance classes consisting of military high reliability (device classes Q and M) and space application (device class V), and a choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). Device class M microcircuits represent non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices". When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:



1.2.1 RHA designator. Device class M RHA marked devices shall meet the MIL-I-38535 appendix A specified RHA levels and shall be marked with the appropriate RHA designator. Device classes Q and V RHA marked devices shall meet the MIL-I-38535 specified RHA levels and shall be marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	SCANPSC100F	Serially controlled access network, parallel/serial converter, TTL compatible inputs, CMOS outputs

1.2.3 Device class designator. The device class designator shall be a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883
Q or V	Certification and qualification to MIL-I-38535

1.2.4 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	GDIP1-T28 or CDIP2-T28	28	dual-in-line package
Y	GDFP2-F28	28	flat package
3	CQCC1-N28	28	Leadless-chip-carrier package

1.2.5 Lead finish. The lead finish shall be as specified in MIL-STD-883 (see 3.1 herein) for class M or MIL-I-38535 for classes Q and V. Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference.

1.3 Absolute maximum ratings. 1/ 2/ 3/

Supply voltage range (V_{CC})	-0.5 V dc to +7.0 V dc
DC input voltage range (V_{IN})	-0.5 V dc to V_{CC} + 0.5 V dc
DC output voltage range (V_{OUT})	-0.5 V dc to V_{CC} + 0.5 V dc
DC input clamp current (I_{IK}) (V_{IN} = -0.5 V and V_{CC} + 0.5 V)	±20 mA
DC output clamp current (I_{OK}) (V_{OUT} = -0.5 V and V_{CC} + 0.5 V)	±20 mA
DC output source/sink current (I_{OUT})	±50 mA
DC V_{CC} or GND current (I_{CC}, I_{GND}) per output pin	±50 mA 4/
DC latchup source or sink current	±300 mA
Storage temperature range (T_{STG})	-65°C to +150°C
Maximum power dissipation (P_D)	550 mW
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (Θ_{JC})	See MIL-STD-1835
Junction temperature (T_J)	+175°C

1.4 Recommended operating conditions. 2/ 3/

Supply voltage range (V_{CC})	+4.5 V dc to +5.5 V dc
Input voltage range (V_{IN})	+0.0 V dc to V_{CC}
Output voltage range (V_{OUT})	+0.0 V dc to V_{CC}
Minimum high level input voltage (V_{IH})	2.0 V
Maximum low level input voltage (V_{IL})	0.8 V
Case operating temperature range (T_C)	-55°C to +125°C
Input edge rate ($\Delta V/\Delta t$) minimum: (from V_{IN} = 0.8 V to 2.0 V, 2.0 V to 0.8 V)	125 mV/ns
Maximum high level output current (I_{OH})	-24 mA
Maximum low level output current (I_{OL})	+24 mA

1.5 Digital logic testing for device classes Q and V.

Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012)	XX percent 5/

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability. The maximum junction temperature may be exceeded for allowable short duration burn-in screening conditions in accordance with method 5004 of MIL-STD-883.

2/ Unless otherwise noted, all voltages are referenced to GND.

3/ The limits for the parameters specified herein shall apply over the full specified V_{CC} range and case temperature range of -55°C to +125°C.

4/ This value represents the maximum total current flowing into or out of all V_{CC} or GND pins.

5/ Values will be added when they become available from the qualified source.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, bulletin, and handbook. Unless otherwise specified, the following specification, standards, bulletin, and handbook of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MILITARY

MIL-I-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Microcircuit Case Outlines.

BULLETIN

MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

HANDBOOK

MILITARY

MIL-HDBK-780 - Standardized Military Drawings.

(Copies of the specification, standards, bulletin, and handbook required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents which are DOD adopted are those listed in the issue of the DODISS cited in the solicitation. Unless otherwise specified, the issues of documents not listed in the DODISS are the issues of the documents cited in the solicitation.

ELECTRONIC INDUSTRIES ASSOCIATION (EIA)

JEDEC Standard No. 20 - Standardized for Description of 54/74ACXXXX and 54/74ACTXXXX Advanced High-Speed CMOS Devices.

(Applications for copies should be addressed to the Electronics Industries Association, 2001 Eye Street, NW, Washington, DC 20006.)

INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS (IEEE)

IEEE Standard 1149.1 - IEEE Standard Test Access Port and Boundary-Scan Architecture.

(Applications for copies should be addressed to the Institute of Electrical and Electronics Engineers, 445 Hoes Lane, Piscataway, NJ 08854-4150.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents may also be available in or through libraries or other informational services.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device class M shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein. The individual item requirements for device classes Q and V shall be in accordance with MIL-I-38535, the device manufacturer's Quality Management (QM) plan, and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-STD-883 (see 3.1 herein) for device class M and MIL-I-38535 for device classes Q and V and herein.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Mode and status register. The mode and status register shall be as specified on figure 2.

3.2.4 Parallel processing interface. The parallel processing interface (PPI) shall be as specified on figure 3.

3.2.5 TAP controller state diagram. The TAP controller state diagram shall be as specified on figure 4.

3.2.6 Block diagrams. The block diagrams shall be as specified on figure 5.

3.2.7 Synchronizer and consecutive read/write timing waveforms. The synchronizer and consecutive read/write timing waveforms shall be as specified on figure 6.

3.2.8 Serial scan interface timing waveforms. The serial scan interface timing waveforms shall be as specified on figure 7.

3.2.9 Write cycle and read cycle timing waveforms. The write cycle and read cycle timing waveforms shall be as specified on figure 8.

3.2.10 Reset and interrupt timing waveform. The reset and interrupt timing waveform shall be as specified on figure 9.

3.2.11 Test circuit. The test circuit shall be as specified on figure 10.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. Marking for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein). In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103. Marking for device classes Q and V shall be in accordance with MIL-I-38535.

3.5.1 Certification/compliance mark. The compliance mark for device class M shall be a "C" as required in MIL-STD-883 (see 3.1 herein). The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-I-38535.

3.6 Certificate of compliance. For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.7.2 herein). For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.7.1 herein). The certificate of compliance submitted to DESC-EC prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device class M, the requirements of MIL-STD-883 (see 3.1 herein), or for device classes Q and V, the requirements of MIL-I-38535 and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required for device class M in MIL-STD-883 (see 3.1 herein) or for device classes Q and V in MIL-I-38535 shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DESC-EC of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-973.

3.9 Verification and review for device class M. For device class M, DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 40 (see MIL-I-38535, appendix A).

TABLE I. Electrical performance characteristics.

Test and MIL-STD-883 test method 1/	Symbol	Test conditions 2/ $-55°C \le T_C \le +125°C$ $+4.5\ V \le V_{CC} \le +5.5\ V$ unless otherwise specified	Device type	V_{CC}	Group A subgroups	Limits 3/		Unit
						Min	Max	
High level output voltage 3006	V_{OH1}	For all inputs affecting output under test $V_{IN} = V_{IH}$ or V_{IL} $V_{IH} = 2.0$ V $V_{IL} = 0.8$ V For all other inputs $V_{IN} = V_{CC}$ or GND $I_{OH} = -50\ \mu A$	All	4.5 V	1, 2, 3	4.40		V
	V_{OH2}	For all inputs affecting output under test $V_{IN} = V_{IH}$ or V_{IL} $V_{IH} = 2.0$ V $V_{IL} = 0.8$ V For all other inputs $V_{IN} = V_{CC}$ or GND $I_{OH} = -50.0\ \mu A$		5.5 V		5.40		
	V_{OH3}	For all inputs affecting output under test $V_{IN} = V_{IH}$ or V_{IL} $V_{IH} = 2.0$ V $V_{IL} = 0.8$ V For all other inputs $V_{IN} = V_{CC}$ or GND $I_{OH} = -24.0$ mA		4.5 V	1	3.86		
					2, 3	3.70		
	V_{OH4}	For all inputs affecting output under test $V_{IN} = V_{IH}$ or V_{IL} $V_{IH} = 2.0$ V $V_{IL} = 0.8$ V For all other inputs $V_{IN} = V_{CC}$ or GND $I_{OH} = -24.0$ mA		5.5 V	1	4.86		
					2, 3	4.70		
	V_{OH5} 4/	For all inputs affecting output under test $V_{IN} = V_{IH}$ or V_{IL} $V_{IH} = 2.0$ V $V_{IL} = 0.8$ V For all other inputs $V_{IN} = V_{CC}$ or GND $I_{OH} = -50.0$ mA		5.5 V	1, 2, 3	3.85		
Low level output voltage 3007	V_{OL1}	For all inputs affecting output under test $V_{IN} = V_{IH}$ or V_{IL} $V_{IH} = 2.0$ V $V_{IL} = 0.8$ V For all other inputs $V_{IN} = V_{CC}$ or GND $I_{OL} = 50.0\ \mu A$		4.5 V	1, 2, 3		0.10	
	V_{OL2}	For all inputs affecting output under test $V_{IN} = V_{IH}$ or V_{IL} $V_{IH} = 2.0$ V $V_{IL} = 0.8$ V For all other inputs $V_{IN} = V_{CC}$ or GND $I_{OL} = 50.0\ \mu A$		5.5 V	1, 2, 3		0.10	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test and MIL-STD-883 test method 1/	Symbol	Test conditions 2/ $-55°C \le T_C \le +125°C$ $+4.5\ V \le V_{CC} \le +5.5\ V$ unless otherwise specified	Device type	V_{CC}	Group A subgroups	Limits 3/		Unit
						Min	Max	
Low level output voltage 3007	V_{OL3}	For all inputs affecting output under test $V_{IN} = V_{IH}$ or V_{IL}, $V_{IH} = 2.0$ V, $V_{IL} = 0.8$ V. For all other inputs $V_{IN} = V_{CC}$ or GND. $I_{OL} = 24.0$ mA	All	4.5 V	1		0.36	V
					2, 3		0.50	
	V_{OL4}	For all inputs affecting output under test $V_{IN} = V_{IH}$ or V_{IL}, $V_{IH} = 2.0$ V, $V_{IL} = 0.8$ V. For all other inputs $V_{IN} = V_{CC}$ or GND. $I_{OL} = 24.0$ mA		5.5 V	1		0.36	
					2, 3		0.50	
	V_{OL5} 4/	For all inputs affecting output under test $V_{IN} = V_{IH}$ or V_{IL}, $V_{IH} = 2.0$ V, $V_{IL} = 0.8$ V. For all other inputs $V_{IN} = V_{CC}$ or GND. $I_{OL} = 50.0$ mA			1, 2, 3		1.65	
Maximum input leakage current, high 3010	I_{IH}	For input under test $V_{IN} = 5.5$ V. For all other inputs $V_{IN} = V_{CC}$ or GND	All	5.5 V	1		+0.1	µA
					2, 3		+1.0	
Maximum input leakage current, low 3009	I_{IL}	TDI, $\overline{OE}$ inputs only. For TDI and $\overline{OE}$ inputs $V_{IN} = 0.0$ V. For all other inputs $V_{IN} = V_{CC}$	All	5.5 V	1, 2, 3		-385	µA
		All other inputs. For input under test $V_{IN} = GND$. For all other inputs $V_{IN} = V_{CC}$ or GND			1		-0.1	
					2, 3		-1.0	
Positive input clamp voltage 3022	V_{IC+}	For input under test $I_{IN} = 18$ mA	All	5.5 V	1, 2, 3		5.7	V
Negative input clamp voltage 3022	V_{IC-}	For input under test $I_{IN} = -18$ mA	All	5.5 V	1, 2, 3		-1.2	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test and MIL-STD-883 test method 1/	Symbol	Test conditions 2/ $-55°C \le T_C \le +125°C$ $+4.5\ V \le V_{CC} \le +5.5\ V$ unless otherwise specified	Device type	V_{CC}	Group A subgroups	Limits 3/		Unit
						Min	Max	
Three-state output leakage current, high 3021	I_{OZH} 5/	$\overline{OE}$, R/$\overline{W}$, STB, $\overline{CE}$ = 2.0 V or 0.0 V For all other inputs $V_{IN} = V_{CC}$ or GND	All	4.5 V and 5.5 V	1		0.5	µA
					2, 3		10.0	
Three-state output leakage current, low 3021	I_{OZL} 5/	$\overline{OE}$, R/$\overline{W}$, STB, $\overline{CE}$ = 2.0 V or 0.0 V For all other inputs $V_{IN} = V_{CC}$ or GND	All	4.5 V and 5.5 V	1		-0.5	µA
					2, 3		-10.0	
Input/output leakage current, high	I_{OZHT} 5/	For input/output under test V_{IN} or $V_{OUT} = V_{CC}$ or GND R/$\overline{W}$, $\overline{CE}$, STB = 2.0 V or 0.0 V	All	4.5 V and 5.5 V	1		0.6	µA
					2, 3		11.0	
Input/output leakage current, low	I_{OZLT} 5/	For input/output under test V_{IN} or $_{OUT} = V_{CC}$ or GND R/$\overline{W}$, $\overline{CE}$, STB = 2.0 V or 0.0 V	All	4.5 V and 5.5 V	1		-0.6	µA
					2, 3		-11.0	
Quiescent supply current, high 3005	I_{CCH}	TDI float (OE current subtracted) For all other inputs $V_{IN} = V_{CC}$ or GND	All	5.5 V	1		8.0	µA
					2, 3		160	
		TDI, $\overline{OE}$ = 0.0 V For all other inputs $V_{IN} = V_{CC}$ or GND	All	5.5 V	1		768	µA
					2, 3		920	
Quiescent supply current, low 3005	I_{CCL}	TDI float (OE current subtracted) For all other inputs $V_{IN} = V_{CC}$ or GND	All	5.5 V	1		8.0	µA
					2, 3		160	
		TDI, $\overline{OE}$ = 0.0 V For all other inputs $V_{IN} = V_{CC}$ or GND	All	5.5 V	1		768	µA
					2, 3		920	
Quiescent supply current, three-state 3005	I_{CCZ} 5/	TDI, $\overline{OE}$ float For all other inputs $V_{IN} = V_{CC}$ or GND	All	5.5 V	1		8.0	µA
					2, 3		160	
Quiescent supply current delta, TTL input level 3005	ΔI_{CC} 6/	For input under test $V_{IN} = 3.4$ V TDI, $\overline{OE}$ float	All	5.5 V	1, 2, 3		1.60	mA
		For input under test $V_{IN} = 3.4$ V TDI, $\overline{OE}$ test only Float untested pin					1.65	
Input capacitance 3012	C_{IN}	See 4.4.1b	All	0.0 V	4		8	pF
Output capacitance 3012	C_{OUT}			5.0 V	4		15	
Power dissipation capacitance	C_{PD} 7/				4		100	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test and MIL-STD-883 test method 1/	Symbol	Test conditions 2/ $-55°C \le T_C \le +125°C$ $+4.5\ V \le V_{CC} \le +5.5\ V$ unless otherwise specified	Device type	V_{CC}	Group A subgroups	Limits 3/		Unit
						Min	Max	
Functional test 3014		See 4.4.1c	All	4.5 V and 5.5 V	7, 8			
Propagation delay time, Am to Dn	t_{PLH1}, t_{PHL1} 8/	C_L = 50 pF minimum, R_L = 500Ω, See figure 6	All	4.5 V	1	6.5	21.0	ns
					2, 3	6.5	24.0	
Propagation delay time, Am to RDY	t_{PLH2}, t_{PHL2} 8/		All	4.5 V	1	5.5	18.5	ns
					2, 3	5.5	21.0	
Propagation delay time, SCK to Dn	t_{PLH3}, t_{PHL3} 8/		All	4.5 V	1	7.5	34.0	ns
					2, 3	7.5	39.0	
Propagation delay time, SCK to RDY	t_{PHL4} 8/		All	4.5 V	1	10.0	31.0	ns
					2, 3	10.0	36.0	
Propagation delay time, STB to RDY	t_{PLH5} 8/		All	4.5 V	1	7.0	20.0	ns
					2, 3	7.0	24.0	
Propagation delay time, R/W to RDY	t_{PLH6}, t_{PHL6} 8/		All	4.5 V	1	5.0	16.5	ns
					2, 3	5.0	19.5	
Setup time, high, STB to SCK	t_{s1} 9/		All	4.5 V	1, 2, 3	7.5		ns
Hold time, low, STB to SCK, RDY to STB	t_{h1} 9/		All	4.5 V	1, 2, 3	0.0		ns
Pulse width, high or low SCK	t_{w1} 9/		All	4.5 V	1, 2, 3	20.0		ns
Pulse width, high or low STB	t_{w2} 9/		All	4.5 V	1, 2, 3	6.0		ns
Propagation delay time, FRZ to TCK	t_{PLH7}, t_{PHL7} 8/	C_L = 50 pF minimum, R_L = 500Ω, See figure 7	All	4.5 V	1	3.0	11.5	ns
					2, 3	3.0	13.5	
Propagation delay time, TDI to TDO	t_{PLH8}, t_{PHL8} 8/		All	4.5 V	1	3.5	13.0	ns
					2, 3	3.5	15.0	
Propagation delay time, SCK to TDO	t_{PLH9}, t_{PHL9} 8/		All	4.5 V	1	5.5	17.5	ns
					2, 3	5.5	19.5	
Propagation delay time, SCK to TMS	t_{PLH10}, t_{PHL10} 8/		All	4.5 V	1	4.5	16.0	ns
					2, 3	4.5	18.5	
Propagation delay time, SCK to TCK	t_{PLH11}, t_{PHL11} 8/		All	4.5 V	1	3.0	12.0	ns
					2, 3	3.0	14.0	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test and MIL-STD-883 test method 1/	Symbol	Test conditions 2/ $-55°C \le T_C \le +125°C$ $+4.5\ V \le V_{CC} \le +5.5\ V$ unless otherwise specified	Device type	V_{CC}	Group A subgroups	Limits 3/		Unit
						Min	Max	
Propagation delay time, output enable, OE to TCK	t_{PZL1}, t_{PZH1} 8/	C_L = 50 pF minimum, R_L = 500Ω, See figure 7	All	4.5 V	1	2.0	11.0	ns
					2, 3	2.0	13.0	
Propagation delay time, output disable, OE to TCK	t_{PLZ1}, t_{PHZ1} 8/		All	4.5 V	1	1.5	9.5	ns
					2, 3	1.5	11.0	
Propagation delay time, output enable, OE to TDO	t_{PZL2}, t_{PZH2} 8/		All	4.5 V	1	2.0	11.0	ns
					2, 3	2.0	13.0	
Propagation delay time, output disable, OE to TDO	t_{PLZ2}, t_{PHZ2} 8/		All	4.5 V	1	1.5	9.5	ns
					2, 3	1.5	11.0	
Propagation delay time, output enable, OE to TMSO	t_{PZL3}, t_{PZH3} 8/		All	4.5 V	1	2.0	11.0	ns
					2, 3	2.0	13.0	
Propagation delay time, output disable, OE to TMSO	t_{PLZ3}, t_{PHZ3} 8/		All	4.5 V	1	1.5	9.5	ns
					2, 3	1.5	11.0	
Propagation delay time, output enable, OE to TMS1	t_{PZL4}, t_{PZH4} 8/		All	4.5 V	1	2.0	11.0	ns
					2, 3	2.0	13.0	
Propagation delay time, output disable, OE to TMS1	t_{PLZ4}, t_{PHZ4} 8/		All	4.5 V	1	1.5	9.5	ns
					2, 3	1.5	11.0	
Setup time, high or low, TDI to SCK	t_{s2} 9/		All	4.5 V	1, 2, 3	7.5		ns
Hold time, high or low, TDI to SCK	t_{h2} 9/		All	4.5 V	1, 2, 3	0.5		ns
Maximum clock frequency SCK	f_{MAX}		All	4.5 V	1, 2, 3	25.0		MHz

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test and MIL-STD-883 test method 1/	Symbol	Test conditions 2/ $-55°C \le T_C \le +125°C$ $+4.5\ V \le V_{CC} \le +5.5\ V$ unless otherwise specified	Device type	V_{CC}	Group A subgroups	Limits 3/		Unit
						Min	Max	
Propagation delay time, output enable, CE to RDY	t_{PZH5}, t_{PZL5} 8/	C_L = 50 pF minimum, R_L = 500Ω, See figure 8	All	4.5 V	1	2.0	11.0	ns
					2, 3	2.0	13.0	
Propagation delay time, output disable, CE to RDY	t_{PHZ5}, t_{PLZ5} 8/		All	4.5 V	1	1.5	8.5	ns
					2, 3	1.5	10.0	
Propagation delay time, output enable, CE to Dn	t_{PZH6}, t_{PZL6} 8/		All	4.5 V	1	1.5	14.0	ns
					2, 3	1.5	16.5	
Propagation delay time, output disable, CE to Dn	t_{PHZ6}, t_{PLZ6} 8/		All	4.5 V	1	2.5	13.0	ns
					2, 3	2.5	14.5	
Propagation delay time, output enable, R/W to Dn	t_{PZL7}, t_{PZH7} 8/		All	4.5 V	1	3.0	15.0	ns
					2, 3	3.0	17.5	
Propagation delay time, output disable, R/W to Dn	t_{PLZ7}, t_{PHZ7} 8/		All	4.5 V	1	3.0	14.0	ns
					2, 3	3.0	16.0	
Propagation delay time, output enable, STB to Dn	t_{PZH8}, t_{PZL8} 8/		All	4.5 V	1	3.0	14.0	ns
					2, 3	3.0	16.0	
Propagation delay time, output disable, STB to Dn	t_{PHZ8}, t_{PLZ8} 8/		All	4.5 V	1	2.5	12.0	ns
					2, 3	2.5	14.5	
Setup time, high, CE to STB	t_{s3} 9/		All	4.5 V	1, 2, 3	0.5		ns
Hold time, high, CE to STB	t_{h3} 9/		All	4.5 V	1, 2, 3	1.0		ns
Setup time, high or low, R/W to STB	t_{s4} 9/		All	4.5 V	1, 2, 3	1.0		ns
Hold time, high or low, R/W to STB	t_{h4} 9/		All	4.5 V	1, 2, 3	0.5		ns
Setup time, high or low, Am to STB	t_{s5} 9/		All	4.5 V	1, 2, 3	5.0		ns
Hold time, high or low, Am to STB	t_{h5} 9/		All	4.5 V	1, 2, 3	4.5		ns
Setup time, high or low, Dn to STB	t_{s6} 9/		All	4.5 V	1, 2, 3	0.0		ns
Hold time, high or low, Dn to STB	t_{h6} 9/		All	4.5 V	1, 2, 3	4.5		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test and MIL-STD-883 test method 1/	Symbol	Test conditions 2/ $-55°C \le T_C \le +125°C$ $+4.5\ V \le V_{CC} \le +5.5\ V$ unless otherwise specified	Device type	V_{CC}	Group A subgroups	Limits 3/		Unit
						Min	Max	
Propagation delay time, RST to INT	t_{PHL12} 8/	C_L = 50 pF minimum, R_L = 500Ω, See figure 9	All	4.5 V	1	7.0	26.0	ns
					2, 3	7.0	28.0	
Propagation delay time, RST to TDO	t_{PLH13} 8/		All	4.5 V	1	5.5	18.0	ns
					2, 3	5.5	21.0	
Propagation delay time, SCK to INT	t_{PHL14}, t_{PLH14} 8/		All	4.5 V	1	9.0	29.0	ns
					2, 3	9.0	34.0	
Propagation delay time, RST to Dn	t_{PHL15}, t_{PLH15} 8/		All	4.5 V	1	8.0	25.0	ns
					2, 3	8.0	29.5	
Propagation delay time, RST to RDY	t_{PHL16}, t_{PLH16} 8/		All	4.5 V	1	8.0	27.0	ns
					2, 3	8.0	31.0	
Propagation delay time, RST to TMS	t_{PLH17} 8/		All	4.5 V	1	5.5	17.0	ns
					2, 3	5.5	20.0	
Pulse width, low, RST	t_{W3} 9/		All	4.5 V	1, 2, 3	6.5		ns
Recovery time, SCK to $\overline{RST}$	t_{REC} 9/		All	4.5 V	1, 2, 3	1.0		ns

1/ For tests not listed in the referenced MIL-STD-883 (e.g. ΔI_{CC}), utilize the general test procedure under the conditions listed herein. All inputs and outputs shall be tested, as applicable, to the tests in table I herein.

2/ Each input/output, as applicable, shall be tested at the specified temperature, for the specified limits, to the tests in table I herein. Output terminals not designated shall be high level logic, low level logic, or open, except for the ΔI_{CC} and I_{CC} tests, the output terminals shall be open. When performing the ΔI_{CC} and I_{CC} tests, the current meter shall be placed in the circuit such that all current flows through the meter.

3/ For negative and positive voltage and current values, the sign designates the potential difference in reference to GND and the direction of current flow respectively; and the absolute value of the magnitude, not the sign, is relative to the minimum and maximum limits, as applicable, listed herein. All devices shall meet the limits specified in table I, as applicable, at $4.5\ V \le V_{CC} \le 5.5\ V$.

4/ Transmission driving tests are performed at V_{CC} = 5.5 V dc with a 2 ms duration maximum. This test may be performed using $V_{IN} = V_{CC}$ or GND. When $V_{IN} = V_{CC}$ or GND is used, the test is guaranteed for V_{IN} = 2.0 V or 0.8 V.

5/ Three-state output conditions are required.

6/ This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V_{CC}. This test may be performed either one input at a time (preferred method) or with all input pins simultaneously at $V_{IN} = V_{CC}$ -2.1 V (alternate method). When the test is performed using the alternate test method, the maximum limits is equal to the number of inputs at a high TTL input level times 1.6 mA or 1.65 mA, as applicable; and the preferred method and limits are guaranteed.

7/ Power dissipation capacitance (C_{PD}) determines both the power consumption (P_D) and current consumption (I_S). Where

$P_D = (C_{PD} + C_L) (V_{CC} \times V_{CC})f + (I_{CC} \times V_{CC}) + (n \times d \times \Delta I_{CC} \times V_{CC})$

$I_S = (C_{PD} + C_L) V_{CC} f + I_{CC} + (n \times d \times \Delta I_{CC})$

and f is the frequency of the input signal, n is the number of device inputs at TTL levels; and d is the duty cycle of the input signal.

8/ AC limits at V_{CC} = 5.5 V are equal to the limits at V_{CC} = 4.5 V and guaranteed by testing at V_{CC} = 4.5 V. Minimum propagation delay time limits for V_{CC} = 5.5 V shall be guaranteed to be no more than 0.5 ns less than those specified at V_{CC} = 4.5 V in table I herein. For propagation delay tests, all paths must be tested.

9/ This parameter shall be guaranteed, if not tested, to the limits in table I herein.

Device type	01		
Case outlines	X, Y and 3		
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	$\overline{RST}$	15	D4
2	SCK	16	D5
3	$\overline{OE}$	17	D6
4	$\overline{CE}$	18	D7
5	R/$\overline{W}$	19	INT
6	STB	20	$\overline{RDY}$
7	A0	21	TDO
8	A1	22	GND
9	A2	23	TMS0
10	D0	24	TMS1
11	D1	25	TCK
12	D2	26	TDI
13	D3	27	FRZ
14	GND	28	V_{CC}

FIGURE 1. Terminal connections.

Terminal symbol description	
Terminal symbol	Description
$\overline{RST}$ (input)	The reset pin is an asynchronous input that, when low, initializes device type 01. Mode bits, shifter/buffer and 32-bit counter control logic, TCK control, and the parallel processor interface (PPI) are all initialized to define states. RST has hysteresis for improved noise immunity.
SCK (input)	The system clock drives all internal timing. Also, TCK is a gated and buffered version of SCK. SCK has hysteresis for improved noise immunity.
$\overline{OE}$ (input)	Output enable three-states all serial scan interface (SSI) outputs when high. A 20 kΩ pull-up resistor is connected to automatically three-state these outputs when this signal is floating.
$\overline{CE}$ (input)	Chip enable, when low, enables the parallel processor interface (PPI) for byte transfers. Dn (n = 0 to 7) and $\overline{RDY}$ are three-stated if $\overline{CE}$ is high. $\overline{CE}$ has hysteresis for improved noise immunity.
R/$\overline{W}$ (input)	Read/write defines a parallel processor interface (PPI) cycle - Read when high, write when low. R/$\overline{W}$ has hysteresis for improved noise immunity.
STB (input)	Strobe is used for timing all parallel processor interface (PPI) byte transfers. Dn (n = 0 to 7) are three-stated when STB is high. All other PPI inputs must meet specified setup and hold times with respect to this signal. STB has hysteresis for improved noise immunity.
Am (m = 0 to 2)	The address pins are used to select the register to be written to or read from.
Dn (n = 0 to 7) (I/O)	Bidirectional pins used to transfer parallel data to and from device type 01.
INT (output)	Interrupt is used to trigger a host interrupt for any of the defined interrupt events. INT is active high.
$\overline{RDY}$ (three-state output)	Ready is used to synchronize asynchronous byte transfers between the host and device type 01. When low, $\overline{RDY}$ signals that the addressed register is ready to be accessed. $\overline{RDY}$ is enabled when $\overline{CE}$ is low.
TDO (three-state output)	Test data out is the serial scan output from device type 01. TDO is enabled when $\overline{OE}$ is low.
TMS (0 to 1) (three-state output)	The test mode select pins are serial outputs used to supply control logic to the unit under test (UUT). TMS (0 to 1) are enabled when $\overline{OE}$ is low.
TCK (three-state output)	The test clock output is a buffered version of SCK for distribution in the unit under test. TCK control logic starts and stops TCK to prevent overflow and underflow conditions. TCK is enabled when $\overline{OE}$ is low.
TDI (input)	Test data in is the serial scan input to device type 01. A 20 kΩ pull-up resistor is connected to force TDI to a logic 1 when the TDO line from the unit under test is floating.
FRZ (input)	The freeze pin is used to generate user-specific pulses on TCK. If the FRZ enable mode bit is set, TCK will be forced high if FRZ goes high. FRZ has hysteresis for improved noise immunity.

FIGURE 1. Terminal connections - Continued.

Mode register 0 (Mode 0)							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TDO enable	TDI enable	32 Bit counter enable	TMS0 enable	TMS1 enable	32 Bit counter Freeze enable	TMS high enable	Loop-around enable

This register is purely a mode register. All bits are writeable and readable. The value 00100000 is placed in this register upon RST low or a synchronous reset operation. The following describes each Bit:

Bit 7: This bit signifies that the TDO shifter/buffer is enabled for shift operations. If this bit is set, the TDO shifter/buffer will cause TCK to stop if it is empty.

Bit 6: This bit signifies that the TDI shifter/buffer is enabled for shift operations. If this bit is set, the TDI shifter/buffer will cause TCK to stop if it is full

Bit 5: This bit signifies that the 32-bit counter is enabled. If this bit is set, the counter will cause TCK to stop if it has not been loaded or if it has reached terminal count.

Bit 4: This bit signifies that the TMS0 shifter/buffer is enabled for shift operations. If this bit is set, the TMS0 shifter/buffer will cause TCK to stop if it is empty.

Bit 3: This bit signifies that the TMS1 shifter/buffer is enabled for shift operations. If this bit is set, the TMS1 shifter/buffer will cause TCK to stop if it is empty.

Bit 2: If this bit is set, the 32-bit counter will cause a single TCK pulse to be issued upon terminal count.

Bit 1: If this bit is set, TMS will be forced high when the 32-bit counter is at state 00000001.

Bit 0: This bit causes TDI to be connected directly back through TDO for loop-around operations.

FIGURE 2. Mode and status registers.

Mode register 1 (Mode 1)							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TDO interrupt enable	TDI interrupt enable	32 bit counter interrupt enable	Pseudo ramdom pattern generator (PRPG) enable	Serial signature compactor (SSC) enable	Freeze pin enable	Test loop-back	Test loop-back

This register is purely a mode register. All bits are writeable and readable. The value 00000000 is placed in this register upon RST low or a synchronous reset operation. The following describes each Bit:

Bit 7: If this bit is set, and the TDO shifter/buffer is not full, the INT pin will go high.

Bit 6: If this bit is set, and the TDI shifter/buffer is not empty, the INT pin will go high.

Bit 5: If this bit is set, and the 32-bit counter is not loaded or has reached terminal count, the INT pin will go high.

Bit 4: This bit signifies that the TDO shifter/buffer is reconfigured as a 32-bit Pseudo Random Pattern Generator (PRPG). If set, and MODE0 Bit 7 is set, the TDO shifter/buffer will stop TCK until a seed value has been written to all four of the 8-bit Linear Feedback Shift register (LFSR) segments.

Bit 3: This bit signifies that the TDI shifter/buffer is reconfigured as a 16-bit Serial Signature Compactor (SSC). If set, the TDI shifter/buffer will cause TCK to stop until a seed value has been written to the two TDI registers.

Bit 2: If this bit is set, a high value on FRZ will force TCK high.

Bits 1 and 0: These bits are used to control test loop-back operations according to the following table:

Mode 1 Bit 1	Mode 1 Bit 0	Function
0	0	Normal operation
0	1	Loop-back TDO
1	0	Loop-back TMS0
1	0	Loop-back TMS1

FIGURE 2. Mode and status registers - Continued.

Mode register 2 (Mode 2) (Write)							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Not used	Not used	Not used	Not used	Continuous update	Update status	Reset	Single step 32-bit counter

Mode register 2 (Mode 2) (Read)							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TDO status	TDI status	32-bit counter status	TMS0 status	TMS1 status	Continuous update	Reset	Single step 32-bit counter

This register contains both mode and status bits. Bits 4 to 7 are status bits only. Bit 3 is a status bit during read operations and a mode bit during write operations. Bits 0 to 2 are mode bits only. Upon RST low, or a synchronous reset, the value placed in Mode 2 is 10111000 (read mode). Latches used to update status bits 4 to 7 retain their last state upon RST and are in an "unknown" state after power-up. To initialize the latches to a known state, they need to be updated using the update bit (bit 2). The following describes each Bit:

Bit 7: Set high if the TDO shifter/buffer is not full, i.e., it is ready to be written.

Bit 6: Set high if the TDI shifter/buffer is not empty, i.e., it is ready to be read.

Bit 5: Set high if the 32-bit counter has not been loaded, or has reached terminal count.

Bit 4: Set high if the TMS0 shifter/buffer is not full, i.e., it is ready to be written.

Bit 3 (Read cycle): Set high if the TMS1 shifter/buffer is not full, i.e., it is ready to be written.

Bit 3 (Write cycle): If set, will cause all status bits to be continuously updated.

Bit 2 (Read cycle): Shows the state of the continuous update bit during read operations (Bit 3 during writes).

Bit 2 (Write cycle): If set, will cause a pulse to be issued internally that will update 2 status bits. This bit will be reset upon completion of the pulse. The state of this bit is not readable. It is reset upon RST low.

Bit 1: If set, will cause a synchronous reset of all functions except the parallel interface. The value of this bit will return to zero when the reset operation is complete.

Bit 0: If set, will cause the 32-bit counter to count for one clock cycle. The value of this bit will return to zero when the single step operation is complete.

FIGURE 2. Mode and status registers - Continued.

Parallel processor interface (PPI) address assignment:

The following table defines which register is selected for access with the address lines, A = 0 to 2.

PPI address assignment				
A2	A1	A0	R/$\overline{W}$	Function
0	0	0	0	TDO shifter/buffer
0	0	0	1	Counter register 1
0	0	1	0	TDI shifter/buffer
0	0	1	1	TDI shifter/buffer
0	1	0	0	TMSO shifter/buffer
0	1	0	1	Counter register 2
0	1	1	0	TMS1 shifter/buffer
0	1	1	1	Counter register 3
1	0	0	0	32-bit counter
1	0	0	1	Counter register 0
1	0	1	0	MODE0
1	0	1	1	MODE0
1	1	0	0	MODE1
1	1	0	1	MODE1
1	1	1	0	MODE2
1	1	1	1	MODE2

FIGURE 3. Parallel processor interface.

Ready logic:

$\overline{RDY}$ = 0 signifies that the device is ready to complete the current PPI cycle. The logic that determines the state of $\overline{RDY}$ is summarized in the following table.

R/$\overline{W}$	Write synchronizer busy	TDO shifter/buffer full and Am (m = 2 to 0) = 0	TMS0 shifter/buffer full and Am (m = 2 to 0) = 2	TMS1 shifter/buffer full and Am (m = 2 to 0) = 3	Read synchronizer busy	TDI shifter/buffer empty and Am (m = 2 to 0) = 1	$\overline{RDY}$
0	1	X	X	X	X	X	1
0	X	1	X	X	X	X	1
0	X	X	1	X	X	X	1
0	X	X	X	1	X	X	1
0	0	0	0	0	X	X	0
1	X	X	X	X	1	X	1
1	X	X	X	X	X	1	1
1	X	X	X	X	0	0	0

Interrupt logic:

Interrupts can be generated using the INT pin. Three events can trigger INT high. Each event has its own mode bit associated with it for masking or enabling these interupts. The following table outlines operation of the INT pin.

MODE1(7) = 1 and TDO shifter/buffer not full	MODE1(6) = 1 and TD1 shifter/buffer not empty	MODE1(5) = 1 and CNT32 not loaded, or at terminal count	INT
1	X	X	1
X	1	X	1
X	X	1	1
0	0	0	0

FIGURE 3. Parallel processor interface - Continued.

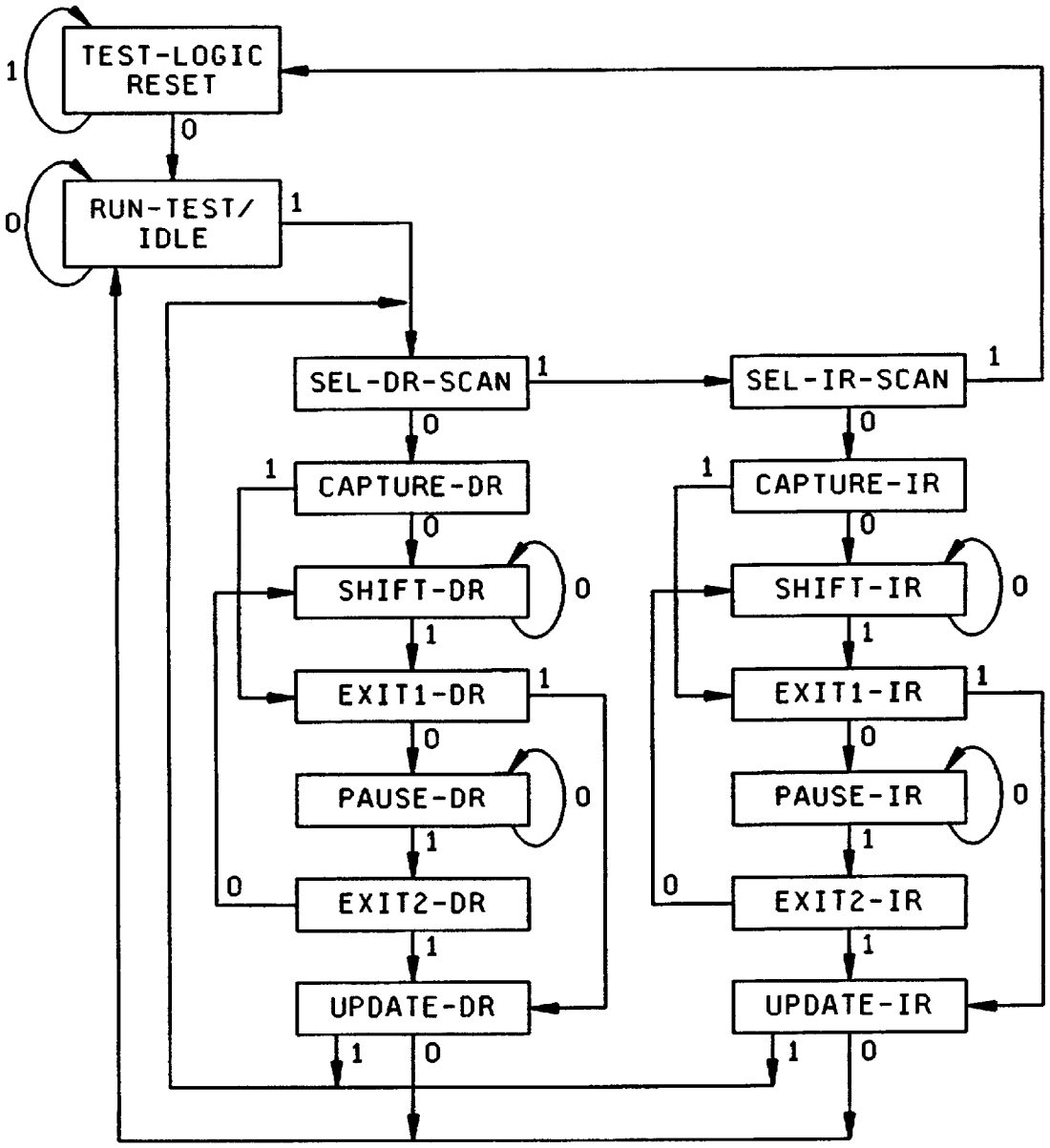


FIGURE 4. TAP controller state diagram.

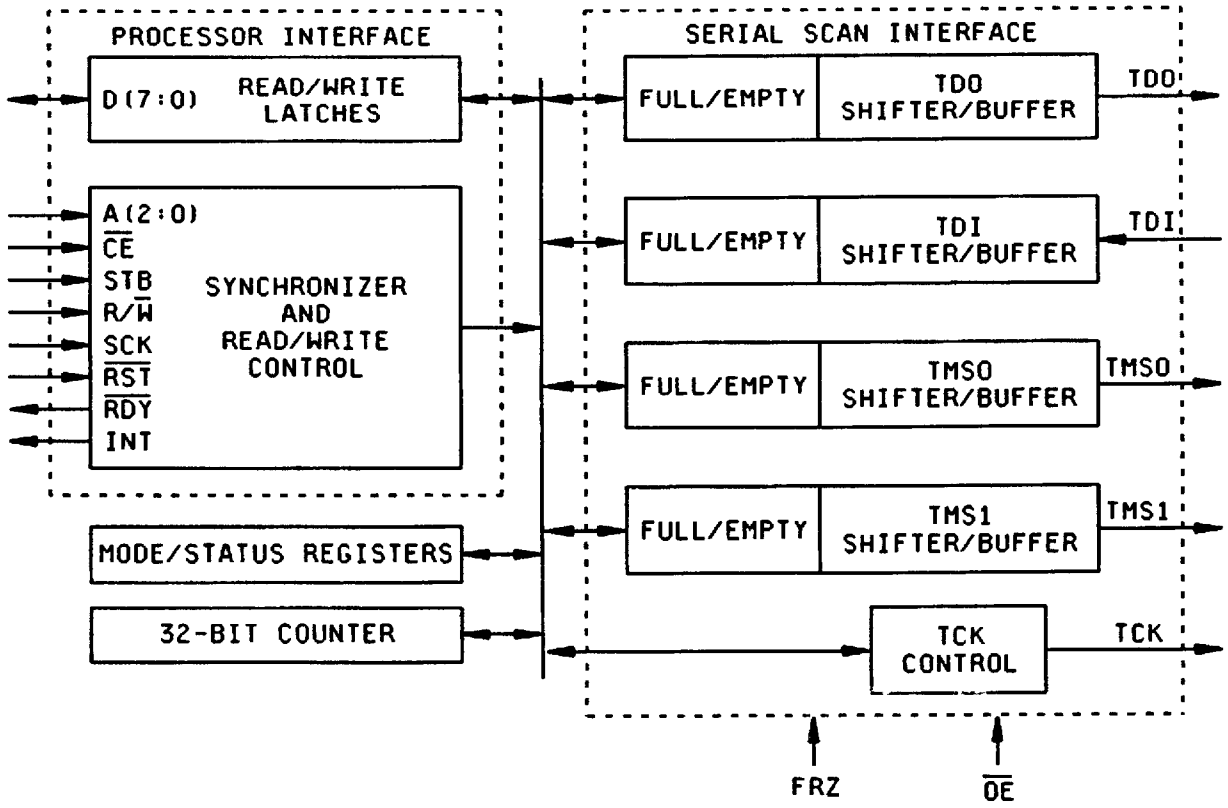
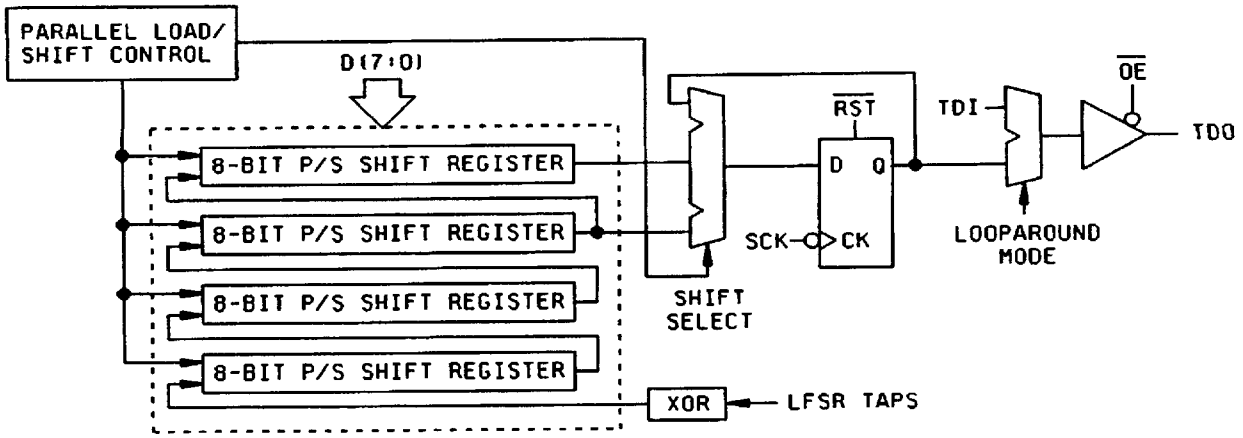


FIGURE 5. Block diagrams.

TDO shifter/buffer register hookup



TDO psuedo random pattern generator

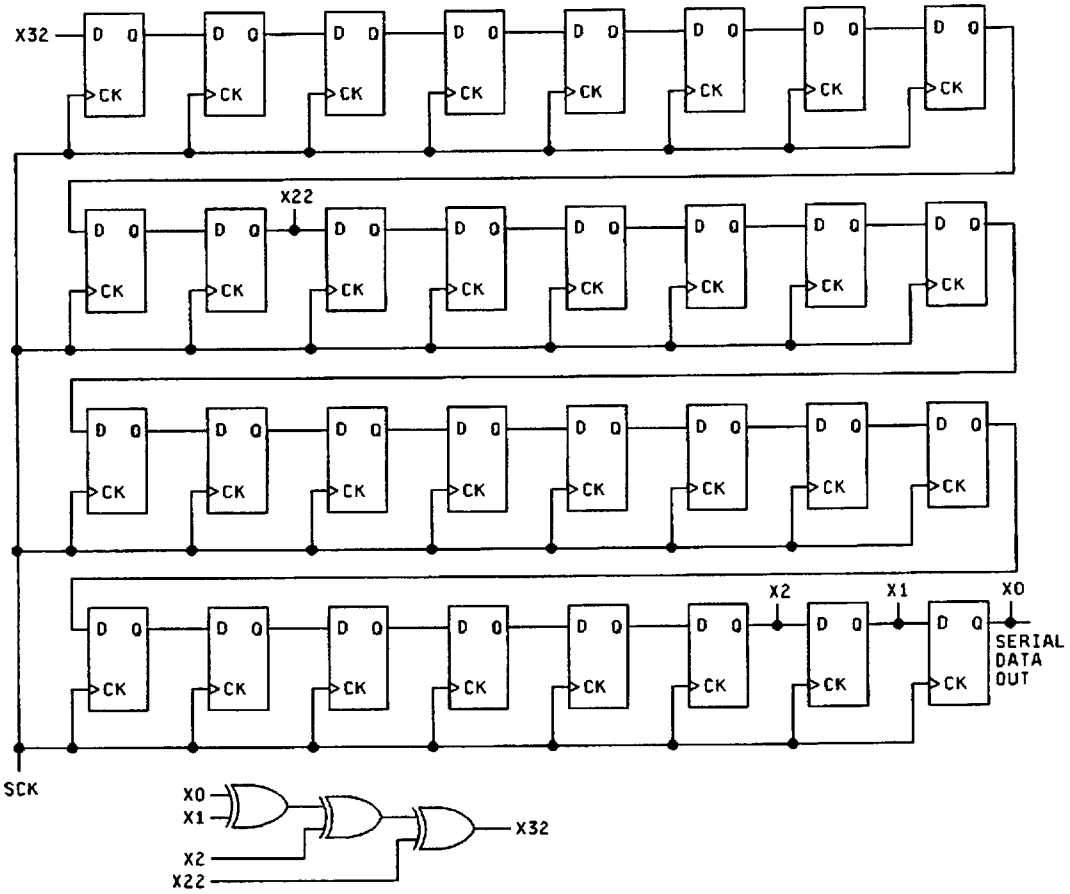


FIGURE 5. Block diagrams - Continued.

STANDARD MICROCIRCUIT DRAWING DEFENSE ELECTRONICS SUPPLY CENTER DAYTON, OHIO 45444	SIZE A		5962-94750
		REVISION LEVEL	SHEET 22

DESC FORM 193A
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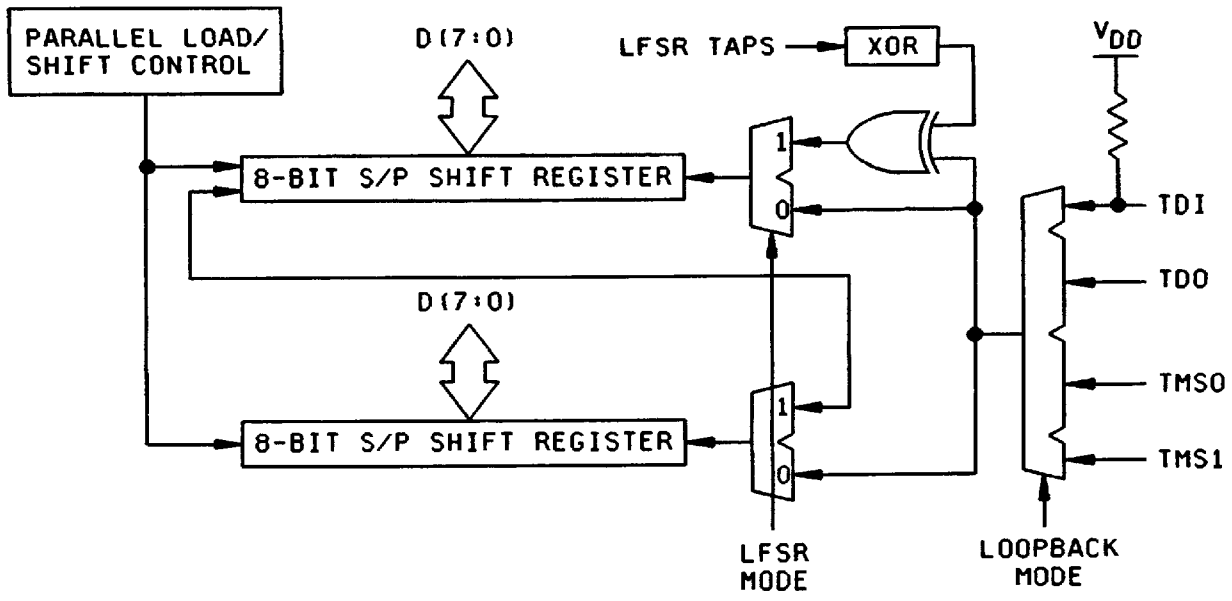
9004708 0009488 904

TDI shifter/buffer



TDI serial signature compactor

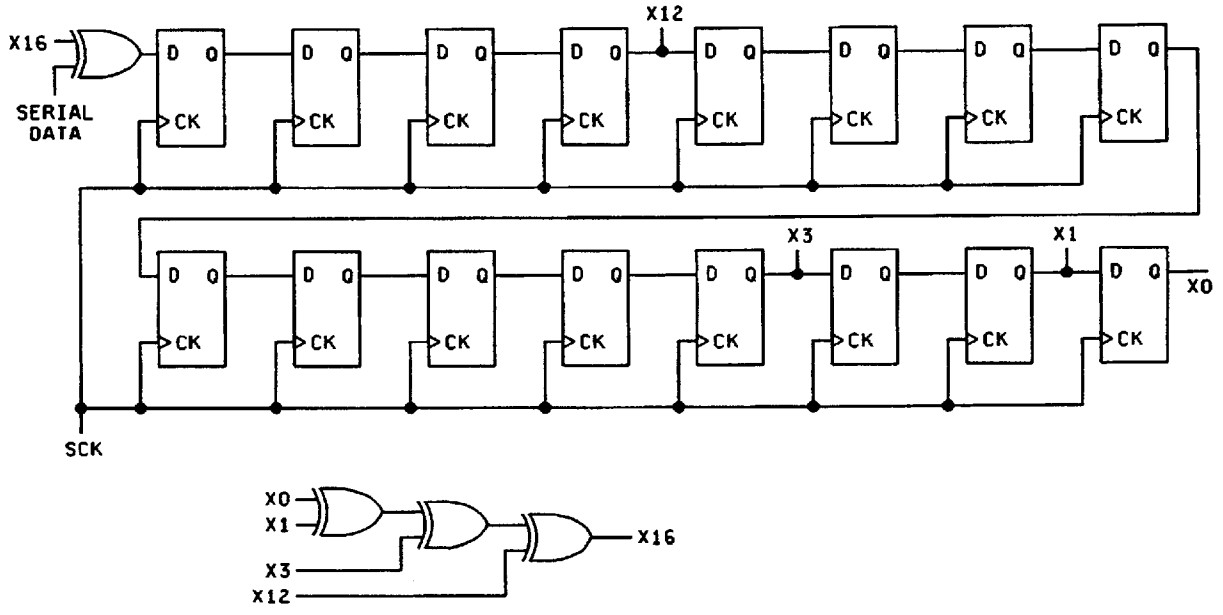


FIGURE 5. Block diagrams - Continued.

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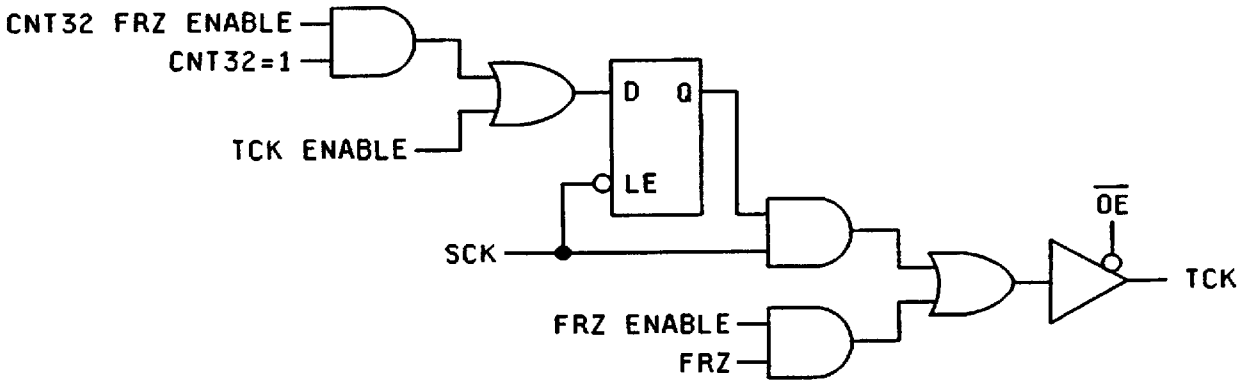
		REVISION LEVEL	SHEET 23

TCK logic



TMS shifter/buffer

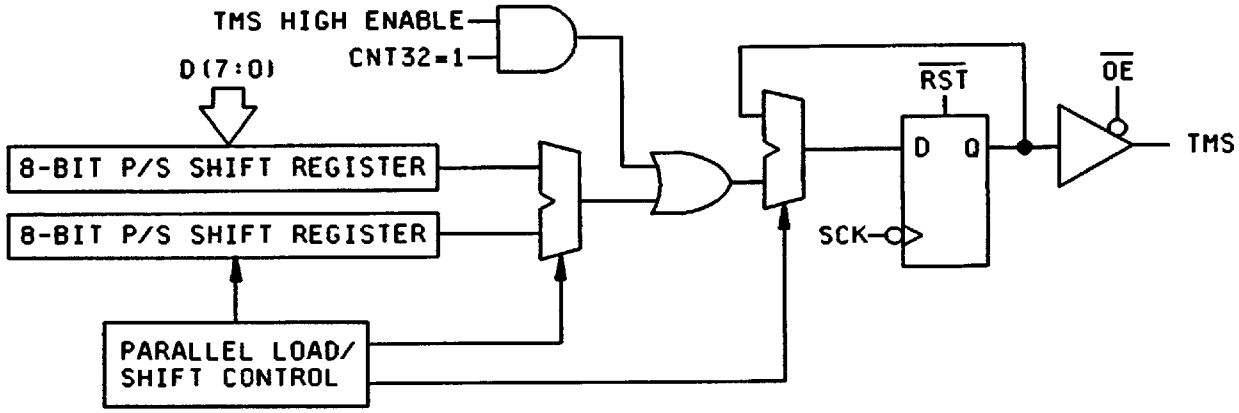


FIGURE 5. Block diagrams - Continued.

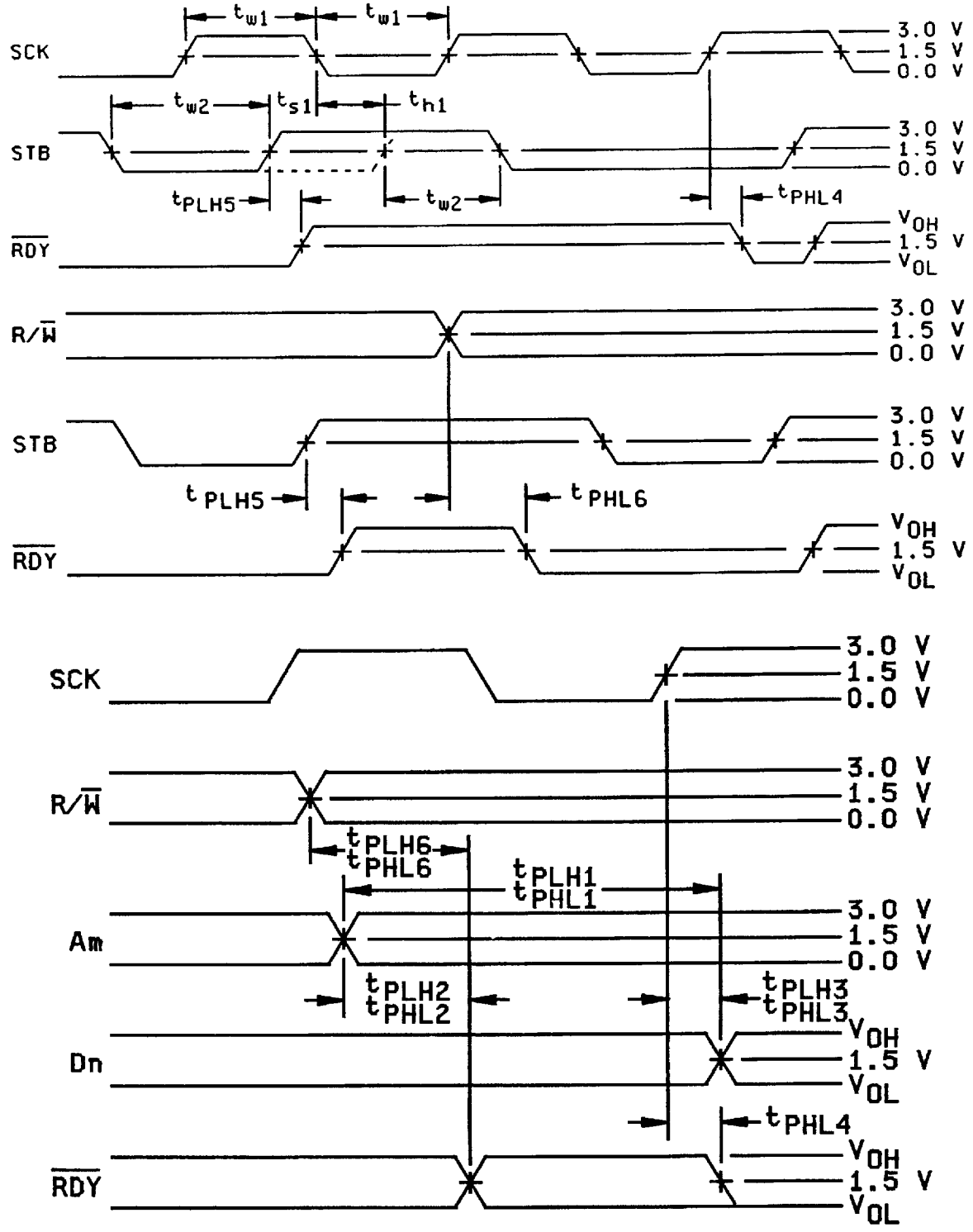
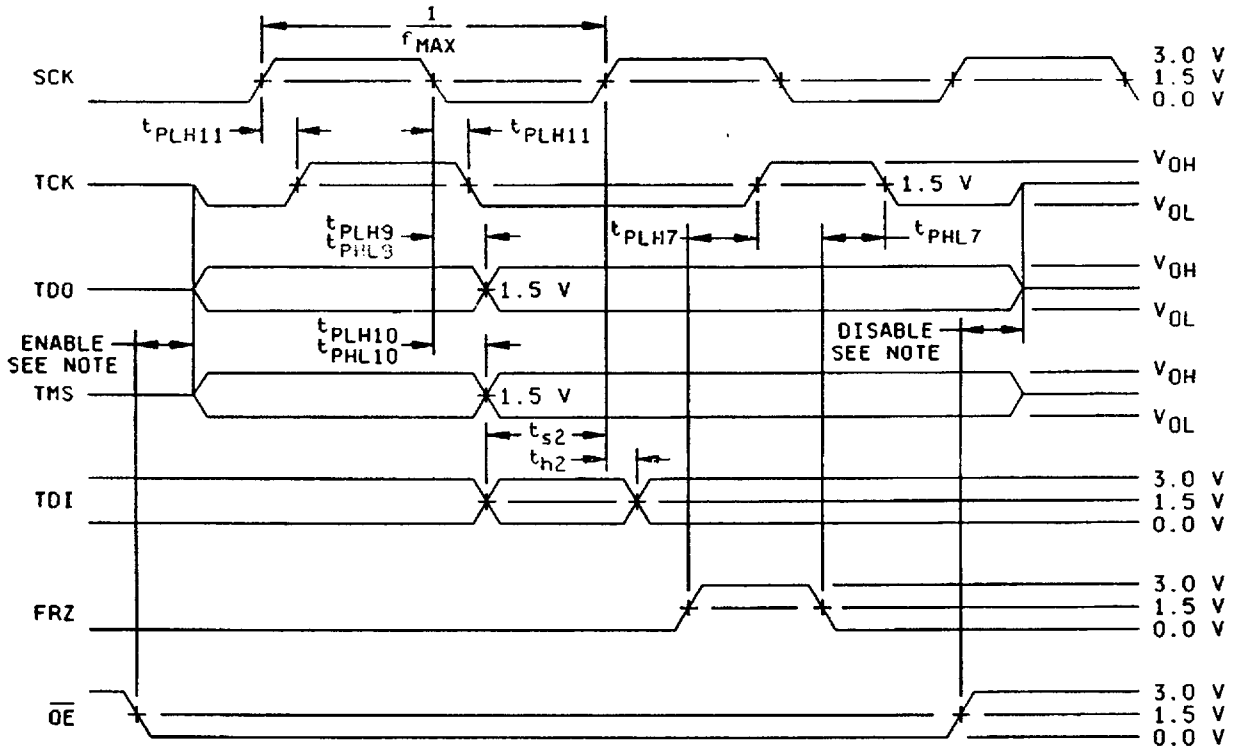


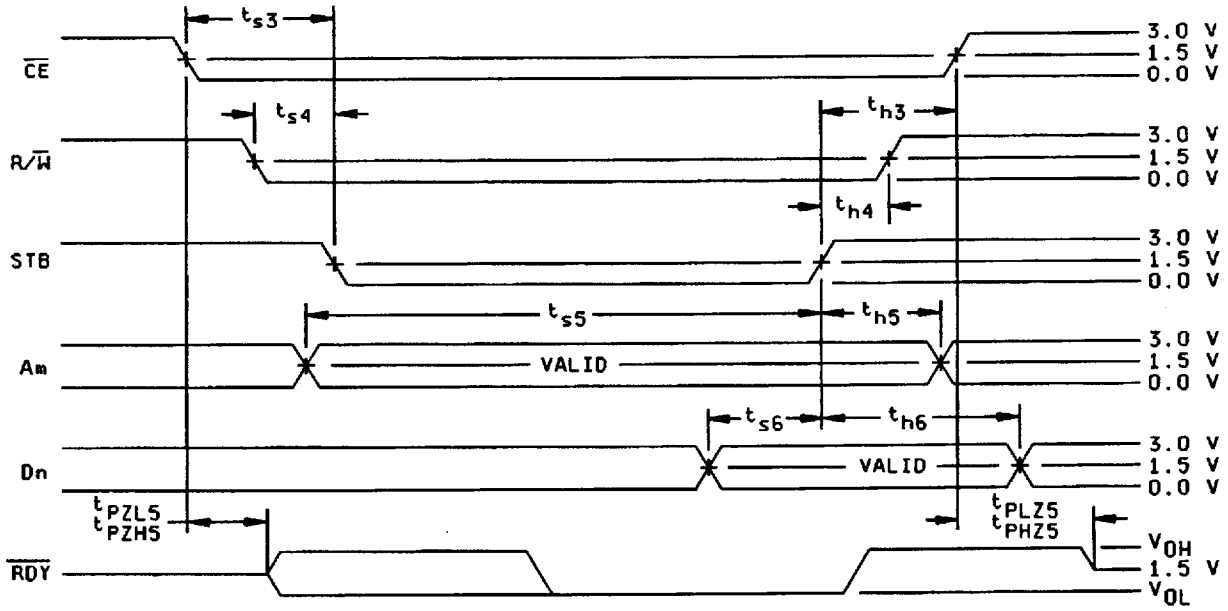
FIGURE 6. Synchronizer and consecutive read/write timing waveforms.



NOTE: Enable = t_{PZL1}, t_{PZH1}, t_{PZL2}, t_{PZH2}, t_{PZL3}, t_{PZH3}, t_{PZL4} and t_{PZH4}.
Disable = t_{PLZ1}, t_{PHZ1}, t_{PLZ2}, t_{PHZ2}, t_{PLZ3}, t_{PHZ3}, t_{PLZ4} and t_{PHZ4}.

FIGURE 7. Serial scan interface timing waveforms.

Write cycle



Read cycle

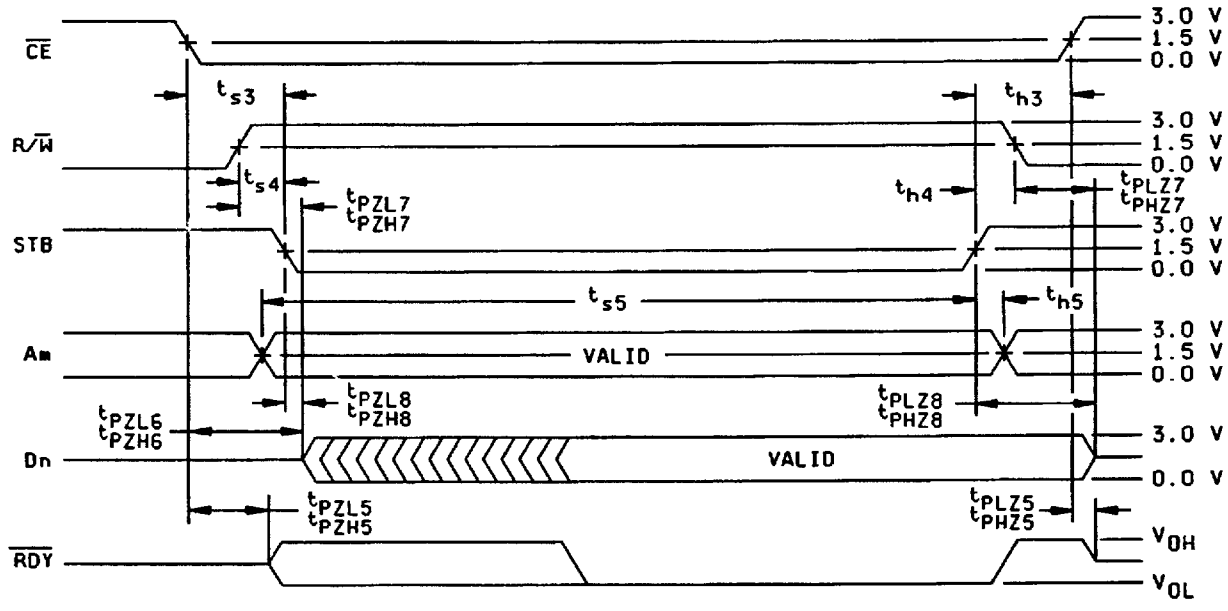


FIGURE 8. Write cycle, read cycle timing waveforms.

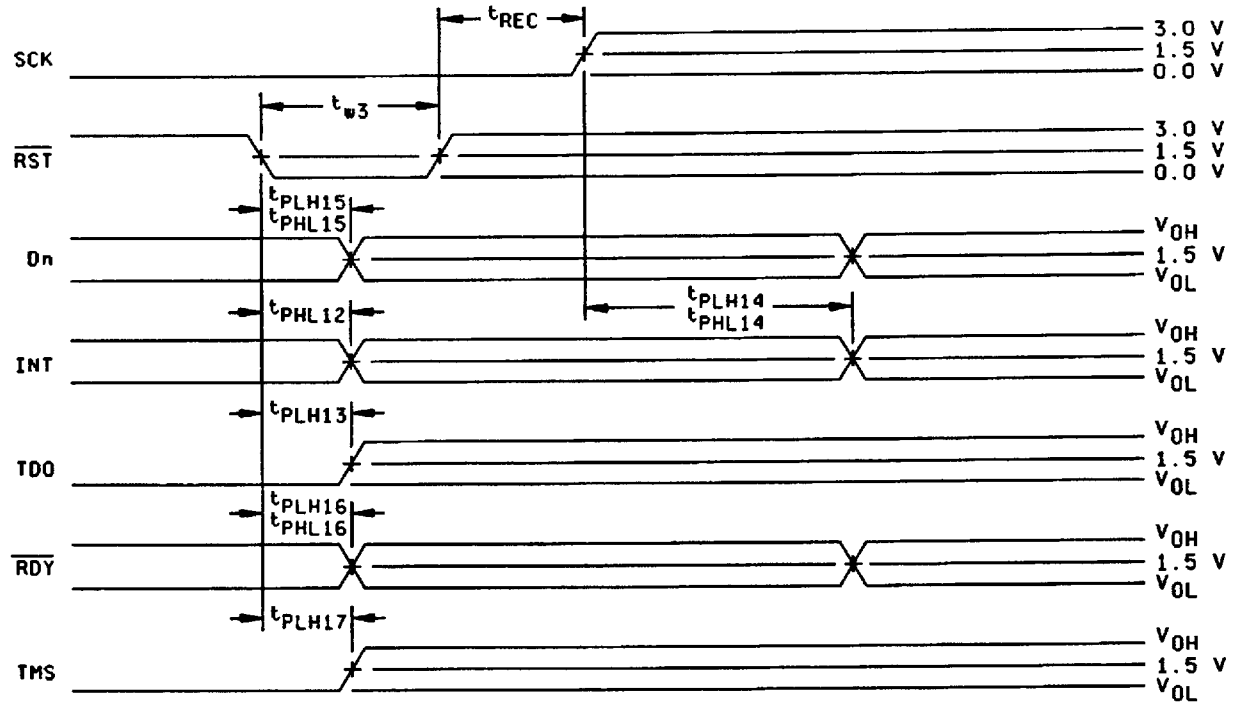
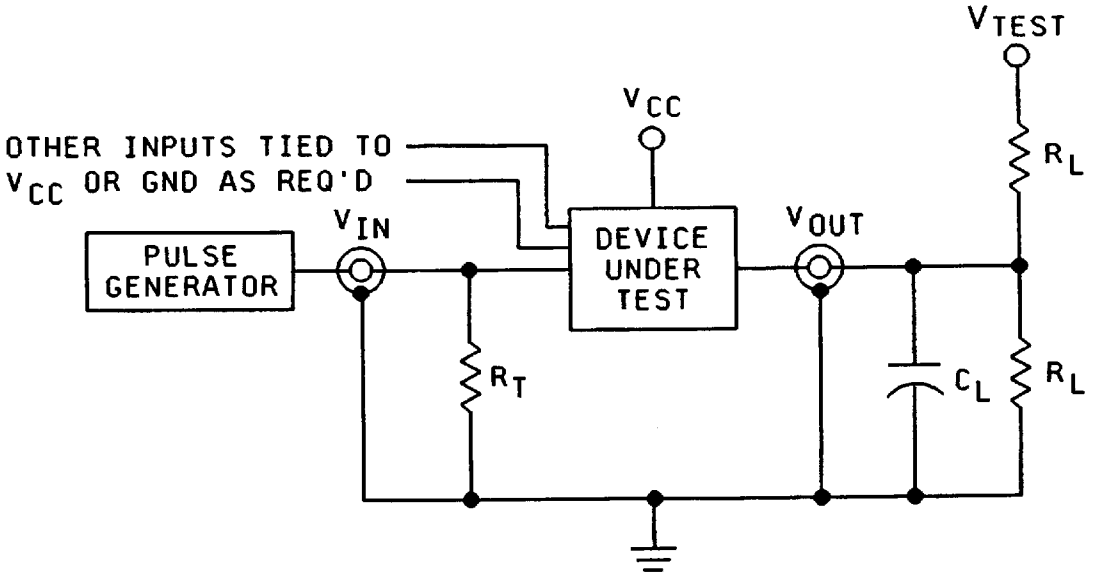


FIGURE 9. Reset and interrupt timing waveforms.



NOTES:
1. When measuring t_{PLZ} and t_{PZL}: V_{TEST} = 7.0 V.
2. When measuring t_{PHZ}, t_{PZH}, t_{PLH} and t_{PHL}: V_{TEST} = open.
3. The t_{PZL} and t_{PLZ} reference waveform is for the output under test with internal conditions such that the output is at V_{OL} except when disabled by the output enable control. The t_{PZH} and t_{PHZ} reference waveform is for the output under test with internal conditions such that the output is at V_{OH} except when disabled by the output enable control.
4. C_L = 50 pF minimum or equivalent (includes test jig and probe capacitance).
5. R_L = 500Ω or equivalent.
6. R_T = 50Ω or equivalent.
7. Input signal from pulse generator: V_{IN} = 0.0 V to 3.0 V; PRR ≤ 10 MHz; t_r ≤ 2.5 ns; t_f ≤ 2.5 ns; t_r and t_f shall be measured from 0.3 to 2.7 V and 2.7 V to 0.3 V, respectively; duty cycle = 50 percent.
8. Timing parameters shall be tested at a minimum input frequency of 1 MHz.
9. The outputs are measured one at a time with one transition per measurement.

FIGURE 10. Test circuit.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device class M, sampling and inspection procedures shall be in accordance with MIL-STD-883 (see 3.1 herein). For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-I-38535 and the device manufacturer's QM plan.

4.2 Screening. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. For device classes Q and V, screening shall be in accordance with MIL-I-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-I-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in appendix B of MIL-I-38535.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-I-38535. Inspections to be performed shall be those specified in MIL-I-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.3.1 Electrostatic discharge sensitivity qualification inspection. Electrostatic discharge sensitivity (ESDS) testing shall be performed in accordance with MIL-STD-883, method 3015. ESDS testing shall be measured only for initial qualification and after process or design changes which may affect ESDS classification.

4.4 Conformance inspection. Quality conformance inspection for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein) and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4). Technology conformance inspection for classes Q and V shall be in accordance with MIL-I-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-I-38535 permits alternate in-line control testing.

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. C_{IN}, C_{OUT}, and C_{PD} shall be measured only for initial qualification and after process or design changes which may affect capacitance. C_{IN} and C_{OUT} shall be measured between the designated terminal and GND at a frequency of 1 MHz. C_{PD} shall be tested in accordance with the latest revision of JEDEC Standard No. 20 and table I, herein. For C_{IN}, C_{OUT}, and C_{PD}, test all applicable pins on five devices with zero failures.

For C_{IN}, C_{OUT}, and C_{PD}, a device manufacturer may qualify devices by functional groups. A specific functional group shall be composed of function types, that by design, will yield the same capacitance values when tested in accordance with table I, herein. The device manufacturer shall set a function group limit for the C_{IN}, C_{OUT}, and C_{PD} tests. The device manufacturer may then test one device functional group, to the limits and conditions specified herein. All other device functions in that particular functional group shall be guaranteed, if not tested, to the limits and test conditions specified in table I, herein. The device manufacturers shall submit to DESC-EC the device functions listed in each functional group and the test results for each device tested.

c. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the functionality of the device. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A, B, C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB, in accordance with MIL-I-38535, and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes Q and V shall be M, D, R, and H and for device class M shall be M and D.

a. End-point electrical parameters shall be as specified in table II herein.

b. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-I-38535, appendix A, for the RHA level being tested. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-I-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, TM 5005, table I)	Subgroups (in accordance with MIL-I-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)		1	1
Final electrical parameters (see 4.2)	1/ 1,2,3,7,8,9	1/ 1,2,3,7,8,9	2/ 1,2,3,7,8,9
Group A test requirements (see 4.4)	1,2,3,4,7,8,9, 10,11	1,2,3,4,7,8,9, 10,11	1,2,3,4,7,8,9, 10,11
Group C end-point electrical parameters (see 4.4)	1,2,3	1,2,3	1,2,3
Group D end-point electrical parameters (see 4.4)	1,2,3	1,2,3	1,2,3
Group E end-point electrical parameters (see 4.4)	1,7,9	1,7,9	1,7,9

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1 and 7.

4.5 Methods of inspection. Methods of inspection shall be specified as follows:

4.5.1 Voltage and current. Unless otherwise specified, all voltages given are referenced to the microcircuit GND terminal. Currents given are conventional current and positive when flowing into the referenced terminal.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-STD-883 (see 3.1 herein) for device class M and MIL-I-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and which SMD's are applicable to that system. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DESC-EC, telephone (513) 296-6047.

6.4 Comments. Comments on this drawing should be directed to DESC-EC, Dayton, Ohio 45444-5270, or telephone (513) 296-5377.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-I-38535 and MIL-STD-1331 and as follows:

GND	Ground zero voltage potential.
I_{CC}	Quiescent supply current.
I_{IL}	Input current low.
I_{IH}	Input current high.
T_C	Case temperature.
T_A	Ambient temperature.
V_{CC}	Positive supply voltage.
C_{IN}	Input terminal-to-GND capacitance.
C_{OUT}	Output terminal-to-GND capacitance.
C_{PD}	Power dissipation capacitance.
V_{IC+}	Positive input clamp voltage.
V_{IC-}	Negative input clamp voltage.

6.6 One part - one part number system. The one part - one part number system described below has been developed to allow for transitions between identical generic devices covered by the three major microcircuit requirements documents (MIL-H-38534, MIL-I-38535, and 1.2.1 of MIL-STD-883) without the necessity for the generation of unique PIN's. The three military requirements documents represent different class levels, and previously when a device manufacturer upgraded military product from one class level to another, the benefits of the upgraded product were unavailable to the Original Equipment Manufacturer (OEM), that was contractually locked into the original unique PIN. By establishing a one part number system covering all three documents, the OEM can acquire to the highest class level available for a given generic device to meet system needs without modifying the original contract parts selection criteria.

Military documentation format	Example PIN under new system	Manufacturing source listing	Document listing
New MIL-H-38534 Standard Microcircuit Drawings	5962-XXXXXZZ(H or K)YY	QML-38534	MIL-BUL-103
New MIL-I-38535 Standard Microcircuit Drawings	5962-XXXXXZZ(Q or V)YY	QML-38535	MIL-BUL-103
New 1.2.1 of MIL-STD-883 Standard Microcircuit Drawings	5962-XXXXXZZ(M)YY	MIL-BUL-103	MIL-BUL-103

6.7 Sources of supply.

6.7.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DESC-EC and have agreed to this drawing.

6.7.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-EC.