	REVISIONS		
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add device class N and plastic small outlines X and Y. Make changes to 1.2.3, 1.2.4, 1.3, table I, figure 1, figure 2, and table II.	95-07-20	M. A. FRYE
В	Add device types 03 and 04. Technical and editoral changes throughout.	96-02-02	M. A. FRYE
С	Add case outlines X and Y to device types 03 and 04. Make changes to 1.2.6 and editorial changes throughout ro	97-10-20	R. MONNIN
D	Make change to device type 03 manufacturers PIN as specified under 1.2.6 ro	97-11-14	R. MONNIN

THE ORIGINAL FIRST SHEET OF THIS DRAWING HAS BEEN REPLACED.

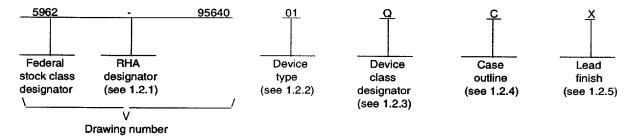
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STANDARD MICROCIRCUIT DRAWING	CHECKED B RAJESH P					COLUMBUS, OHIO 43216										
THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS	APPROVED RAYMOND		N			MICROCIRCUIT, LINEAR, DUAL/QUAD, RAIL- TO-RAIL, LOW POWER, OPERATIONAL					-					
AND AGENCIES OF THE DEPARTMENT OF DEFENSE	DRAWING A	APPROV	AL D	ATE		AM	PLIF	IER,	MON	OLIT	HIC	SILIC	ON			
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DSCC FORM 2233
APR 97
DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

- 1.1 <u>Scope</u>. This drawing documents three product assurance class levels consisting of high reliability (device classes Q and M), space application (device class V), and non traditional performance environment (device class N). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.
 - 1.2 PIN. The PIN is as shown in the following example:



- 1.2.1 RHA designator. Device classes N, Q, and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.
 - 1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	TLC2252	Rail-to-rail, very low power, dual, operational amplifier
02	TLC2254	Rail-to-rail, very low power, quad, operational amplifier
03	TLC2252A	Rail-to-rail, very low power, dual, operational amplifier with enhanced V _{IO}
04	TLC2254A	Rail-to-rail, very low power, quad, operational amplifier with enhanced V _{IO}

1.2.3 <u>Device class designator</u>. The device class designator is a single letter identifying the product assurance level as follows:

Device class	<u>Device requirements documentation</u>
М	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
N	Certification and qualification to MIL-PRF-38535 with non-traditional performance environment (encapsulated in plastic)
Q or V	Certification and qualification to MIL-PRF-38535

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-95640
DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000		REVISION LEVEL C	SHEET 2

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style	Document
С	GDIP1-T14 or CDIP2-T14	14	Dual-in-line	MIL-STD-1835
D	GDFP1-F14 or CDFP2-F14	14	Flat pack	MIL-STD-1835
H	GDFP1-F10 or CDFP2-F10	10	Flat pack	MIL-STD-1835
Р	GDIP1-T8 or CDIP2-T8	8	Dual-in-line	MIL-STD-1835
X	MS-012AA	8	Plastic small outline	JEP-95
Υ	MS-012AB	14	Plastic small outline	JEP-95
2	CQCC1-N20	20	Square leadless chip carrier	MIL-STD-1835

1.2.5 <u>Lead finish</u>. The lead finish is as specified in MIL-PRF-38535 for device classes N, Q, and V or MIL-PRF-38535, appendix A for device class M.

1.2.6 <u>Device class N manufacturer PIN</u>. For device class N, plastic encapsulated microcircuits (PEMs) the following manufacturer PIN (see 3.5.1 herein) shall be marked:

Standard Microcircuit 1/	Manufacturer
Drawing PIN	PIN
5962-9564001NXD	2252M
5962-9564002NYD	TLC2254M
5962-9564003NXD	2252A
5962-9564004NYD	TLC2254AM

1.3 Absolute maximum ratings. 2/

Supply voltage range (VDD)	-8.0 V dc to +8.0 V dc 3/
Differential input voltage (VID)	
Input voltage range (VIN)	-VDD - 0.3 V to +VDD 3/
Input current, each input (I _{IN})	.+5.0 mA to -5.0 mA
Output current (IOUT)	+50.0 mA to -50.0 mA
Total current into +V _{DD}	
Total current into -V _{DD}	+50.0 mA to -50.0 mA
Duration of short circuit current at or below +25°C	.Unlimited <u>5</u> /
Operating free-air temperature range (T _A)	55°C to +125°C
Storage temperature range (Tstg)	
Lead temperature (soldering 10 seconds)	
Maximun junction temperature (T _J)	.+150°C
Maximum power dissipation (P _D): 6/	
Cases C and 2	. 1375 mW
Case D and H	.700 mW
Case P	. 1050 mW
Case X	.725 mW
Case Y	.950 mW
Thermal resistance, junction-to-case (O _{JC}):	
Cases C, D, H, P, 2	.See MIL-STD-1835

- 1/ The SMD PIN is provided for cross reference information, see 3.5.2 herein.
- 2/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
- 3/ All voltage values, except differential voltages, are with respect to the midpoint between +Vpb and -Vpb.
- 4/ Differential voltages are at the noninverting input with respect to the inverting input. Excessive current flows if the input is brought below -V_{DD} -0.3 V.
- 5/ The output may be shorted to either supply. Temperature and/or supply voltages must be limited to ensure that the maximum dissipation rating is not exceeded.
- 6/ Above T_A = +25°C, derate by the following factors; cases C and 2 at 11.0 mW/°C, cases D and H at 5.5 mW/°C, case P at 8.4 mW/°C, case X at 5.8 mW/°C, and case Y at 7.6 mW/°C.

STANDARD MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS	SIZE A		5962-95640
DEFENSE SUPPLY CENTER COLUMBUS		REVISION LEVEL	SHEET
COLUMBUS, OHIO 43216-5000		C	3

1.4 Recommended operating conditions.

2. APPLICABLE DOCUMENTS

2.1 <u>Government specification, standards, and handbooks</u>. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Method Standard Microcircuits.

MIL-STD-973 - Configuration Management.

MIL-STD-1835 - Interface Standard For Microcircuit Case Outlines.

HANDBOOKS

DEPARTMENT OF DEFENSE

MIL-HDBK-103 - List of Standard Microcircuit Drawings (SMD's).

MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 <u>Non-Government publications</u>. The following documents form a part of this drawing and the references cited herein. Unless otherwise specified, the issues of the documents which are DoD adopted are those listed in the issue of the DODISS cited in the solicitation. Unless otherwise specified, the issues of documents not listed in the DODISS are the issues of the documents cited in the solicitation.

ELECTRONIC INDUSTRIES ASSOCIATION (EIA)

JEDEC Publication 95 - Registered and Standard Outlines for Semiconductor Devices

(Application for copies should be addressed to the Electronic Industries Association, 2500 Wilson Boulevard, Arlington, VA 22201-3834).

(Non-Government standards and other publications are normally available from the organization that prepare or distribute the documents. These documents also may be available in or through libraries or other informational services).

2.3 <u>Order of precedence</u>. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

	SIZE A		5962-95640
DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000		REVISION LEVEL C	SHEET 4

DSCC FORM 2234

3. REQUIREMENTS

- 3.1 Item requirements. The individual item requirements for device classes N, Q, and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.
- 3.2 <u>Design, construction, and physical dimensions</u>. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes N, Q, and V or MIL-PRF-38535, appendix A and herein for device class M.
 - 3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein.
 - 3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.
- 3.3 <u>Electrical performance characteristics and postirradiation parameter limits</u>. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full ambient operating temperature range.
- 3.4 <u>Electrical test requirements</u>. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.
- 3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.
- 3.5.1 <u>Certification/compliance mark</u>. The certification mark for device classes N, Q, and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.
- 3.5.2 Marking for device class N. For PEM packages the SMD PIN in 1.2 herein and the MIL-PRF-38535 marking is not required. Marking on the device shall include; a traceable data code, country of origin, pin one indicator and manufacturers identification. In addition, the QML certification mark and the manufacturer PIN as shown in 1.2.6 herein shall be marked on the topside of the package. Manufacturer may at their option place QML certification mark adjacent to the manufacturer pin. In all cases, the purchase order shall reflect the SMD PIN as shown 1.2 herein.
- 3.6 <u>Certificate of compliance</u>. For device classes N, Q, and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes N, Q, and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.
- 3.7 <u>Certificate of conformance</u>. A certificate of conformance as required for device classes N, Q, and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.
- 3.8 <u>Notification of change for device class M</u>. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-973.
- 3.9 <u>Verification and review for device class M.</u> For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.
- 3.10 <u>Microcircuit group assignment for device class M</u>. Device class M devices covered by this drawing shall be in microcircuit group number 49 (see MIL-PRF-38535, appendix A).

STANDARD MICROCIRCUIT DRAWING	SIZE A		5962-95640
DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000		REVISION LEVEL C	SHEET 5

DSCC FORM 2234

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55^{\circ}\text{C} \le T_{A} \le +125^{\circ}\text{C}$ unless otherwise specified	Group A <u>1</u> / subgroups	Device type	Limits	Unit	
				3.	Min	Max	1
Input offset voltage	Vio	$V_{DD} = \pm 2.5 \text{ V}, V_{IC} = 0 \text{ V},$	1	01,02		1500	μV
		Rs = 50 Ω , Vout = 0 V		03,04		850	
			2,3	01,02		1750	
			!	03,04		1000	
		$V_{DD} = \pm 5 \text{ V}, V_{IC} = 0 \text{ V},$	1	01,02		1500	
	'	$R_S = 50 \Omega$, $V_{OUT} = 0 V$	1	03,04		850	
	'		2,3	01,02		1750	
	1		!	03,04		1000	
Input offset current	lo lo	$V_{DD} = \pm 2.5 \text{ V}, V_{IC} = 0 \text{ V},$	2	All		500	pA
		$R_S = 50 \Omega, V_{OUT} = 0 V,$ $T_A = +125^{\circ}C$					
	1	$V_{DD} = \pm 5 \text{ V}, V_{IC} = 0 \text{V},$	1	1		500	
	1	$R_S = 50 \Omega$, $V_{OUT} = 0 V$,	1			1	
	<u> </u>	T _A = +125°C	'	(!		1 '	
Input bias current	Ìв	$V_{DD} = \pm 2.5 \text{ V}, V_{IC} = 0 \text{V},$	2	All		500	pΑ
	'	$R_S = 50 \Omega$, $V_{OUT} = 0 V$,		1	, ,	1 1	
	'	T _A = +125°C] '	1	L	<u> </u>	1
	'	$V_{DD} = \pm 5 \text{ V}, V_{IC} = 0 \text{V},$] !	1		500	ĺ
		$R_S = 50 \Omega$, $V_{OUT} = 0 V$,		1	1	1 1	1
		T _A = +125°C	<u> </u>				L
Common-mode input	Vica	$V_{DD} = 5 \text{ V, } V_{IO} \le 5 \text{ mV,}$	1	All	0 to 4	لــــــــــــــــــــــــــــــــــــــ	٧
voltage range	1	Rs = 50 Ω	2,3		0 to 3.5	L	i
		$V_{DD} = \pm 5 \text{ V}, V_{DO} \le 5 \text{ mV},$	1		-5 to 4		i
		$R_S = 50 \Omega$	2,3		-5 to 3.5		i
High level output voltage	Vон	$V_{DD} = 5 \text{ V}, V_{IC} = 2.5 \text{ V},$	1	All	4.9		٧
		lo _H = -75 μA	2,3	<i>i</i>	4.8		i
	1	$V_{DD} = 5 \text{ V}, V_{IC} = 2.5 \text{ V},$	1	1	4.8		i
	·	lo _H = -150 μA	1 1	ı	,		i

See footnotes at end of table.

STANDARD MICROCIRCUIT DRAWING	SIZE A		5962-95640
DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000		REVISION LEVEL C	SHEET 6

TABLE I. <u>Electrical performance characteristics</u> - Continued.

Test	Symbol	Conditions -55°C ≤ T _A ≤ +125°C unless otherwise specified	Group A <u>1</u> / subgroups	Device type	Limits	; <u>2</u> /	Unit
					Min	Max	
Low level output voltage	Vol.	V _{DD} = 5 V, V _{IC} = 2.5 V, I _{OL} = 500 μA	1,2,3	All		0.15	٧
		$V_{DD} = 5 \text{ V}, V_{IC} = 2.5 \text{ V},$	1			1.0	
		lou = 4 mA	2,3			1.2	
Maximum positive peak	+Vom	$V_{DD} = \pm 5 \text{ V}, V_{IC} = 0 \text{ V},$	1	All	4.9		٧
output voltage swing		louτ = -100 μA	2,3		4.7		
		V _{DD} = ±5 V, V _{IC} = 0 V, louτ = -200 μA	1		4.8		
Maximum negative peak output voltage swing	-V _{OM}	V _{DD} = ±5 V, V _{IC} = 0 V, lout = 500 μA	1,2,3	All	-4.85		٧
- spar rolling		$V_{DD} = \pm 5 \text{ V}, V_{IC} = 0 \text{ V},$	1	 	-4.0	 	
		lout = 4 mA	2.3		-3.8	 	
Large signal differential	AVD	$V_{DD} = 5 \text{ V}, \text{ V}_{IC} = 2.5 \text{ V},$	1	All	100	 	V/mV
voltage amplification	_	V _{OUT} = 1 V to 4 V,	2,3	1 · · · · · · · · · · · · · · · · · · ·	10	 	
- ·		$R_L = 100 \text{ k}\Omega 3/$					
		$V_{DD} = \pm 5 \text{ V}, V_{IC} = 0 \text{ V},$	1	1	40		
		$V_{OUT} = \pm 4 V$,	2,3	1	10		
		$R_L = 100 \text{ k}\Omega$					
Common mode rejection	CMRR	$V_{DD} = 5 \text{ V, V}_{OUT} = 2.5 \text{ V,}$	1,2,3	All	70		dB
ratio		V _{IC} = 0 V to 2.7 V,					
		Rs = 50 Ω]				
		$V_{DD} = \pm 5 \text{ V}, V_{OUT} = 0 \text{ V},$			75]
		$V_{IC} = -5 \text{ V to } 2.7 \text{ V},$					
		$R_S = 50 \Omega$					
Supply voltage rejection	k _{svR}	$\pm V_{DD} = \pm 2.2 \text{ V to } \pm 8 \text{ V},$	1,2,3	All	80		dB
ratio (ΔV _{DD} / ΔV _{IO})		no load					
Supply current	loo	$V_{DD} = 5 \text{ V}, V_{OUT} = 2.5 \text{ V},$	1,2,3	01,03		125	μА
(both channels)		no load	1	02,04		250	
		$V_{DD} = \pm 5 \text{ V}, V_{OUT} = 0 \text{ V},$		01,03		125	
		no load		02,04		250	

See footnotes at end of table.

STANDARD MICROCIRCUIT DRAWING	SIZE A		5962-95640
DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000		REVISION LEVEL C	SHEET 7

DSCC FORM 2234

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions -55°C ≤ T _A ≤ +125°C unless otherwise specified	Group A <u>1</u> / subgroups	Device type	Limits	s <u>2</u> /	Unit
					Min	Max	
Slew rate at unity gain	SR	V _{DD} = 5 V, <u>3</u> /	4	Ali	0.07		V/µs
		Vout = 1.25 V to 2.75 V,	5,6		0.05		
		$R_L = 100 \text{ k}\Omega$, $C_L = 100 \text{ pF}$	ŀ				
		$V_{DD} = \pm 5 V$,	4		0.07		
		Vout = ±1.0 V,	5,6		0.05		
		$R_L = 100 \text{ k}\Omega$, $C_L = 100 \text{ pF}$					

- 1/ For device class N, subgroup 3 ($T_A = -55$ °C) test limits are guaranteed but not tested.
- 2/ The algebraic convention, whereby the most negative value is a minimum and the most positive is a maximum, is used in this table. Negative current shall be defined as conventional current flow out of a device terminal.
- 3/ Referenced to 2.5 V.

4. QUALITY ASSURANCE PROVISIONS

- 4.1 <u>Sampling and inspection</u>. For device classes N, Q, and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.
- 4.2 <u>Screening</u>. For device classes N, Q, and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

- a. Burn-in test, method 1015 of MIL-STD-883.
 - (1) Test condition B or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.
 - (2) $T_A = +125^{\circ}C$, minimum.
- b. Interim and final electrical test parameters shall be as specified in table II herein.

STANDARD MICROCIRCUIT DRAWING	SIZE A		5962-95640
DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000		REVISION LEVEL C	SHEET 8

DSCC FORM 2234

Device types		01, 03		02,	04
Case outlines	Н	P and X	2	C, D, and Y	2
Terminal number					
1	NC	OUTPUT 1	NC	OUTPUT 1	NC
2	OUTPUT 1	-INPUT 1	OUTPUT 1	-INPUT 1	OUTPUT 1
3	-INPUT 1	+INPUT 1	NC	+INPUT 1	-INPUT 1
4	+INPUT 1	-V _{DD} / GND	NC	+V _{DD}	+INPUT 1
5	-V _{DD} / GND	+INPUT 2	-INPUT 1	+INPUT 2	NC
6	+INPUT 2	-INPUT 2	NC	-INPUT 2	+V _{DD}
7	-INPUT 2	OUTPUT 2	+INPUT 1	OUTPUT 2	NC
8	OUTPUT 2	+V _{DD}	NC	OUTPUT 3	+INPUT 2
9	+V _{DD}		NC	-INPUT 3	-INPUT 2
10	NC		-V _{DD} / GND	+INPUT 3	OUTPUT 2
11			NC	-V _{DD} / GND	NC
12	•••		+INPUT 2	+INPUT 4	OUTPUT 3
13			NC	-INPUT 4	-INPUT 3
14	•••		NC	OUTPUT 4	+INPUT 3
15			-INPUT 2		NC
16			NC		-V _{DD} / GND
17			OUTPUT 2		NC
18			NC		+INPUT 4
19		***	NC		-INPUT 4
20			+V _{DD}		OUTPUT 4

NC = No connection

FIGURE 1. Terminal connections.

STANDARD MICROCIRCUIT DRAWING	SIZE A		5962-95640
DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000		REVISION LEVEL C	SHEET 9

DSCC FORM 2234

4.2.2 Additional criteria for device classes N, Q, and V.

- a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.
- b. Interim and final electrical test parameters shall be as specified in table II herein.
- Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.
- 4.3 Qualification inspection for device classes N, Q, and V. Qualification inspection for device classes N, Q, and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).
- 4.4 Conformance inspection. Technology conformance inspection for classes N, Q, and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-PRF-38535 permits alternate in-line control testing. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).
 - 4.4.1 Group A inspection.
 - a. Tests shall be as specified in table II herein.
 - b. Subgroups 7, 8, 9, 10, and 11 in table I, method 5005 of MIL-STD-883 shall be omitted.
 - 4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.
 - 4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:
 - a. Test condition B or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.
 - b. $T_A = +125^{\circ} C$, minimum.
 - c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.
- 4.4.2.2 Additional criteria for device classes N, Q, and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.
 - 4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

STANDARD MICROCIRCUIT DRAWING	SIZE A		5962-95640
DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000		REVISION LEVEL C	SHEET 10

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)		
	Device class M	Device class N	Device class Q	Device class V
Interim electrical parameters (see 4.2)				
Final electrical parameters (see 4.2)	1,2,3,4,5,6 1/	1,2,3, <u>1</u> / 4,5,6	1,2,3, <u>1</u> / 4,5,6	1,2,3, <u>1</u> / 4,5,6
Group A test requirements (see 4.4)	1,2,3,4,5,6	1,2,3,4,5,6	1,2,3,4,5,6	1,2,3,4,5,6
Group C end-point electrical parameters (see 4.4)	1	1	1	1
Group D end-point electrical parameters (see 4.4)	1	1	1	1
Group E end-point electrical parameters (see 4.4)				

^{1/} PDA applies to subgroup 1 with the exception of V_{IO}.

- 4.4.4 <u>Group E inspection</u>. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).
 - a. End-point electrical parameters shall be as specified in table II herein.
 - b. For device classes N, Q, and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.
 - c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

5. PACKAGING

5.1 <u>Packaging requirements</u>. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes N, Q, and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

- 6.1 <u>Intended use</u>. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.
- 6.1.1 <u>Replaceability</u>. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.
 - 6.1.2 Substitutability. Device class Q devices will replace device class M devices.

STANDARD MICROCIRCUIT DRAWING	SIZE A		5962-95640
DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000		REVISION LEVEL C	SHEET 11

DSCC FORM 2234

- 6.2 <u>Configuration control of SMD's</u>. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.
- 6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0525.
- 6.4 <u>Comments</u>. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43216-5000, or telephone (614) 692-0674.
- 6.5 <u>Abbreviations, symbols, and definitions</u>. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.
 - 6.6 Sources of supply.
- 6.6.1 <u>Sources of supply for device classes N, Q, and V</u>. Sources of supply for device classes N, Q, and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.
- 6.6.2 <u>Approved sources of supply for device class M.</u> Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING	SIZE A		5962-95640
DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000		REVISION LEVEL C	SHEET 12

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 97-11-14

Approved sources of supply for SMD 5962-95640 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535.

Standard microcircuit drawing PIN <u>1</u> /	Vendor CAGE number	Vendor similar PIN <u>2</u> /
5962-9564001NXD	01295	TLC2252MDQ
5962-9564001QHA	01295	TLC2252MUB
5962-9564001QPA	01295	TLC2252MJGB
5962-9564001Q2A	01295	TLC2252MFKB
5962-9564002NYD	01295	TLC2254MDQ
5962-9564002QCA	01295	TLC2254MJB
5962-9564002QDA	01295	TLC2254MWB
5962-9564002Q2A	01295	TLC2254MFKB

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Page 1 of 2

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9564003NXD	01295	TLC2252AMDQ
5962-9564003QHA	01295	TLC2252AMUB
5962-9564003QPA	01295	TLC2252AMJGB
5962-9564003Q2A	01295	TLC2252AMFKB
5962-9564004NYD	01295	TLC2254AMDQ
5962-9564004QCA	01295	TLC2254AMJB
5962-9564004QDA	01295	TLC2254AMWB
5962-9564004Q2A	01295	TLC2254AMFKB

- 1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed, contact the vendor to determine its availability.
- 2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number Vendor name and address

01295

Texas Instruments Incorporated 13500 N. Central Expressway P.O. Box 655303 Dallas, TX 75265

Point of contact:

I-20 at FM 1788 Midland, TX 79711-0448

Page 2 of 2