

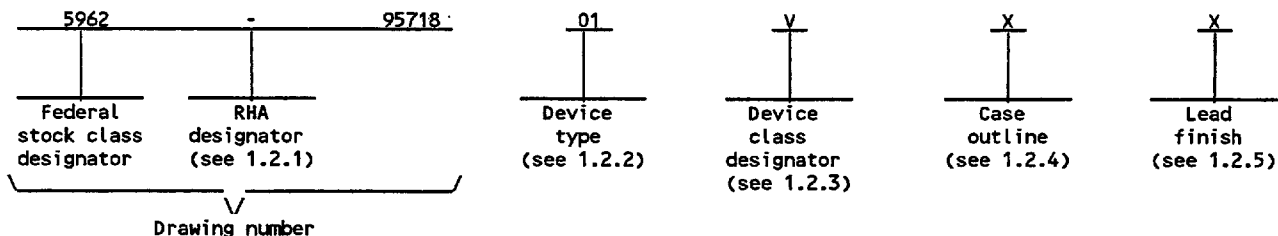
REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

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## 1. SCOPE

1.1 Scope. This drawing forms a part of a one part - one part number documentation system (see 6.6 herein). Two product assurance classes consisting of military high reliability (device classes Q and M) and space application (device class V), and a choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). Device class M microcircuits represent non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices". When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:



1.2.1 RHA designator. Device class M RHA marked devices shall meet the MIL-I-38535 appendix A specified RHA levels and shall be marked with the appropriate RHA designator. Device classes Q and V RHA marked devices shall meet the MIL-I-38535 specified RHA levels and shall be marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

<u>Device type</u>	<u>Generic number</u>	<u>Circuit function</u>
01	MD82C59A/7	Latchup resistant Priority interrupt controller

1.2.3 Device class designator. The device class designator shall be a single letter identifying the product assurance level as follows:

<u>Device class</u>	<u>Device requirements documentation</u>
M	Vendor self-certification to the requirements for non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883
Q or V	Certification and qualification to MIL-I-38535

1.2.4 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

<u>Outline letter</u>	<u>Descriptive designator</u>	<u>Terminals</u>	<u>Package style</u>
X	CDIP2-T28	28	Dual-in-line

1.2.5 Lead finish. The lead finish shall be as specified in MIL-STD-883 (see 3.1 herein) for class M or MIL-I-38535 for classes Q and V. Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference.

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### 1.3 Absolute maximum ratings. 1/

Supply voltage ( $V_{CC}$ )	- - - - -	+8.0 V dc
Input or output voltage range	- - - - -	GND -0.5 V dc to $V_{CC}$ +0.5 V dc
Storage temperature range ( $T_{STG}$ )	- - - - -	-65°C to +150°C
Junction temperature ( $T_J$ )	- - - - -	+175°C
Lead temperature (soldering, 10 seconds)	- - - - -	+275°C
Thermal resistance Junction-to-Case ( $\theta_{JC}$ )	- - - - -	10°C/W
Thermal resistance Junction-to-ambient ( $\theta_{JA}$ )	- - - - -	47°C/W
Maximum power dissipation at +125°C ( $P_D$ ) 2/	- - - - -	1.06 W

### 1.4 Recommended operating conditions.

Operating supply voltage range ( $V_{DD}$ )	- - - - -	4.5 V dc to +5.5 V dc
Ambient operating temperature range ( $T_A$ )	- - - - -	-55°C to +125°C
Input low voltage range ( $V_{IL}$ )	- - - - -	0 V dc to +0.8 V dc
Input high voltage range ( $V_{IH}$ )	- - - - -	2.2 V dc to $V_{DD}$

## 2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, bulletin, and handbook. Unless otherwise specified, the following specification, standards, bulletin, and handbook of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

### SPECIFICATION

#### MILITARY

MIL-I-38535 - Integrated Circuits, Manufacturing, General Specification for.

### STANDARDS

#### MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.  
MIL-STD-973 - Configuration Management.  
MIL-STD-1835 - Microcircuit Case Outlines.

### BULLETIN

#### MILITARY

MIL-BUL-103 - List of Standardized Military Drawings (SMD's).

### HANDBOOK

#### MILITARY

MIL-HDBK-780 - Standardized Military Drawings.

(Copies of the specification, standards, bulletin, and handbook required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

- 1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.  
2/ If device power exceeds package dissipation capability, derate linearly (the derating is based on  $\theta_{JA}$ ) at the following rate: 21.3 mW/°C

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2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

### 3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device class M shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein. The individual item requirements for device classes Q and V shall be in accordance with MIL-I-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not effect the form, fit, or function as described herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-STD-883 (see 3.1 herein) for device class M and MIL-I-38535 for device classes Q and V and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Block diagram. The block diagram shall be as specified on figure 2.

3.2.4 Waveforms. The waveforms shall be as specified on figure 3.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. Marking for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein). In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103. Marking for device classes Q and V shall be in accordance with MIL-I-38535.

3.5.1 Certification/compliance mark. The compliance mark for device class M shall be a "C" as required in MIL-STD-883 (see 3.1 herein). The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-I-38535.

3.6 Certificate of compliance. For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.7.2 herein). For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.7.1 herein). The certificate of compliance submitted to DESC-EC prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device class M, the requirements of MIL-STD-883 (see 3.1 herein), or for device classes Q and V, the requirements of MIL-I-38535 and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required for device class M in MIL-STD-883 (see 3.1 herein) or for device classes Q and V in MIL-I-38535 shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DESC-EC of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-973.

3.9 Verification and review for device class M. For device class M, DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 105 (see MIL-I-38535, appendix A).

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TABLE 1. Electrical performance characteristics.

Test	Symbol	Conditions -55°C ≤ T <sub>A</sub> ≤ +125°C unless otherwise specified 1/	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Logical 1 input voltage	V <sub>IH</sub>	V <sub>CC</sub> = 5.5 V,	1,2,3	All	2.2		V
Logical 0 input voltage	V <sub>IL</sub>	V <sub>CC</sub> = 4.5 V,	1,2,3	All		0.8	V
Output high voltage	V <sub>OH1</sub>	V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -2.5 mA 2/	1,2,3	All	3.0		V
Output high voltage	V <sub>OH2</sub>	V <sub>CC</sub> = 4.5 V, I <sub>OH</sub> = -100.0 μA 2/	1,2,3	All	V <sub>CC</sub> -0.4		V
Output low voltage	V <sub>OL1</sub>	V <sub>CC</sub> = 4.5 V, I <sub>OL</sub> = 2.5 mA 2/	1,2,3	All		0.4	V
High input leakage current	I <sub>IH</sub>	V <sub>CC</sub> = 5.5 V V <sub>IN</sub> = 0 V or V <sub>CC</sub> Pins 1-3, 26, 27	1,2,3	All	-1.0	1.0	μA
Output leakage current	I <sub>OZL</sub> I <sub>OZH</sub>	V <sub>CC</sub> = 5.5 V V <sub>IN</sub> = 0 V or V <sub>CC</sub> Pins 4-13, 15, 16	1,2,3	All	-10	10	μA
IR input load current	I <sub>LIRL</sub>	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 0 V Pins 18-25	1,2,3	All	-500		μA
IR input load current	I <sub>LIRH</sub>	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = 5.5 V Pins 18-25	1,2,3	All		10	μA
Standby power supply	I <sub>CCSB</sub>	V <sub>CC</sub> = 5.5 V, V <sub>IN</sub> = V <sub>CC</sub> or GND Outputs open 3/	1,2,3	All		10	μA
Input capacitance	C <sub>IN</sub>	V <sub>CC</sub> = Open, f = 1 MHz All measurements referenced to device GND See 4.4.1c	4	All		15	pF
Output capacitance	C <sub>OUT</sub>	V <sub>CC</sub> = Open, f = 1 MHz All measurements referenced to device GND, See 4.4.1c	4	All		15	pF
Input capacitance	C <sub>I/O</sub>	V <sub>CC</sub> = Open, f = 1 MHz All measurements referenced to device GND, See 4.4.1c	4	All		15	pF
Functional tests		V <sub>CC</sub> = 4.5 V and V <sub>CC</sub> = 5.5 V 4/ 5/ See 4.4.1b	7,8	All			

See notes at end of table

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions -55°C ≤ T <sub>A</sub> ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
TIMING REQUIREMENTS							
AO $\overline{\text{CS}}$ setup to $\overline{\text{RD}}$ $\overline{\text{INTA}}$	t <sub>AHRL</sub> (1)	6/ 7/	9,10,11	All	10		ns
AO $\overline{\text{CS}}$ hold after $\overline{\text{RD}}$ $\overline{\text{INTA}}$	t <sub>RHAX</sub> (2)	6/ 7/	9,10,11	All	5		ns
$\overline{\text{RD}}$ $\overline{\text{INTA}}$ pulse width	t <sub>RLRH</sub> (3)	6/ 7/	9,10,11	All	235		ns
AO $\overline{\text{CS}}$ setup to $\overline{\text{WR}}$	t <sub>AHWL</sub> (4)	6/ 7/	9,10,11	All	0		ns
AO $\overline{\text{CS}}$ hold after $\overline{\text{WR}}$	t <sub>WHAX</sub> (5)	6/ 7/	9,10,11	All	5		ns
$\overline{\text{WR}}$ pulse width	t <sub>WLWH</sub> (6)	6/ 7/	9,10,11	All	165		ns
Data setup to $\overline{\text{WR}}$	t <sub>DVWH</sub> (7)	6/ 7/	9,10,11	All	240		ns
Data hold after $\overline{\text{WR}}$	t <sub>WDHDX</sub>	6/ 7/	9,10,11	All	5		ns
Interrupt request	t <sub>JLJH</sub>	6/ 7/	9,10,11	All	100		ns
Cascade setup to second or third $\overline{\text{INTA}}$ (slave only)	t <sub>CVIAL</sub> (10)	6/ 7/	9,10,11	All	55		ns
End of $\overline{\text{RD}}$ to next $\overline{\text{RD}}$ ; <del>END of <math>\overline{\text{INTA}}</math> to next</del> $\overline{\text{INTA}}$ within an $\overline{\text{INTA}}$ sequence only	t <sub>RHRL</sub> (11)	6/ 7/	9,10,11	All	160		ns
End of $\overline{\text{WR}}$ to next $\overline{\text{WR}}$	t <sub>WHWL</sub> (12)	6/ 7/	9,10,11	All	190		ns

See footnotes at end of table.

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TABLE 1. Electrical performance characteristics - Continued.

Test	Symbol	Conditions -55°C ≤ T <sub>C</sub> ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
TIMING REQUIREMENTS - CONTINUED.							
End of command to next command (not same command type) end of <u>INTA</u> sequence to next <u>INTA</u> sequence	t <sub>CHCL</sub> (13)	6/7/8/	9,10,11	All	500		ns
Data valid from <u>RD</u> <u>INTA</u>	t <sub>RLDV</sub> (14)	6/7/	9,10,11	All		160	ns
Interrupt output delay	t <sub>JHIH</sub> (16)	6/7/	9,10,11	All		350	ns
Cascade valid from first <u>INTA</u> (master only)	t <sub>IALCV</sub> (17)	6/7/	9,10,11	All		565	ns
Enable active form <u>RD</u> or <u>INTA</u>	t <sub>RLEL</sub> (18)	6/7/	9,10,11	All		125	ns
Enable inactive form <u>RD</u> <u>INTA</u>	t <sub>RHEH</sub> (19)	6/7/	9,10,11	All		60	ns
Data valid from stable address	t <sub>AHDV</sub> (20)	6/7/	9,10,11	All		210	ns
Cascade valid to valid data	t <sub>CVDV</sub> (21)	6/7/	9,10,11	All		300	ns
Data float after <u>RD</u> / <u>INTA</u>	t <sub>RHDZ</sub> (15)	7/9/	9,10,11	All	10	100	ns

1/ All testing to be performed using worst case test conditions, unless otherwise specified.

2/ Interchanging of force and sense conditions is permitted.

3/ Except for IR0-IR7, where V<sub>IN</sub> = V<sub>CC</sub> or open.

4/ Frequency defines the peripheral read/write cycle time. f = 1.25 MHz.

5/ Tested as follows: V<sub>IH</sub> = 2.6 V, V<sub>IL</sub> = 0.4 V, V<sub>OH</sub> ≥ 1.5 V, V<sub>OL</sub> ≤ 1.5 V.

6/ Tested as follows: f = 1 MHz, V<sub>IH</sub> = 2.6 V, V<sub>IL</sub> = 0.4 V, V<sub>OH</sub> ≥ 1.5 V, V<sub>OL</sub> ≤ 1.5 V, V<sub>CC</sub> = 4.5 V, test condition 2 in figure 4.

7/ See test condition 1 in figure 4.

8/ Worst case timing for t<sub>CHCL</sub> in actual system is typically much greater than 400 ns.

9/ The parameters listed in the table are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design and after process and/or design changes.

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Device type	01
Case outline	X
Terminal number	Terminal symbol
1	$\overline{CS}$
2	$\overline{WR}$
3	$\overline{RD}$
4	D <sub>7</sub>
5	D <sub>6</sub>
6	D <sub>5</sub>
7	D <sub>4</sub>
8	D <sub>3</sub>
9	D <sub>2</sub>
10	D <sub>1</sub>
11	D <sub>0</sub>
12	CAS 0
13	CAS 1
14	GND
15	CAS 2
16	$\overline{SP/EN}$
17	INT
18	IR0
19	IR1
20	IR2
21	IR3
22	IR4
23	IR5
24	IR6
25	IR7
26	$\overline{INTA}$
27	A <sub>0</sub>
28	V <sub>CC</sub>

FIGURE 1. Terminal connections.

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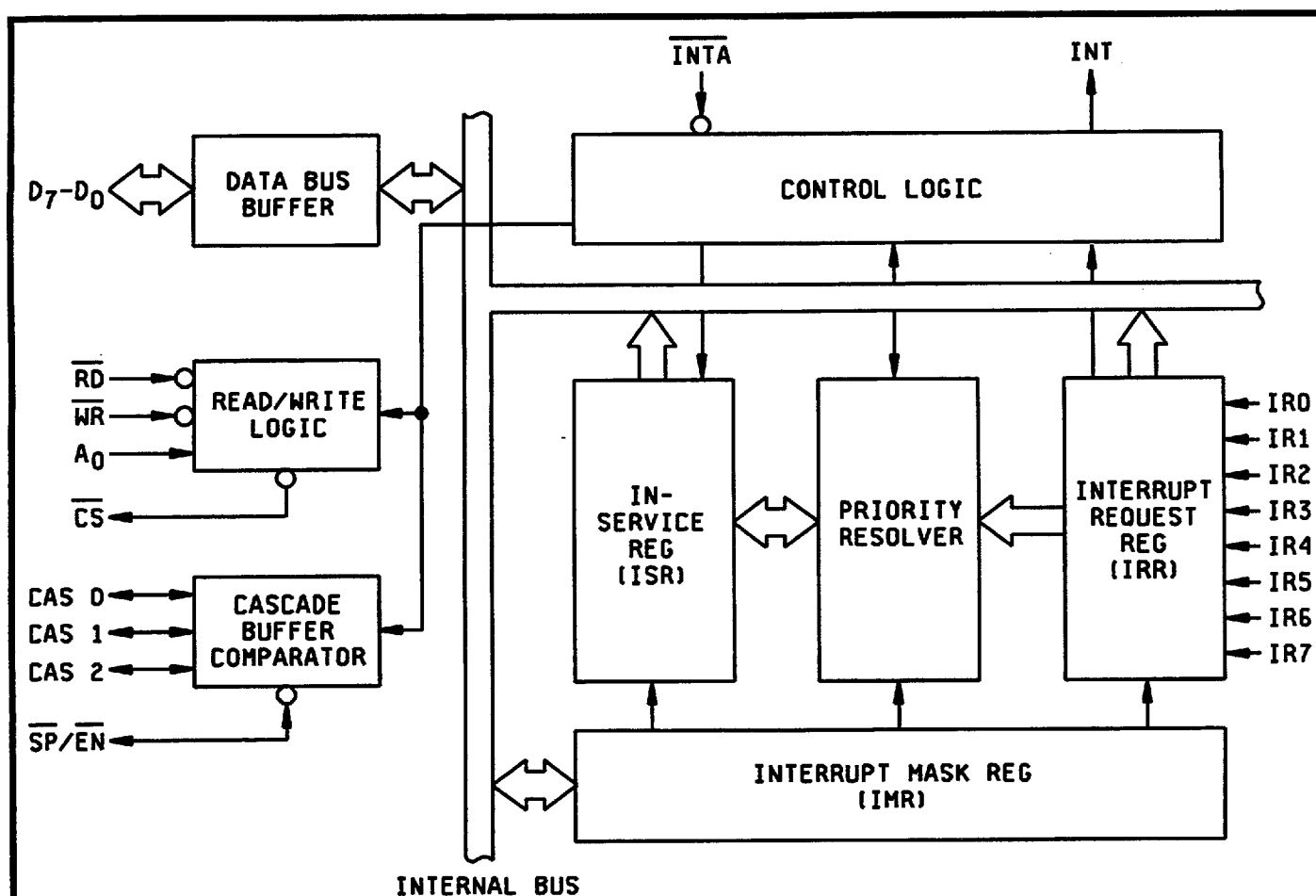


FIGURE 2. Block diagram.

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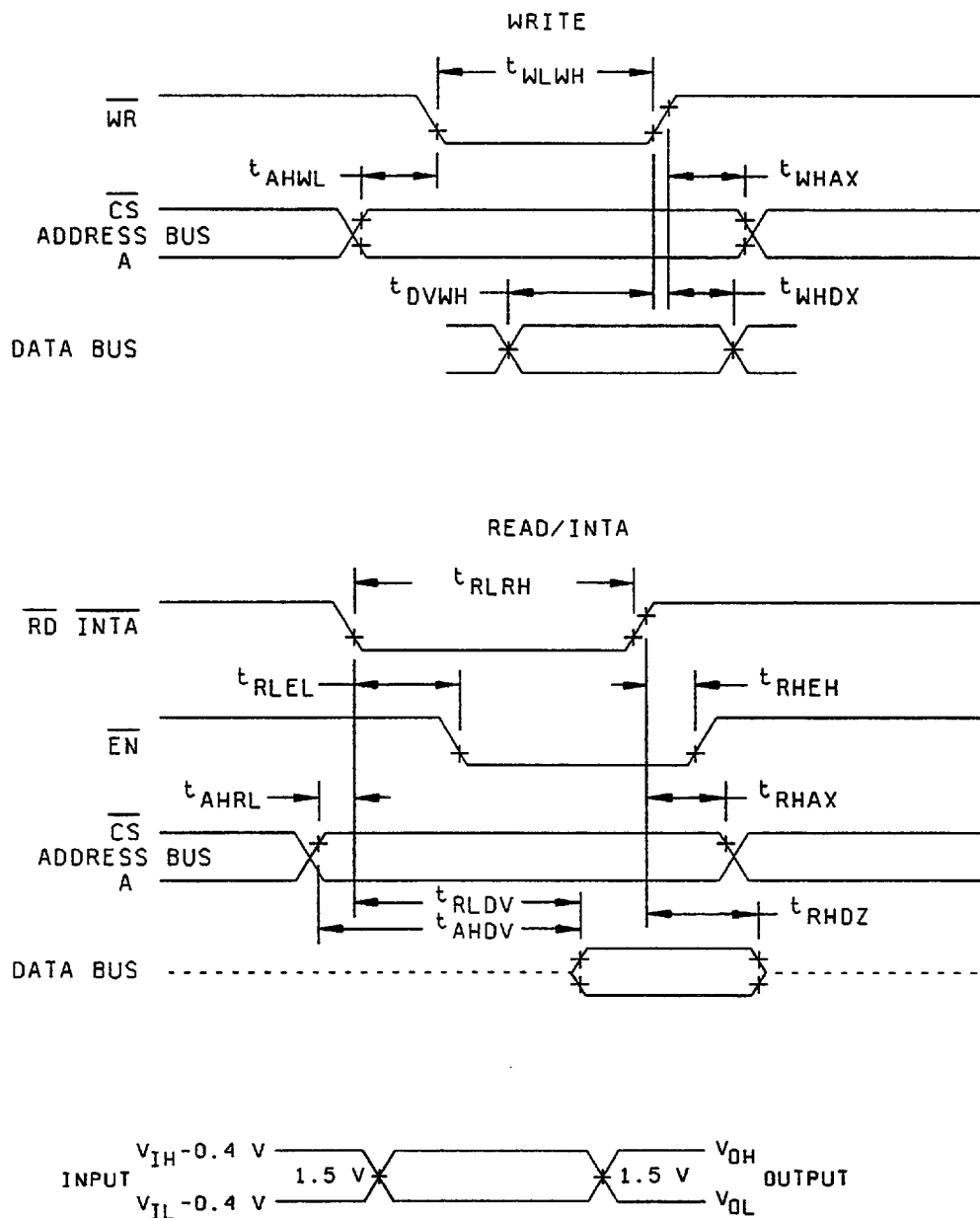
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Note: All inputs signals must switch between  $V_{IL} - 0.4 V$  and  $V_{IH} + 0.4 V$ . Input rise and fall times are driven at 1 ns/V

FIGURE 3. Timing waveforms.

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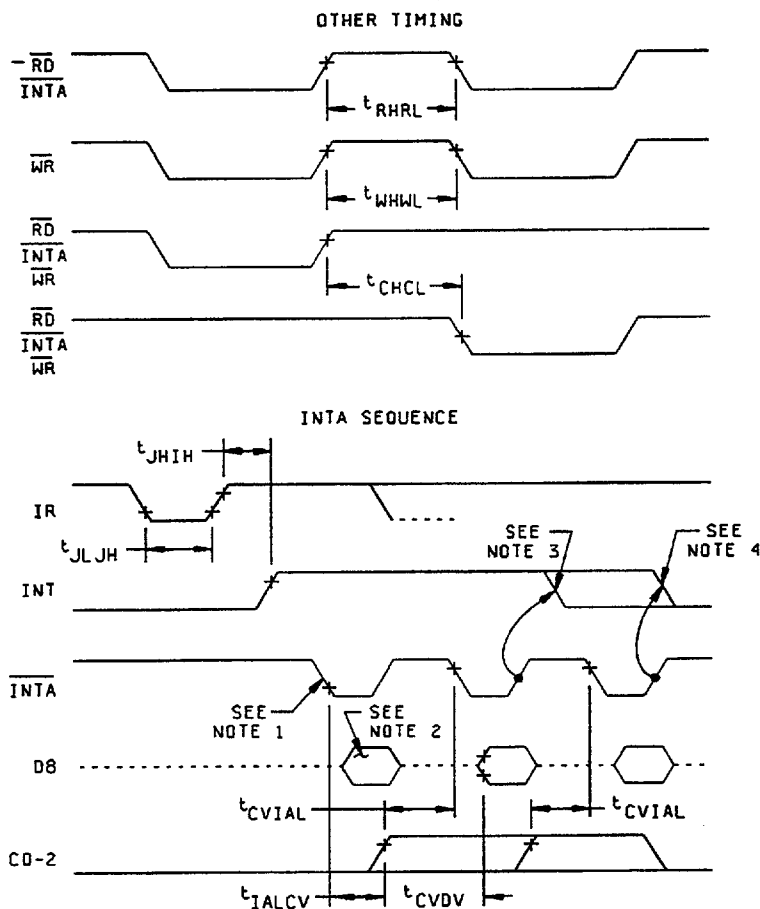
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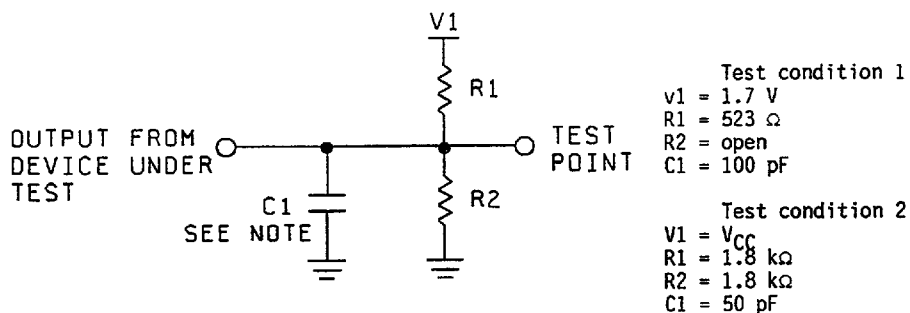
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**notes:**

1. Interrupt request (IR) must remain high until leading edge of first  $\overline{\text{INTA}}$ .
2. During first INTA the data bus is not active in 80c86/88 mode.
3. 80c86/88 mode.
4. 8080/8085 mode.



Note: Includes stray jig capacitance.

FIGURE 3. Timing waveforms - Continued.

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#### 4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device class M, sampling and inspection procedures shall be in accordance with MIL-STD-883 (see 3.1 herein). For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-I-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not effect the form, fit, or function as described herein.

4.2 Screening. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. For device classes Q and V, screening shall be in accordance with MIL-I-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

##### 4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(2)  $T_A = +125^{\circ}\text{C}$ , minimum.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

##### 4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-I-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in appendix B of MIL-I-38535, or as modified in the device manufacturers approved quality management(QM) plan.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-I-38535. Inspections to be performed shall be those specified in MIL-I-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Quality conformance inspection for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein) and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4). Technology conformance inspection for classes Q and V shall be in accordance with MIL-I-38535 or as specified in QM plan including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-I-38535 permits alternate in-line control testing.

##### 4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.

c. Subgroup 4 ( $C_{IN}$ ,  $C_{OUT}$  and  $C_{I/O}$  measurements) shall be measured only for the initial qualification and after process or design changes which may affect capacitance. A minimum sample size of 5 devices with zero rejects shall be required.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

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TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, TM 5005, table I)	Subgroups (in accordance with MIL-I-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1,7,9	1,7,9	1,7,9
Final electrical parameters (see 4.2)	1,2,3,7,8, 1/ 9,10,11	1,2,3,7,8, 1/ 9,10,11	1,2,3,7,2/ 8,9,10,11 3/
Group A test requirements (see 4.4)	1,2,3,4,7,8,9,10,11	1,2,3,4,7,8,9, 10, 11	1,2,3,4,7,8, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1,2,3,7,8,9 10,11	1,2,3,7,8,9 10,11	1,2,3,7,8,9 10,11 3/
Group D end-point electrical parameters (see 4.4)	1,7,9	1,7,9	1,7,9
Group E end-point electrical parameters (see 4.4)	1,7,9	1,7,9	1,7,9

1/ PDA applies to subgroup 1 and 7.

2/ PDA applies to subgroups 1, 7, 9 and delta's.

3/ Delta limits are as specified in Table IIB herein and shall be required where specified and the delta value shall be completed with reference to the zero hour electrical parameters (See Table I).

Table IIB Burn-in and operating life test delta parameters (+25°C)

Parameter	Symbol	Delta Limits
Standby power supply current	I <sub>CCSB</sub>	±2.0 µA
Output leakage current	I <sub>OZL</sub> , I <sub>OZH</sub>	±2.0 µA
Input leakage current	I <sub>IH</sub> , I <sub>IL</sub>	±200.0 nA

#### 4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A, B, C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

b. T<sub>A</sub> = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

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4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-I-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB, in accordance with MIL-I-38535, and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes Q and V shall be M, D, L, R, F, G, and H and for device class M shall be M and D.

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-I-38535, appendix A, for the RHA level being tested. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-I-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at  $T_A = +25^{\circ}\text{C} \pm 5^{\circ}\text{C}$ , after exposure, to the subgroups specified in table IIA herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

## 5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-STD-883 (see 3.1 herein) for device class M and MIL-I-38535 for device classes Q and V.

## 6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and which SMD's are applicable to that system. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DESC-EC, telephone (513) 296-6047.

6.4 Comments. Comments on this drawing should be directed to DESC-EC, Dayton, Ohio 45444-5270, or telephone (513) 296-5377.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-I-38535 and MIL-STD-1331 and as follows:

<u>Pin symbol</u>	<u>Type</u>	<u>Description</u>
$V_{CC}$	I	$V_{CC}$ : The +5 V power supply pin. A 0.1 $\mu\text{F}$ capacitor between $V_{CC}$ and GND is recommended for decoupling.
GND	I	GROUND.
$\overline{\text{CS}}$	I	CHIP SELECT: A low on this pins enable $\overline{\text{RD}}$ and $\overline{\text{WR}}$ communications between the CPU and the device. INTA functions are independent of CS.
$\overline{\text{WR}}$	I	WRITE: A low on this pin when $\overline{\text{CS}}$ is low enables the device to release status onto the data bus for the CPU.
$\overline{\text{RD}}$	I	READ: A low on this pin when $\overline{\text{CS}}$ is low enables the device to release status onto the data bus for the CPU.

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<u>Pin symbol</u>	<u>Type</u>	<u>Description</u> - Continued.
D7-D0	I/O	BIDIRECTIONAL DATA BUS: Control status and interrupt-vector information is transferred via the bus.
CAS0-CAS2	I/O	CASCADE LINES: The CAS lines form a private device bus to control a multiple device structure. These pins are outputs for a master device and an inputs for a slave device.
$\overline{SP/EN}$	I/O	SLAVE PROGRAM/ENABLE BUFFER: This is a full function pin. When <u>in</u> the buffered mode it can be used as an output to control buffer transceivers ( <u>EN</u> ). When not in the buffered mode it is used as an input to designate a master ( <u>SP</u> = 1) or slave ( <u>SP</u> = 0).
INT	0	INTERRUPT: This pin goes high whoever a valid interrupt request is asserted. It is used to interrupt the CPU, thus it is connected to the CPU's interrupt pin.
IRO-IR7	I	INTERRUPT REQUESTS: Asynchronous inputs. An interrupt requests is executed by raising an IR input (low to high), and holding it high until it is acknowledged (edge triggered mode), or just by a high level on an IR input (level triggered mode).
$\overline{INTA}$	I	INTERRUPT ACKNOWLEDGE: This pin is used to enable device interrupt-vector data onto the data bus by a sequence of interrupt acknowledge pulses issued by the CPU.
A0	I	ADDRESS LINE: This pin acts in conjunction with the $\overline{CS}$ , $\overline{WR}$ , and $\overline{RD}$ pins. It is used by the device to decipher various command words the CPU writes and status the CPU wishes to read. It is typically connected to CPU A0 address line.

6.6 One part - one part number system. The one part - one part number system described below has been developed to allow for transitions between identical generic devices covered by the three major microcircuit requirements documents (MIL-H-38534, MIL-I-38535, and 1.2.1 of MIL-STD-883) without the necessity for the generation of unique PIN's. The three military requirements documents represent different class levels, and previously when a device manufacturer upgraded military product from one class level to another, the benefits of the upgraded product were unavailable to the Original Equipment Manufacturer (OEM), that was contractually locked into the original unique PIN. By establishing a one part number system covering all three documents, the OEM can acquire to the highest class level available for a given generic device to meet system needs without modifying the original contract parts selection criteria.

<u>Military documentation format</u>	<u>Example PIN under new system</u>	<u>Manufacturing source listing</u>	<u>Document listing</u>
New MIL-H-38534 Standard Microcircuit Drawings	5962-XXXXXZZ(H or K)YY	QML-38534	MIL-BUL-103
New MIL-I-38535 Standard Microcircuit Drawings	5962-XXXXXZZ(Q or V)YY	QML-38535	MIL-BUL-103
New 1.2.1 of MIL-STD-883 Standard Microcircuit Drawings	5962-XXXXXZZ(M)YY	MIL-BUL-103	MIL-BUL-103

#### 6.7 Sources of supply.

6.7.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DESC-EC and have agreed to this drawing.

6.7.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-EC.

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