REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																				
SHEET																				
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SHEET	15																			

REV STATUS OF SHEETS	REV														
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

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DRAWING APPROVAL DATE
96-04-11

REVISION LEVEL

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

MICROCIRCUIT, MEMORY, DIGITAL, RADIATION-HARDENED, CMOS/SOS, 1K x 4 STATIC RAM, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	67268	**5962-96695**

SHEET 1 OF 15

DESC FORM 193
JUL 94

9004708 0021553 044

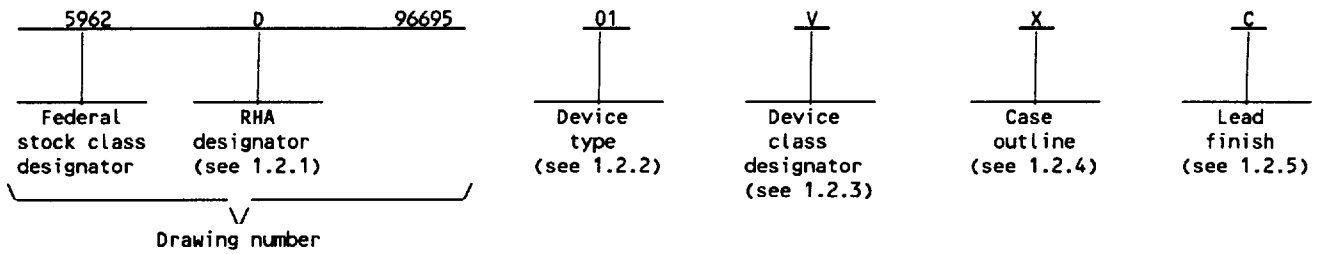
DISTRIBUTION STATEMENT A. Approved for public release, distribution is unlimited

5962-E069-96

1. SCOPE

1.1 Scope. This drawing forms a part of a one part - one part number documentation system (see 6.6 herein). Two product assurance classes consisting of military high reliability (device classes Q and M) and space application (device class V), and a choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). Device class M microcircuits represent non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices." When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:



1.2.1 RHA designator. Device class M RHA marked devices shall meet the MIL-PRF-38535 appendix A specified RHA levels and shall be marked with the appropriate RHA designator. Device classes Q and V RHA marked devices shall meet the MIL-PRF-38535 specified RHA levels and shall be marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device types. The device types shall identify the circuit function as follows:

Device type	Generic number 1/	Circuit function	Access time
01	5114A	1K X 4 Radiation hardened CMOS/SOS SRAM	250 ns

1.2.3 Device class designator. The device class designator shall be a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for non-JAN class B microcircuits in accordance with 1.2.1 of MIL-STD-883
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
V	CDIP2-T18	18	Dual-in-line package
X	CDFP4-F24	24	Flat pack

1.2.5 Lead finish. The lead finish shall be as specified in MIL-STD-883 (see 3.1 herein) for class M or MIL-PRF-38535 for classes Q and V. Finish letter "X" shall not be marked on the microcircuit or its packaging. The "X" designation is for use in specifications when lead finishes A, B, and C are considered acceptable and interchangeable without preference.

1/ Generic numbers are listed on the Standard Microcircuit Drawing Source Approval Bulletin at the end of this document and will also be listed in QML-38535 and MIL-BUL-103.

1.3 Absolute maximum ratings. 2/

Supply voltage range	-0.5 V to +7.0 V dc
Input voltage range, all inputs	-0.5 V dc to V_{DD} +0.5 V dc
Input current, any one input	±10mA
Maximum package power dissipation (P_D) at T_A = +125°C:	
Case V	0.64 W 3/
Case X	0.63 W 3/
Lead temperature (soldering, 10 seconds maximum)	+265°C
Thermal resistance, junction-to-case (Θ_{JC}):	
Case V	18°C/W
Case X	20°C/W
Thermal resistance, junction-to-ambient (Θ_{JA}):	
Case V	78°C/W
Case X	80°C/W
Junction temperature (T_J)	+175°C
Storage temperature range	-65°C to +150°C

1.4 Recommended operating conditions.

Supply voltage (V_{DD})	+4.5 V dc to +5.5 V dc
Ground voltage (GND)	0.0 V dc
Input high voltage (V_{IH})	$V_{DD}/2$ to V_{DD}
Input Low voltage (V_{IL})	0.0 V dc to +0.8 V dc maximum
Case operating temperature range (T_C)	-55°C to +125°C
Radiation features:	
Total dose irradiation	≥ 10 KRads(Si)
Dose rate upset (20 ns pulse)	≥ 1×10^{10} Rads(Si)/sec 4/
Dose rate survivability	≥ 1×10^{12} Rads(Si)/sec 4/
Single event phenomenon (SEP) effective linear energy threshold (LET) with no upsets	≥ 100 MeV/(cm^2/mg) 4/

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, bulletin, and handbook. Unless otherwise specified, the following specification, standards, bulletin, and handbook of the issue listed in that issue of the Department of Defense Index of Specifications and Standards specified in the solicitation, form a part of this drawing to the extent specified herein.

SPECIFICATION

MICROCIRCUIT

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

MICROCIRCUIT

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Microcircuit Case Outlines.

BULLETIN

MICROCIRCUIT

MIL-BUL-103 - List of Standard Microcircuit Drawings (SMD's).

2/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
3/ If device power exceeds package dissipation capability, provide heat sinking or derate linearly (the derating is based on Θ_{JA}) at the following rate: case outline V - - - 12.8 mW/°C, case outline X - - - 12.5 mW/°C.
4/ Guaranteed by process or design, but not tested.

HANDBOOK

MICROCIRCUIT

MIL-HDBK-780 - Standardized Military Drawings.

(Copies of the specification, standards, bulletin, and handbook required by manufacturers in connection with specific acquisition functions should be obtained from the contracting activity or as directed by the contracting activity.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device class M shall be in accordance with 1.2.1 of MIL-STD-883, "Provisions for the use of MIL-STD-883 in conjunction with compliant non-JAN devices" and as specified herein. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535, and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not effect the form, fit, or function as described herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-STD-883 (see 3.1 herein) for device class M and MIL-PRF-38535 for device classes Q and V and herein.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.4 Irradiation test connections. The irradiation test connections shall be as specified in table III.

3.2.5 Functional tests. Functional tests used to test this device shall be maintained under document revision level control by the manufacturer and shall be made available to the preparing or acquiring activity upon request. For device classes Q and V, test patterns shall be under the control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the preparing or acquiring activity upon request.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified, the electrical performance characteristics, and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. Marking for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein). In addition, the manufacturer's PIN may also be marked as listed in MIL-BUL-103. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The compliance mark for device class M shall be a "C" as required in MIL-STD-883 (see 3.1 herein). The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-BUL-103 (see 6.7.2 herein). For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.7.1 herein). The certificate of compliance submitted to DESC-EC prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device class M the requirements of MIL-STD-883 (see 3.1 herein), or for device classes Q and V, the requirements of MIL-PRF-38535 and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required for device class M in MIL-STD-883 (see 3.1 herein) or for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DESC-EC of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-973.

Table I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.75\ V \le V_{DD} \le 5.25\ V$ unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
Output current (sink)	I_{OL}	V_{DD} = 4.75 V, V_{OUT} = 0.4 V		1,3	01	2.6		mA
				2		1.7		
			M,D	1				
				2/		1.7		mA
Output current (source)	I_{OH}	V_{DD} = 4.75 V, $V_{OUT} = V_{DD} - 0.4$ V		1,3	01	-1.8		mA
				2		-1.1		
			M,D	1				
				2/		-1.1		mA
High level input voltage	V_{IH}	V_{DD} = 4.75 V		1,2,3	01	$V_{DD}/2$		V
			M,C	1				
				2/		3/		V
Low level input voltage	V_{IL}	V_{DD} = 4.5 V		1,2,3	01		0.8	V
			M,D	1				
				2/			3/	V
Input leakage current	I_{IN}	V_{DD} = 5.25 V, V_{IN} = GND or V_{DD}		1,3	01	-2	2	µA
				2		-10	10	
			M,D	1				
				2/		-10	10	µA
High impedance output leakage current	I_{OZ}	V_{DD} = 5.25 V, $V_{I/O}$ = GND or V_{DD}		1,3	01	-5	5	µA
				2		-50	50	
			M,D	1				
				2/		-50	50	µA
Quiescent supply current	I_{DD}	V_{DD} = 5.25 V, V_{IN} = GND or V_{DD}, $\overline{CE} = V_{DD}$		1,3	01		0.1	mA
				2			1.0	
			M,D	1				
				2/			1.0	mA
Operating supply current	I_{DDOP}	V_{DD} = 5.25 V, f= 1 Mhz, V_{IN} = GND or V_{DD}, C_L = 50 pF, outputs open circuit		1,3	01		5	mA
				2			6	
			M,D	1				
				2/			6	mA

See footnotes at end of table.

Table I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.75\ V \le V_{DD} \le 5.25\ V$ unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
Data retention voltage	V_{DR}			1,3	01		2.0	V
				2			2.5	
			M,D	1 2/			2.5	V
Data retention current	I_{DDDR}	$V_{DD} = V_{DR}$, $I_{OUT} = 0$ mA V_{IN} = GND or V_{DD}		1,3	01		50	µA
				2			500	
			M,D	1 2/			500	µA
Input capacitance 1/	C_{IN}	V_{DD} = open, f = 1.0 MHz, see 4.4.1c		4	01		5	pF
Output capacitance 1/	C_{OUT}	V_{DD} = open, f = 1.0 MHz, see 4.4.1c		4	01		7	pF
Functional tests		See 4.4.1d, V_{DD} = 4.75 V, f = 1 MHz, $V_{IH} = V_{DD}$ V_{IL} = GND, $V_{OH} \ge V_{DD}/2$ $V_{OL} \le V_{DD}/2$		7,8A,8B	01			
			M,D	7 2/		3/		
Read cycle	t_{AVAV}	See figure 3 4/		9,11	01	200		ns
				10		250		
			M,D	9 2/		250		ns
Address access time	t_{AVQV}			9,11	01		200	ns
				10			250	
			M,D	9 2/			250	ns
Chip enable access time	t_{ELQV}			9,11	01		220	ns
				10			280	
			M,D	9 2/			280	ns
Output hold from address 1/	t_{AVQZ}			9,11	01	30	110	ns
				10		55	150	
Output hold from chip enable 1/	t_{EHQZ}			9,11	01		100	ns
				10			140	
Chip enable to output active 1/	t_{ELQX}			9,10,11	01	20		ns

See footnotes at end of table.

Table I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.75\ V \le V_{DD} \le 5.25\ V$ unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
Write cycle	t_{AVAV}	See figure 3 4/		9,11	01	250		ns
				10		300		
			M,D	9 2/		300		ns
Write pulse width 5/	t_{WLWH}			9,10,11	01	200		ns
			M,D	9 2/		3/		ns
Address hold time from write enable	t_{WHAV}			9,11	01	40		ns
				10		50		
			M,D	9 2/		50		ns
Address set-up to beginning of write	t_{AVWL}			9,10,11	01	0		ns
			M,D	9 2/		3/		ns
Address set-up to end of write	t_{AVWH}			9,11	01	200		ns
				10		250		
			M,D	9 2/		250		ns
Chip enable to write set-up time	t_{ELWH}			9,11	01	200		ns
				10		250		
			M,D	9 2/		250		ns
Chip enable pulse width 5/	t_{ELEH}			9,11	01	200		ns
				10		250		
			M,D	9 2/		250		ns
Data to write set-up time	t_{DVWH}			9,11	01	90		ns
				10		105		
			M,D	9 2/		105		ns

See footnotes at end of table.

Table I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.75\ V \le V_{DD} \le 5.25\ V$ unless otherwise specified		Group A subgroups	Device type	Limits		Unit
						Min	Max	
Data hold from write	t_{WHDX}	See figure 3 4/		9,10,11	01	5		ns
			M,D	9 2/		3/		ns

1/ Tested initially and after any design or process changes that affect that parameter, and therefore shall be guaranteed to the limits specified in table I.
2/ When performing postirradiation electrical measurements for any RHA level $T_A = +25°C$. Limits shown are guaranteed at $T_A = +25°C \pm 5°C$. The M and D in the test condition column are the postirradiation limits for the device types specified in the device types column.
3/ Preirradiation values for RHA marked devices shall also be the postirradiation values, unless otherwise specified.
4/ AC measurements assume rise and fall times of 5 ns or less, timing reference levels of $V_{DD}/2$ and $C_L = 50$ pF (see figure 3).
5/ CE and WE must overlap for at least t_{WLWH} minimum value, t_{DVWH} minimum value must occur during this overlap.

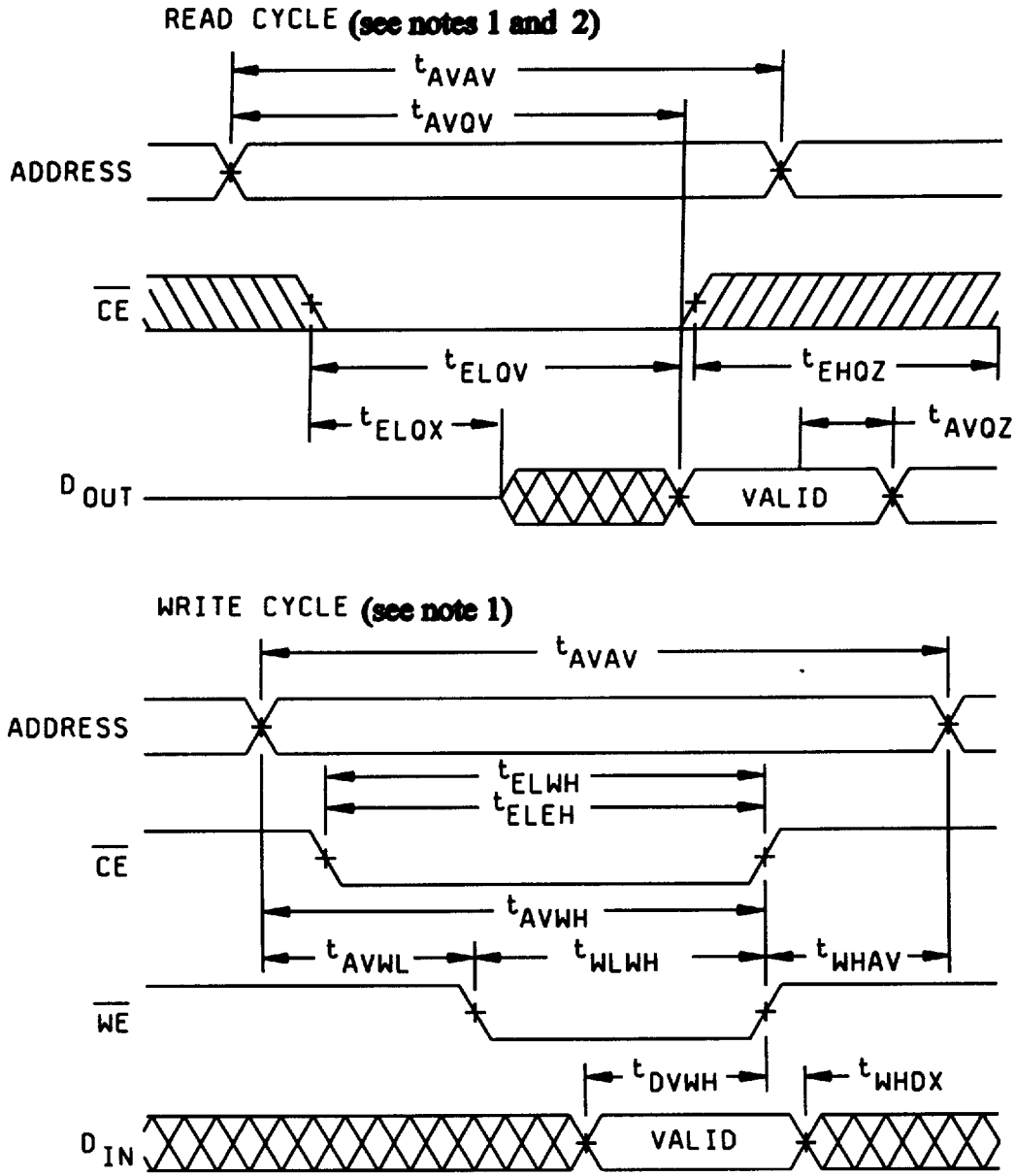
Device types	All	
Case outlines	V	X
Terminal number	Terminal symbol	
1	A_6	NC
2	A_5	A_6
3	A_4	A_5
4	A_3	A_4
5	A_0	A_3
6	A_1	NC
7	A_2	A_0
8	$\overline{CE}$	A_1
9	V_{SS}	A_2
10	$\overline{WE}$	NC
11	I/O_4	$\overline{CE}$
12	I/O_3	V_{SS}
13	I/O_2	$\overline{WE}$
14	I/O_1	NC
15	A_9	I/O_4
16	A_8	I/O_3
17	A_7	I/O_2
18	V_{DD}	I/O_1
19	---	NC
20	---	NC
21	---	A_9
22	---	A_8
23	---	A_7
24	---	V_{DD}

FIGURE 1. Terminal connections.

Mode	$\overline{CE}$	$\overline{WE}$	Outputs
Not selected	H	X	High Z
Write	L	L	Input
Read	L	H	Data out

NOTES:
1. L = logic low voltage level; H = logic high voltage level; X can be H or L.
2. High Z is high impedance state.

FIGURE 2. Truth table.



NOTES:
1. Timing measurement is referenced to $V_{DD}/2$.
2. WE is high during read cycle.

FIGURE 3. Timing waveforms.

Table IIA. Electrical test requirements. 1/ 2/ 3/ 4/ 5/ 6/ 7/

Line no.	Test requirements	Subgroups (per method 5005, table IA)	Subgroups (per MIL-PRF-38535, table III)	
		Device class M	Device class Q	Device class V
1	Interim electrical parameters (see 4.2)	1,7,9	1,7,9	1,7,9
2	Static burn-in I 8/ method 1015	Not required	Required	Required
3	Same as line 1		1*,7*,9	1*,7*,9 Δ*
4	Static burn-in II method 1015	Not required	Not required	Required
5	Same as line 1		1*,7*,9	1*,7*,9 Δ*
6	Dynamic burn-in (method 1015)	Required	Not required	Required
7	Final electrical parameters	1*,2,3,7*, 8A,8B,9,10, 11	1*,2,3,7*, 8A,8B,9,10, 11	1*,2,3,7*, 8A,8B,9,10, 11 Δ*
8	Group A test requirements	1,2,3,4**,7,8 A,8B,9,10, 11	1,2,3,4**,7, 8A,8B,9,10, 11	1,2,3,4**,7, 8A,8B,9,10, 11
9	Group C end-point electrical parameters	1,2,3,7, 8A,8B	1,2,3,7, 8A,8B,9,10, 11	1,2,3,7, 8A,8B,9,10, 11
10	Group D end-point electrical parameters	1,7,9	1,7,9	1,7,9
11	Group E end-point electrical parameters	1,7,9		1,7,9

1/ Blank spaces indicate test are not applicable.
2/ Any or all subgroups may be combined when using high-speed testers.
3/ Subgroups 7 and 8 functional tests shall verify the truth table.
4/ * Indicates subgroups used for PDA calculation.
5/ ** See 4.4.1c.
6/ Δ Indicates delta limit (see table IIB) shall be required where specified, and the delta values shall be computed with reference to the interim electrical parameters (see line 1).
7/ See 4.5.
8/ 24 hours for class Q, 160 hours or equivalent for class V.

Table IIB. Delta limits at +25°C.

Test 1/	All device types
I_{OZ}	+500 nA of specified value in table I
I_{DD}	+30 μA of specified value in table I
I_{OL}	-10% of specified value in table I
I_{OH}	-10% of specified value in table I

1/ The above parameter shall be recorded before and after the required burn-in and life tests to determine the delta.

TABLE III. Irradiation test connections. 1/ 2/

Case	Ground	V_{DD} = 5 V ± 0.25 V
V	9	1,2,3,4,5,6,7,8,10,11, 12,13,14,15,16,17,18

1/ Each pin except V_{DD} and GND connections will have a series resistor of 47kΩ±5% for irradiation testing.
2/ Irradiation samples only assembled in case outline V.

3.9 Verification and review for device class M. For device class M, DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 41 (see MIL-PRF-38535, appendix A).

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device class M, sampling and inspection procedures shall be in accordance with MIL-STD-883 (see 3.1 herein). For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not effect the form, fit, or function as described herein.

4.2 Screening. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device class M.

a. Delete the sequence specified as initial (preburn-in) electrical parameters through interim (postburn-in) electrical parameters of method 5004 and substitute lines 1 through 6 of table IIA herein.

b. For device class M, the test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. For device class M, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(1) Dynamic burn-in for device class M (method 1015 of MIL-STD-883, test condition D; for circuit, see 4.2.1b herein).

c. Interim and final electrical parameters shall be as specified in table IIA herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition, and test temperature or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 or as modified in the device manufacturer's QM plan.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in appendix B of MIL-PRF-38535 or as modified in the device manufacturers Quality Management (QM) plan.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Quality conformance inspection for device class M shall be in accordance with MIL-STD-883 (see 3.1 herein) and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4). Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 or as specified in the QM plan, including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-PRF-38535 permits alternate in-line control testing.

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.

d. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for initial qualification and after any process or design changes which may affect input or output capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency of 1 MHz. Sample size is 5 devices with no failures, and all input and output terminals tested.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition, and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

4.4.3 Group D inspection. For group D inspection, end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein). RHA levels for device classes M, Q and V shall be as specified in MIL-PRF-38535. End-point electrical parameters shall be as specified in table IIA herein.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019 and as specified herein.

4.4.4.1.1 Accelerated aging test. Accelerated aging tests shall be performed on all devices requiring a RHA level greater than 5k rads(Si). The post-anneal end-point electrical parameter limits shall be as specified in table I herein and shall be the pre-irradiation end-point electrical parameter limit at 25°C ±5°C. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

4.4.4.2 Dose rate induced latchup testing. Dose rate induced latchup testing shall be performed in accordance with test method 1020 of MIL-STD-883 and as specified herein (see 1.4). Tests shall be performed on devices, SEC, or approved test structures at technology qualification and after any design or process changes which may effect the RHA capability of the process.

4.4.4.3 Dose rate upset testing. Dose rate upset testing shall be performed in accordance with test method 1021 of MIL-STD-883 and herein (see 1.4).

a. Transient dose rate upset testing shall be performed at initial qualification and after any design or process changes which may effect the RHA performance of the devices. Test 10 devices with 0 defects unless otherwise specified.

b. Transient dose rate upset testing for class Q and V devices shall be performed as specified by a TRB approved radiation hardness assurance plan and MIL-PRF-38535.

4.4.4.4 Single event phenomena (SEP). SEP testing shall be required on class V devices (see 1.4 herein). SEP testing shall be performed on a technology process on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at inital qualification and after any design or process changes which may affect the upset or latchup characteristics. The recommended test conditions for SEP are as follows:

a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e. 0° ≤ angle ≤ 60°). No shadowing of the ion beam due to fixturing or package related effects is allowed.

b. The fluence shall be ≥ 100 errors or ≥ 10^6 ions/cm^2.

c. The flux shall be between 10^2 and 10^5 ions/cm^2/s. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates which differ by at least an order of magnitude.

d. The particle range shall be ≥ 20 microns in silicon.

e. The test temperature shall be +25 °C and the maximum rated operating temperature ±10 °C.

f. Bias conditions shall be defined by the manufacturer for latchup measurements.

g. Test four devices with zero failures.

4.5 Delta measurements for device class V. Delta measurements, as specified in table IIA, shall be made and recorded before and after the required burn-in screens to determine delta compliance. The electrical parameters to be measured, with associated delta limits are listed in table IIB. The device manufacturer may, at his option, either perform delta measurements or within 24 hours after burn-in perform final electrical parameter tests, subgroups 1, 7, and 9.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-STD-883 (see 3.1 herein) for device class M and MIL-PRF-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1693, Engineering Change Proposal (Short Form).

6.3 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and which SMD's are applicable to that system. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DESC-EC, telephone (513) 296-6047.

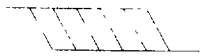
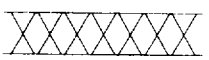
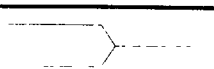
6.4 Comments. Comments on this drawing should be directed to DESC-EC, Dayton, Ohio 45444, or telephone (513) 296-5377.

6.5 Symbols, definitions, and functional descriptions.

C_{IN} . . . . . Input terminal capacitance.
C_{OUT} . . . . . Output terminal capacitance.
GND . . . . . Ground zero voltage potential.
I_{DD} . . . . . Supply current.
I_I . . . . . Input current.
I_O . . . . . Output current.
T_C . . . . . Case temperature.
V_{DD} . . . . . Positive supply voltage.

6.5.1 Timing limits. The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. For example, address setup time would be shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. For example, the access time would be shown as a maximum since the device never provides data later than that time.

6.5.2 Waveforms.

Waveform symbol	Input	Output
	MUST BE VALID	WILL BE VALID
	CHANGE FROM H TO L	WILL CHANGE FROM H TO L
	CHANGE FROM L TO H	WILL CHANGE FROM L TO H
	DON'T CARE ANY CHANGE PERMITTED	CHANGING STATE UNKNOWN
		HIGH IMPEDANCE

6.6 One part - one part number system. The one part - one part number system described below has been developed to allow for transitions between identical generic devices covered by the three major microcircuit requirements documents (MIL-H-38534, MIL-PRF-38535, and 1.2.1 of MIL-STD-883) without the necessity for the generation of unique PIN's. The three military requirements documents represent different class levels, and previously when a device manufacturer upgraded military product from one class level to another, the benefits of the upgraded product were unavailable to the Original Equipment Manufacturer (OEM), that was contractually locked into the original unique PIN. By establishing a one part number system covering all three documents, the OEM can acquire to the highest class level available for a given generic device to meet system needs without modifying the original contract parts selection criteria.

Military documentation format	Example PIN under new system	Manufacturing source listing	Document listing
New MIL-H-38534 Standard Microcircuit Drawings	5962-XXXXXZZ(H or K)YY	QML-38534	MIL-BUL-103
New MIL-PRF-38535 Standard Microcircuit Drawings	5962-XXXXXZZ(Q or V)YY	QML-38535	MIL-BUL-103
New 1.2.1 of MIL-STD-883 Standard Microcircuit Drawings	5962-XXXXXZZ(M)YY	MIL-BUL-103	MIL-BUL-103

6.7 Sources of supply.

6.7.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DESC-EC and have agreed to this drawing.

6.7.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-BUL-103. The vendors listed in MIL-BUL-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-EC.

6.8 Additional information. A copy of the following additional data shall be maintained and available from the device manufacturer:

a. RHA upset levels.

b. Test conditions (SEP).

c. Number of upsets (SEP).

d. Number of transients (SEP).

e. Occurence of latchup (SEP).