REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Added changes in accordance with NOR 5962-R159-97	96-12-20	Raymond Monnin
B	Change to Table I; I_{CCDR}, device type column. Updated boilerplate. ksr	98-02-18	Raymond Monnin

REV																			
SHEET																			
REV	B	B	B	B	B	B	B	B	B										
SHEET	15	16	17	18	19	20	21	22	23										

REV STATUS OF SHEETS	REV	B	B	B	B	B	B	B	B	B	B	B	B	B	B
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY
Gary L. Gross

CHECKED BY
Jeff Bowling

APPROVED BY
Michael A. Frye

DRAWING APPROVAL DATE
96-05-17

REVISION LEVEL
B

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 42316

MICROCIRCUIT, MEMORY, DIGITAL, 256K X 16 STATIC RANDOM ACCESS MEMORY (SRAM), MONOLITHIC SILICON

SIZE	CAGE CODE	
A	67268	**5962-96795**

SHEET 1 OF 23

DSCC FORM 2233
APR 97

5962-E077-98

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:

5962	-	96795	01	M	X	X
*	*		*	*	*	*
*	*		*	*	*	*
*	*		*	*	*	*
Federal stock class designator	RHA designator (see 1.2.1)		Device type (see 1.2.2)	Device class designator (see 1.2.3)	Case outline (see 1.2.4)	Lead finish (see 1.2.5)
\		/				
V						
Drawing number						

1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number 1/	Circuit function	Data retention	Access time
01		256K X 16 CMOS SRAM	No	35 ns
02		256K X 16 CMOS SRAM	No	25 ns
03		256K X 16 CMOS SRAM	No	20 ns
04		256K X 16 CMOS SRAM	Yes	35 ns
05		256K X 16 CMOS SRAM	Yes	25 ns
06		256K X 16 CMOS SRAM	Yes	20 ns

1.2.3 Device class designator. The device class designator shall be a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	See figure 1	44	flat package
Y	See figure 1	44	CSOJ package

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1/ Generic numbers are listed on the Standard Microcircuit Drawing Source Approval Bulletin at the end of this document and will also be listed in MIL-HDBK-103 (see 6.6.2 herein).

1.3 Absolute maximum ratings. 2/

Voltage on any input relative to V_{SS}	-0.5 V dc to +7.0 V dc
Storage temperature range	-65°C to +150°C
Maximum power dissipation (P_D)	1.5 W
Lead temperature (soldering, 10 seconds)	+260°C
Thermal resistance, junction-to-case (Θ_{JC}):	
Case X	5°C/W
Case Y	8°C/W
Junction temperature (T_J)	+150°C 3/
Output current	20 mA

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	4.5 V dc to 5.5 V dc
Supply voltage (V_{SS})	0 V
Input high voltage range (V_{IH})	2.2 V dc to V_{CC} + 0.5 V dc
Input low voltage range (V_{IL})	-0.3 V dc to +0.8 V dc 4/
Case operating temperature range (T_C)	-55°C to +125°C

1.5 Digital logic testing for device classes Q and V.

Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012)	5/ percent

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Interface Standard for Microcircuit Case Outlines.

HANDBOOKS

DEPARTMENT OF DEFENSE

MIL-HDBK-103 - List of Standard Microcircuit Drawings (SMD's).
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
3/ Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions in accordance with method 5004 of MIL-STD-883.
4/ V_{IL} minimum = -3.0 V dc for pulse width less than 20 ns.
5/ Values will be added when they become available.

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents which are DoD adopted are those listed in the issue of the DODISS cited in the solicitation. Unless otherwise specified, the issues of documents not listed in the DODISS are the issues of the documents cited in the solicitation.

AMERICAN SOCIETY FOR TESTING AND MATERIALS (ASTM)

ASTM Standard F1192-88 - Standard Guide for the Measurement of Single Event Phenomena from Heavy Ion Irradiation of Semiconductor Devices.

(Applications for copies of ASTM publications should be addressed to the American Society for Testing and Materials, 1916 Race Street, Philadelphia, PA 19103.)

ELECTRONICS INDUSTRIES ASSOCIATION (EIA)

JEDEC Standard No. 17 - A Standardized Test Procedure for the Characterization of Latch-up in CMOS Integrated Circuits.

(Applications for copies should be addressed to the Electronics Industries Association, 2500 Wilson Blvd., Arlington, VA 22201.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Truth table. The truth table shall be as specified on figure 3.

3.2.4 Functional tests. Various functional tests used to test this device are contained in the appendix. If the test patterns cannot be implemented due to test equipment limitations, alternate test patterns to accomplish the same results shall be allowed. For device class M, alternate test patterns shall be maintained under document revision level control by the manufacturer and shall be made available to the preparing or acquiring activity upon request. For device classes Q and V alternate test patterns shall be under the control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the preparing or acquiring activity upon request.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-973.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 41 (see MIL-PRF-38535, appendix A).

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Delete the sequence specified as initial (preburn-in) electrical parameters through interim (postburn-in) electrical parameters of method 5004 and substitute lines 1 through 6 of table IIA herein.

b. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. For device class M, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(1) Dynamic burn-in for device class M (method 1015 of MIL-STD-883, test condition D; for circuit, see 4.2.1b herein).

c. Interim and final electrical parameters shall be as specified in table IIA herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A Subgroups	Device type	Limits		Units
					Min	Max	
Operating supply current 1/	I_{CC1}	all I/O's = 0 mA, WE, CE = V_{IL}	1, 2, 3	All		300	mA
V_{CC} standby current (TTL)	I_{CC2}	CE = V_{IH}, $V_{IN} \le V_{IL}$ $V_{IN} \ge V_{IH}$	1, 2, 3	All		60	mA
V_{CC} standby current (CMOS)	I_{CC3}	CE $\ge V_{CC}$-0.2 V $V_{IN} \ge V_{CC}$-0.2 V or $V_{IN} < 0.2$ V	1, 2, 3	01-03		25	mA
				04-06		10	
Data retention voltage	V_{DR}	CE $\ge V_{CC}$-0.2 V, $V_{IN} \ge V_{CC}$-0.2 V or $V_{IN} \le 0.2$ V	1, 2, 3	04-06	-2.0		V
Data retention current	I_{CCDR}	V_{CC} = 2.0 V				2.0	mA
Input leakage current (low)	I_{ILK}	V_{IN} = 0.0 V to V_{CC}	1, 2, 3	All	-10	+10	µA
Output leakage current (high)	I_{OLK}	$V_{I/O}$ = 0.0 V to V_{CC}	1, 2, 3	All	-10	+10	µA
High level output voltage	V_{OH}	I_{OH} = -4.0 mA	1, 2, 3	All	2.4		V
Low level output voltage	V_{OL}	I_{OL} = 8.0 mA	1, 2, 3	All		0.4	V
Input capacitance	C_{IN}	V_{IN} = 0 V, T_A = 25°C, f = 1.0 MHz, see 4.4.1e	4	All		12	pF
Input/output capacitance	$C_{I/O}$	V_{OUT} = 0 V, T_A = 25°C, f = 1.0 MHz, see 4.4.1e	4	All		14	pF
Functional tests		See 4.4.1c	7, 8A, 8B	All			
Read cycle time	t_{AVAV}	See figures 4 and 5 as applicable 2/ 3/	9, 10, 11	01,04	35		ns
				02,05	25		
				03,06	20		

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A Subgroups	Device type	Limits		Units
					Min	Max	
Address access time	t_{AVQV}	See figures 4 and 5 as applicable 2/ 3/	9, 10, 11	01,04		35	ns
				02,05		25	
				03,06		20	
Chip enable access time	t_{ELQV}		9, 10, 11	01,04		35	ns
				02,05		25	
				03,06		20	
Chip enable to output in low Z	t_{ELQX}		9, 10, 11	All	5		ns
Chip disable to output in high Z	t_{EHQZ}		9, 10, 11	01,04	0	10	ns
				02,05		8	
				03,06		7	
Output hold from address change	t_{AVQX}		9, 10, 11	01,02 04,05	5		ns
				03,06	4		
Output enable to output valid	t_{OLQV}		9, 10, 11	01,04		15	ns
				02,05		12	
				03,06		10	
Output enable to output in low Z 4/	t_{OLQX}		9, 10, 11	All	0		ns
Output disable to output in high Z 4/	t_{OHQZ}		9, 10, 11	01,04	0	10	ns
				02,05		8	
				03,06		7	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A Subgroups	Device type	Limits		Units
					Min	Max	
LB, UB access time	t_{UBLQV} t_{LBLQV}	See figures 4 and 5 as applicable 2/ 3/	9, 10, 11	01,04		15	ns
				02,05		12	
				03,06		10	
LB, UB enable to low Z output	t_{UBLQX} t_{LBLQX}		9, 10, 11	All	0		ns
LB, UB disable to high Z output	t_{UBHQZ} t_{LBHQZ}		9, 10, 11	01,04	0	10	ns
				02,05		8	
				03,06		7	
Write cycle time	t_{AVAV}	See figures 4 and 5 as applicable 2/	9, 10, 11	01,04	35		ns
				02,05	25		
				03,06	20		
Chip enable to end of write	t_{ELWH} t_{ELEH}		9, 10, 11	01,04	20		ns
				02,05	17		
				03,06	15		
Address setup time	t_{AVWL} t_{AVEL} t_{AVUBL}		9, 10, 11	All	0		ns
Address valid to end of write	t_{AVWH} t_{AVEH} t_{AVUBH}		9, 10, 11	01,04	20		ns
				02,05	17		
				03,06	15		
Write pulse width	t_{WLWH} t_{WLEH}		9, 10, 11	01,04	20		ns
				02,05	17		
				03,06	15		

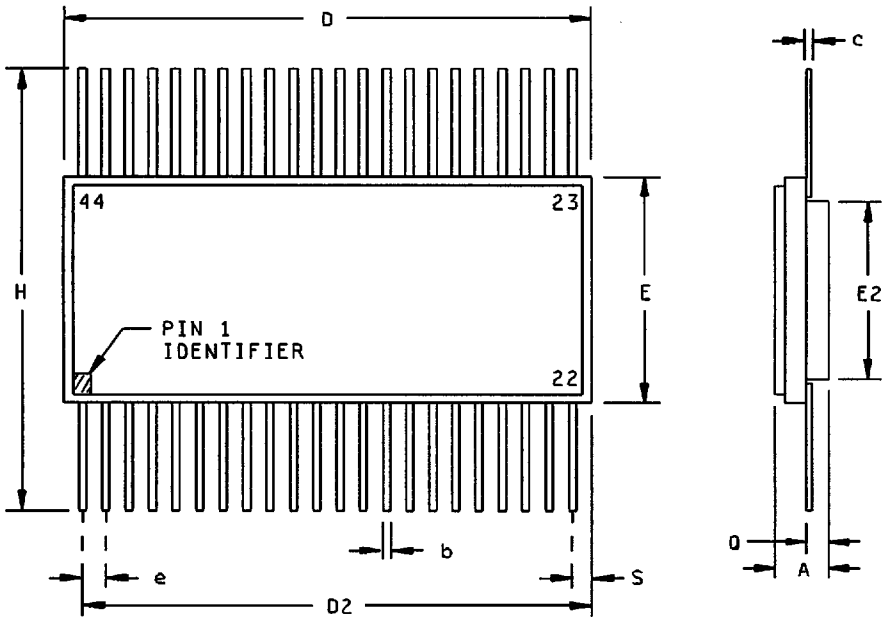
See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$, $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified	Group A Subgroups	Device type	Limits		Units
					Min	Max	
Write recovery time	t_{WHAX} t_{EHAX}	See figures 4 and 5 as applicable 2/	9, 10, 11	All	0		ns
Data hold time in high Z	t_{WHDX} t_{EHDX}		9, 10, 11	All	0		ns
Write to output in high Z	t_{WLQZ}		9, 10, 11	All	0	8	ns
Data to write time	t_{DVWH} t_{DVEH}		9, 10, 11	01,04	15		ns
				02,05	12		
				03,06	10		
Output active from end of write	t_{WHQX}		9, 10, 11	01,04	15		ns
				02,05	12		
				03,06	10		
LB, UB valid to end of write	t_{LBLLBH} t_{UBLUBH}		9, 10, 11	01,04	20		ns
				02,05	18		
				03,06	16		
Operation recovery time	t_R	See figures 4 and 5 as applicable 2/ $\overline{CE} \ge V_{CC}-0.2\ V$, $V_{IN} \ge V_{CC}-0.2\ v$ or $V_{IN} \le 0.2\ V$	9, 10, 11	04-06	t_{AVAV}		ns
Chip disable to data retention time	t_{CDR}		9, 10, 11	All	0		ns

1/ I_{CC} is dependent on output loading and cycle rate. The specified values apply with output(s) unloaded.
2/ AC measurements assume signal transition times of 5 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 V to 3.0 V and output loading of 30 pF load capacitance, unless otherwise specified. Output timing reference is 1.5 V. See figure 4.
3/ For read cycles, $\overline{WE}$ is high for the entire cycle.
4/ Parameter, if not tested, shall be guaranteed to the limits specified in table I.
5/ Measured ±500 mV from steady-state output voltage. Load capacitance is 5.0 pF.

Case X (see notes)

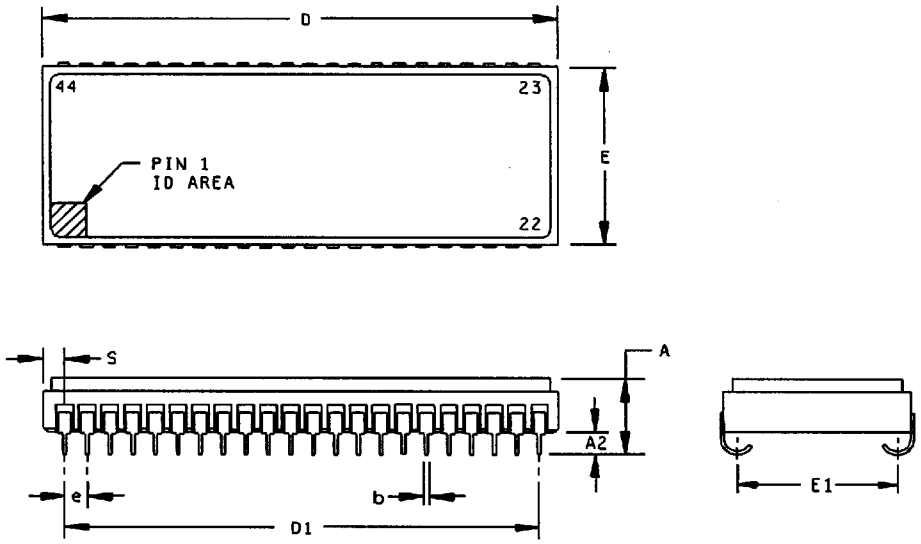


Symbol	Millimeters		Inches		Symbol	Millimeters		Inches	
	Min	Max	Min	Max		Min	Max	Min	Max
A	—	2.92	—	.115	E2	9.78	10.03	3.85	3.95
b	0.38	0.48	.015	.019	e	1.27 Typ.		.050 Typ.	
C	0.08	0.18	.003	.007	H	25.40 Ref.		1.000 Ref.	
D	—	28.70	—	1.130	Q	0.81	0.97	.032	.038
D2	26.67 Ref.		1.050 Ref.		S	0.38	1.14	.015	.045
E	12.83	13.08	.505	.515	N	44			

NOTES:
1. The U.S. Government preferred system of measurement is the metric SI system. However, since this item was originally designed using inch-pound units of measurement, in the event of conflict between the metric and inch-pound units, the inch-pound units shall take precedence. Metric equivalents are for general information only.
2. Index area: a notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the area shown. The manufacturer's identification shall not be used as pin one identification mark.

FIGURE 1. Case outlines.

Case Y (see notes)



Symbol	Millimeters		Inches		Symbol	Millimeters		Inches	
	Min	Max	Min	Max		Min	Max	Min	Max
A	---	4.44	---	.175	E	---	11.30	---	.445
A2	1.52 Ref.		.060 Ref.		E1	10.16 Nom.		.400 Nom.	
b	0.41	0.51	0.16	0.19	e	1.27 Bsc.		.050 Bsc.	
D	28.45	28.70	1.120	1.130	S	0.76	1.02	.030	.040
D1	26.67 Ref.		1.050 Ref.		N	44			

NOTES:
1. The U.S. Government preferred system of measurement is the metric SI system. However, since this item was originally designed using inch-pound units of measurement, in the event of conflict between the metric and inch-pound units, the inch-pound units shall take precedence. Metric equivalents are for general information only.
2. Index area: a notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the area shown. The manufacturer's identification shall not be used as pin one identification mark.

FIGURE 1. Case outlines - continued.

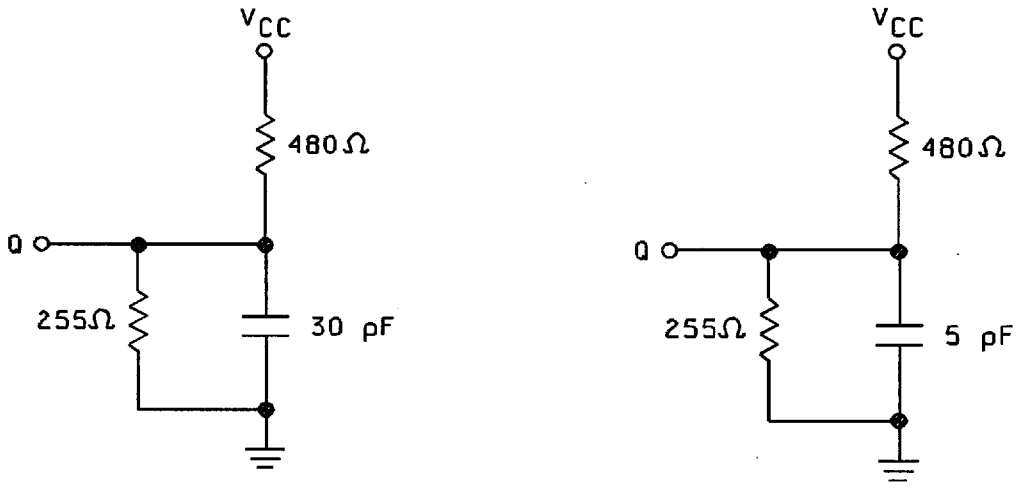
Device type	All		
Case outline	X, Y		
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	A0	23	A10
2	A1	24	A11
3	A2	25	A12
4	A3	26	A13
5	A4	27	A14
6	CE	28	NC
7	DQ1	29	DQ9
8	DQ2	30	DQ10
9	DQ3	31	DQ11
10	DQ4	32	DQ12
11	VCC	33	VCC
12	VSS	34	VSS
13	DQ5	35	DQ13
14	DQ6	36	DQ14
15	DQ7	37	DQ15
16	DQ8	38	DQ16
17	W	39	LB
18	A5	40	UB
19	A6	41	OE
20	A7	42	A15
21	A8	43	A16
22	A9	44	A17

FIGURE 2. Terminal connections.

CE	WE	OE	LB	UB	MODE	I/O PIN		SUPPLY CURRENT
						DQ_1-DQ_8	DQ_9-DQ_{16}	
H	X	X	X	X	NOT SELECT	HIGH-Z	HIGH-Z	I_{CC2},I_{CC3}
L	H	H	X	X	OUTPUT DISABLE	HIGH-Z	HIGH-Z	I_{CC}
L	X	X	H	H				
L	H	L	L	H	READ	D_{OUT}	HIGH-Z	I_{CC}
			H	L		HIGH-Z	D_{OUT}	
			L	H		D_{OUT}	D_{OUT}	
L	L	X	L	H	WRITE	D_{IN}	HIGH-Z	I_{CC}
			H	L		HIGH-Z	D_{IN}	
			L	L		D_{IN}	D_{IN}	

H = Logic "1" state
L = Logic "0" state
X = Don't care

FIGURE 3. Truth table.



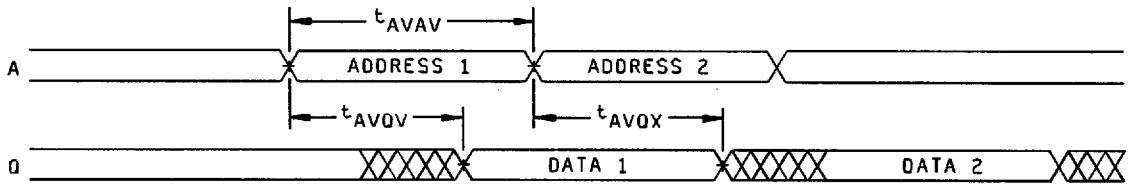
NOTES:
1. Use these output load circuits or equivalent for testing.
2. Including scope and jig.
3. Minimum of 5 pF for t_{EHQZ}, t_{WLQZ}, and t_{OHQZ}.

AC test conditions

Input pulse levels	VSS to 3.0 V
Input rise, fall times	5 ns
Input timing reference levels	1.5 V
Output reference levels	1.5 V

FIGURE 4. Output load circuits.

READ CYCLE NO. 1 (WE HIGH; OE, CE LOW)



READ CYCLE NO. 2 (WE HIGH)

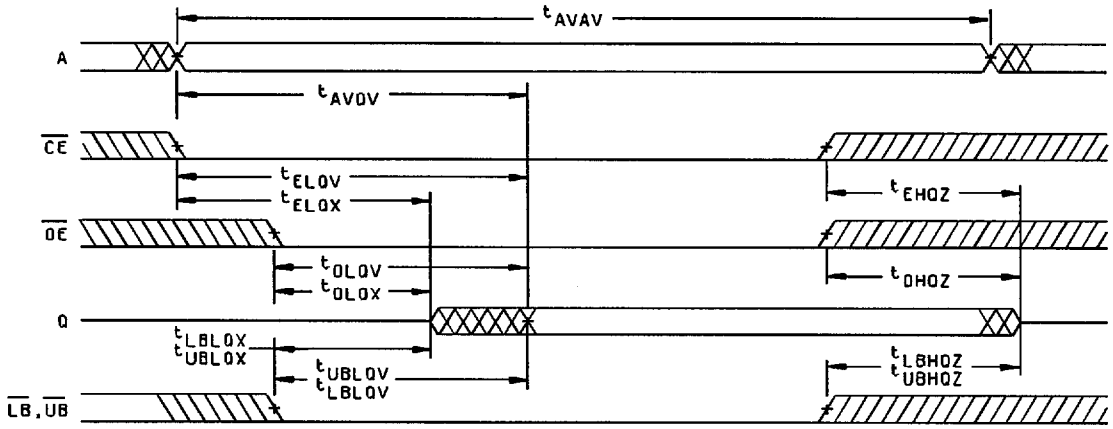
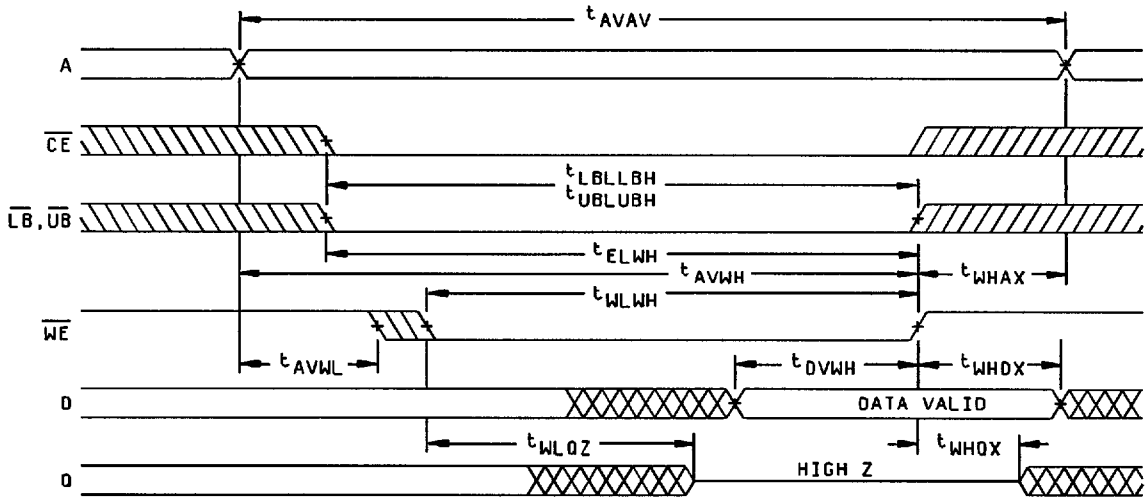


FIGURE 5. Timing waveforms.

WRITE CYCLE NO. 1 (WE CONTROLLED)



WRITE CYCLE NO. 2 (CE CONTROLLED)

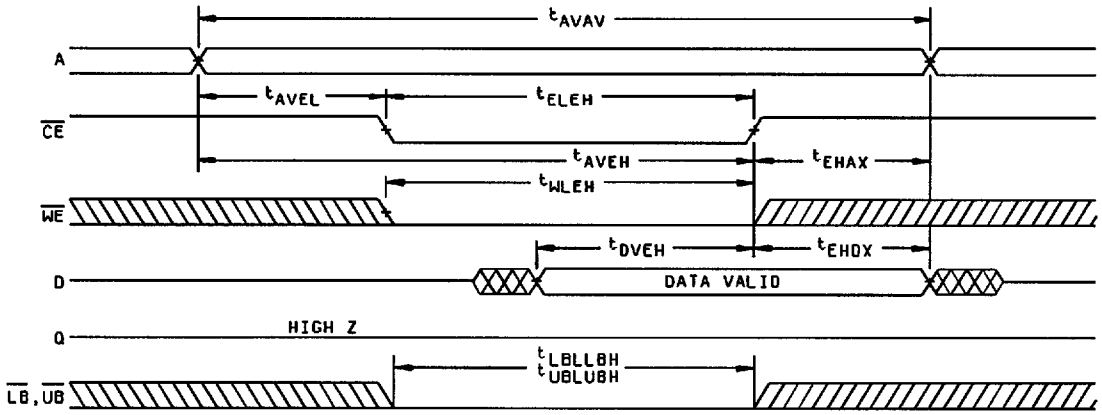
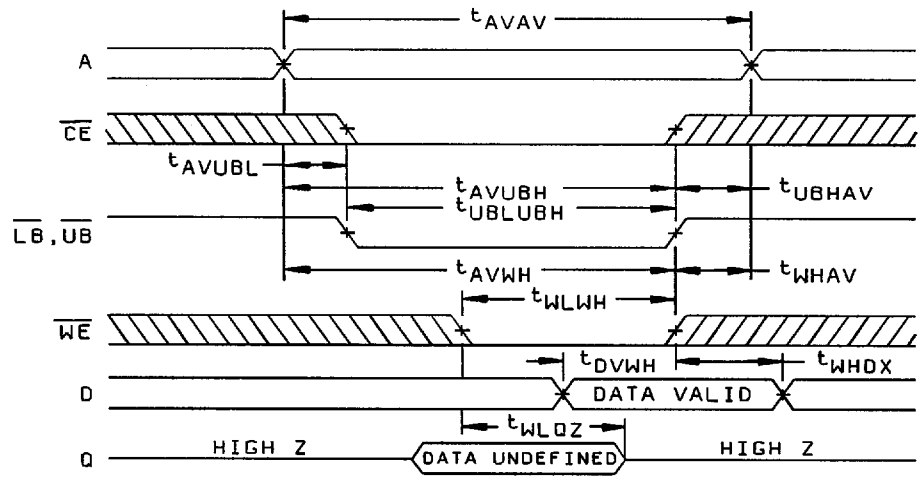


FIGURE 5. Timing waveforms - continued.

WRITE CYCLE NO. 3



DATA RETENTION WAVEFORM

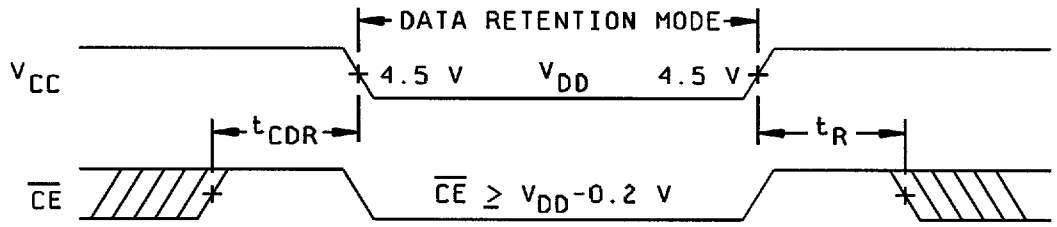


FIGURE 5. Timing waveforms - continued.

TABLE IIA. Electrical test requirements. 1/ 2/ 3/ 4/ 5/ 6/ 7/

Line no.	Test requirements	Subgroups (per method 5005, table I)	Subgroups (per MIL-PRF-38535, table III)	
		Device class M	Device class Q	Device class V
1	Interim electrical parameters (see 4.2)			1,7,9
2	Static burn-in I method 1015	Not required	Not required	Required
3	Same as line 1			1*,7* Δ
4	Dynamic burn-in (method 1015)	Required	Required	Required
5	Same as line 1			1*,7* Δ
6	Final electrical parameters	1*,2,3,7*,8A, 8B,9,10,11	1*,2,3,7*, 8A,8B,9,10, 11	1*,2,3,7*, 8A,8B,9,10, 11
7	Group A test requirements	1,2,3,4**,7,8 A,8B,9,10,11	1,2,3,4**,7, 8A,8B,9,10, 11	1,2,3,4**,7, 8A,8B,9,10, 11
8	Group C end-point electrical parameters	2,3,7, 8A,8B	1,2,3,7, 8A,8B	1,2,3,7, 8A,8B,9,10, 11 Δ
9	Group D end-point electrical parameters	2,3, 8A,8B	2,3, 8A,8B	2,3, 8A,8B
10	Group E end-point electrical parameters	1,7,9	1,7,9	1,7,9

1/ Blank spaces indicate tests are not applicable.
2/ Any or all subgroups may be combined when using high-speed testers.
3/ Subgroups 7 and 8 functional tests shall verify the truth table.
4/ * indicates PDA applies to subgroup 1 and 7.
5/ ** see 4.4.1e.
6/ Δ indicates delta limit (see table IIB) shall be required where specified, and the delta values shall be computed with reference to the previous interim electrical parameters (see line 1).
7/ See 4.4.1d.

TABLE IIB. Delta limits at +25°C.

Parameter 1/	All device types
I_{CC3} standby	±10% of specified value in table I
I_{ILK}, I_{OLK}	±10% of specified value in table I

1/ The above parameter shall be recorded before and after the required burn-in and life tests to determine the delta.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-PRF-38535 permits alternate in-line control testing. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 5 and 6 of table I of method 5005 of MIL-STD-883 shall be omitted.

c. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).

d. O/V (latch-up) tests shall be measured only for initial qualification and after any design or process changes which may affect the performance of the device. For device class M, procedures and circuits shall be maintained under document revision level control by the manufacturer and shall be made available to the preparing activity or acquiring activity upon request. For device classes Q and V, the procedures and circuits shall be under the control of the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the preparing activity or acquiring activity upon request. Testing shall be on all pins, on five devices with zero failures. Latch-up test shall be considered destructive. Information contained in JEDEC Standard number 17 may be used for reference.

e. Subgroup 4 (C_{IN} and $C_{I/O}$ measurements) shall be measured only for initial qualification and after any process or design changes which may affect input or output capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency of 1 MHz. Sample size is 15 devices with no failures, and all input and output terminals tested.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.
4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

4.5 Delta measurements for device class V. Delta measurements, as specified in table IIA, shall be made and recorded before and after the required burn-in screens and steady-state life tests to determine delta compliance. The electrical parameters to be measured, with associated delta limits are listed in table IIB. The device manufacturer may, at his option, either perform delta measurements or within 24 hours after burn-in perform final electrical parameter tests, subgroups 1, 7, and 9.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users shall inform Defense Supply Center Columbus, Ohio when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0525.

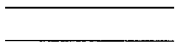
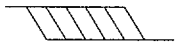
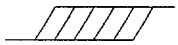
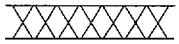
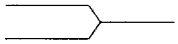
6.4 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43216-5000, or telephone (614) 692-0674.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535, MIL-STD-1331, and as follows:

C_{IN}, $C_{I/O}$	Input and bidirectional output, terminal-to-GND capacitance.
GND	Ground zero voltage potential.
I_{CC}	Supply current.
I_{ILK}	Input leakage current.
I_{OLK}	Output leakage current.
TC	Case temperature.
V_{CC}	Positive supply voltage.

6.5.1 Timing limits. The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

6.5.2 Waveforms.

Waveform symbol	Input	Output
	MUST BE VALID	WILL BE VALID
	CHANGE FROM H TO L	WILL CHANGE FROM H TO L
	CHANGE FROM L TO H	WILL CHANGE FROM L TO H
	DON'T CARE ANY CHANGE PERMITTED	CHANGING STATE UNKNOWN
		HIGH IMPEDANCE

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q, and V. Sources of supply for device classes Q, and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

APPENDIX

FUNCTIONAL ALGORITHMS

10. SCOPE

10.1 Scope. Functional algorithms are test patterns which define the exact sequence of events used to verify proper operation of a random access memory (RAM). Each algorithm serves a specific purpose for the testing of the device. It is understood that all manufacturers do not have the same test equipment; therefore, it becomes the responsibility of each manufacturer to guarantee that the test patterns described herein are followed as closely as possible, or equivalent patterns be used that serve the same purpose. Each manufacturer should demonstrate that this condition will be met. Algorithms shall be applied to the device in a topologically pure fashion. This appendix is a mandatory part of the specification. The information contained herein is intended for compliance.

20. APPLICABLE DOCUMENTS. This section is not applicable to this appendix.

30. ALGORITHMS

30.1 Algorithm A (pattern 1).

30.1.1 Checkerboard, checkerboard-bar.

Step 1. Load memory with a checkerboard data pattern by incrementing from location 0 to maximum.
Step 2. Read memory, verifying the output checkerboard pattern by incrementing from location 0 to maximum.
Step 3. Load memory with a checkerboard-bar pattern by incrementing from location 0 to maximum.
Step 4. Read memory, verifying the output checkerboard-bar pattern by incrementing from location 0 to maximum.

30.2 Algorithm B (pattern 2).

30.2.1 March.

Step 1. Load memory with background data, incrementing from minimum to maximum address locations (all "0's").
Step 2. Read data in location 0.
Step 3. Write complement data to location 0.
Step 4. Read complement data in location 0.
Step 5. Repeat steps 2 through 4 incrementing X-fast sequentially for each location in the array.
Step 6. Read complement data in maximum address location.
Step 7. Write data to maximum address location.
Step 8. Read data in maximum address location.
Step 9. Repeat steps 6 through 8 decrementing X-fast sequentially for each location in the array.
Step 10. Read data in location 0.
Step 11. Write complement data to location 0.
Step 12. Read complement data in location 0.
Step 13. Repeat steps 10 through 12 decrementing X-fast sequentially for each location in the array.
Step 14. Read complement data in maximum address location.
Step 15. Write data to maximum address location.
Step 16. Read data in maximum address location.
Step 17. Repeat steps 14 through 16 incrementing X-fast sequentially for each location in the array.
Step 18. Read background data from memory, decrementing X-fast from maximum to minimum address locations.

30.3 Algorithm C (pattern 3).

30.3.1 XY March.

Step 1. Load memory with background data, incrementing from minimum to maximum address locations (all "0's").
Step 2. Read data in location 0.
Step 3. Write complement data to location 0.
Step 4. Read complement data in location 0.
Step 5. Repeat steps 2 through 4 incrementing Y-fast sequentially for each location in the array.
Step 6. Read complement data in maximum address location.
Step 7. Write data to maximum address location.
Step 8. Read data in maximum address location.
Step 9. Repeat steps 6 through 8 decrementing X-fast sequentially for each location in the array.
Step 10. Read data in location 0.
Step 11. Write complement data to location 0.
Step 12. Read complement data in location 0.
Step 13. Repeat steps 10 through 12 decrementing Y-fast sequentially for each location in the array.
Step 14. Read complement data in maximum address location.
Step 15. Write data to maximum address location.
Step 16. Read data in maximum address location.
Step 17. Repeat steps 14 through 16 incrementing X-fast sequentially for each location in the array.
Step 18. Read background data from memory, decrementing Y-fast from maximum to minimum address locations.

30.4 Algorithm D (pattern 4).

30.4.1 CEDES - CE deselect checkerboard, checkerboard-bar.

Step 1. Load memory with a checkerboard data pattern by incrementing from location 0 to maximum.
Step 2. Deselect device, attempt to load memory with checkerboard-bar data pattern by incrementing from location 0 to maximum.
Step 3. Read memory, verifying the output checkerboard pattern by incrementing from location 0 to maximum.
Step 4. Load memory with a checkerboard-bar pattern by incrementing from location 0 to maximum.
Step 5. Deselect device, attempt to load memory with checkerboard data pattern by incrementing from location 0 to maximum.
Step 6. Read memory, verifying the output checkerboard-bar pattern by incrementing from location 0 to maximum.

STANDARD MICROCIRCUIT DRAWING SOURCE APPROVAL BULLETIN

DATE: 98-02-18

Approved sources of supply for SMD 5962-96795 are listed below for immediate acquisition only and shall be added to MIL-HDBK-103 during the next revision. MIL-HDBK-103 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9679501MXA	66301	EDI816256CA35F44B
5962-9679501MYA	66301	EDI816256CA35N44B
5962-9679502MXA	66301	EDI816256CA25F44B
5962-9679502MYA	66301	EDI816256CA25N44B
5962-9679503MXA	66301	EDI816256CA20F44B
5962-9679503MYA	66301	EDI816256CA20N44B
5962-9679504MXA	66301	EDI816256LPA35F44B
5962-9679504MYA	66301	EDI816256LPA35N44B
5962-9679505MXA	66301	EDI816256LPA25F44B
5962-9679505MYA	66301	EDI816256LPA25N44B
5962-9679506MXA	66301	EDI816256LPA20F44B
5962-9679506MYA	66301	EDI816256LPA20N44B

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
66301	Electronic Design Inc. 1 Research Drive Westborough, MA 01581-3906

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in this information bulletin.