REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																			
SHEET																			
REV																			
SHEET	15	16	17	18	19	20	21	22	23	24	25								

REV STATUS OF SHEETS	REV														
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

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DRAWING APPROVAL DATE
99 - 07 - 13

REVISION LEVEL

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 42316
http://www.dscc.dla.mil

MICROCIRCUIT, MEMORY, DIGITAL, CMOS, FIELD PROGRAMMABLE GATE ARRAY, 36,000 GATES, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**5962-99585**

SHEET 1 OF 25

DSCC FORM 2233
APR 97

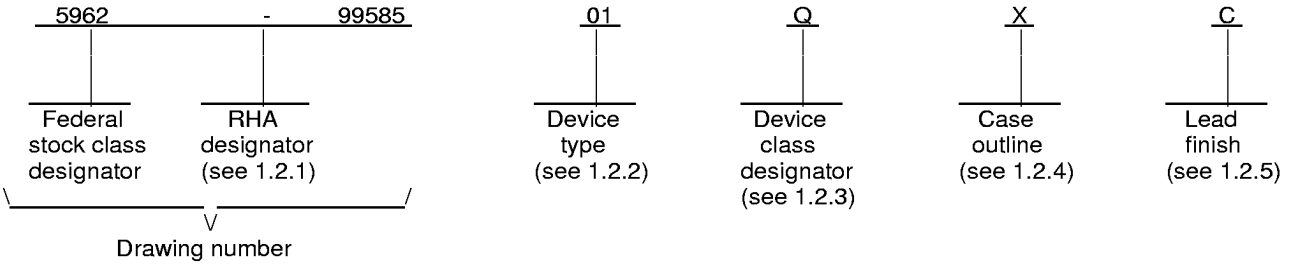
5962-E369-99

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN shall be as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function	Bin speed
01	A42MX36	36,000 gate field programmable gate array with 2,560 SRAM bits	148.5 ns 1/
02	A42MX36-1	36,000 gate field programmable gate array with 2,560 SRAM bits	122.0 ns 1/

1.2.3 Device class designator. The device class designator shall be a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	See figure 1	256	Ceramic Quad Flat Pack
Y	See figure 1	208	Ceramic Quad Flat Pack

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1/ Bin speed is tested at 125°C at 5 volts for worst case condition.

1.3 Absolute maximum ratings. 2/

DC supply voltage range (V_{CC})	-0.5 V dc to +7.0 V dc
Input voltage range (V_I)	-0.5 V dc to V_{CC}+0.5 V dc
Output voltage range (V_O)	-0.5 V dc to V_{CC}+0.5 V dc
I/O source sink current (I_{IO})	±20 mA
Storage temperature range (T_{STG})	-65°C to +150°C
Lead temperature (soldering, 10 seconds)	300°C
Thermal resistance, junction-to-case (Θ_{JC}) :	
Case X	8°C/W 3/
Case Y	9°C/W 3/
Maximum junction temperature (T_J)	+150°C

1.4 Recommended operating conditions.

3.3V Power supply for 3.3 V operation	+3.0 V dc to +3.6 V dc (±10% Vcc)
5.0V Power supply for 5.0 V operation	+4.5 V dc to +5.5 V dc (±10% Vcc)
Case operating temperature range (T_C)	-55°C to +125°C

1.5 Digital logic testing for device classes Q and V.

Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012)	100 percent 4/

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Interface Standard For Microcircuit Case Outlines.

HANDBOOKS

DEPARTMENT OF DEFENSE

MIL-HDBK-103 - List of Standard Microcircuit Drawings (SMD's).
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
3/ When the thermal resistance for this case is specified in MIL-STD-1835, that value shall supersede the value indicated herein.
4/ 100 percent test coverage of blank programmable logic devices.

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of the documents which are DoD adopted are those listed in the issue of the DODISS cited in the solicitation. Unless otherwise specified, the issues of documents not listed in the DODISS are the issues of the documents cited in the solicitation.

AMERICAN SOCIETY FOR TESTING AND MATERIALS (ASTM)

ASTM Standard F1192M-95 - Standard Guide for the Measurement of Single Event Phenomena from Heavy Ion Irradiation of Semiconductor Devices.

(Applications for copies of ASTM publications should be addressed to the American Society for Testing and Materials, 1916 Race Street, Philadelphia, PA 19103.)

ELECTRONICS INDUSTRIES ALLIANCE (EIA)

JEDEC Standard EIA/JESD 78 - IC Latch-Up Test.

(Applications for copies should be addressed to the Electronics Industries Association, 2500 Wilson Boulevard, Arlington, VA 22201.)

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein and on figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Truth table(s).

3.2.3.1 Unprogrammed devices. The truth table or test vectors for unprogrammed devices for contracts involving no altered item drawing is not part of this drawing. When required in screening (see 4.2 herein) or quality conformance inspection group A, B, C, D, or E (see 4.4 herein), the devices shall be programmed by the manufacturer prior to test. A minimum of 50 percent of the total number of logic modules shall be utilized or at least 25 percent of the total logic modules shall be utilized for any altered item drawing pattern.

3.2.3.2 Programmed devices. The truth table or test vectors for programmed devices shall be as specified by an attached altered item drawing.

3.2.4 Switching test circuit and waveforms . The switching test circuit and waveforms diagram shall be as specified on figure 3.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-973.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 42 (see MIL-PRF-38535, appendix A).

3.11 Processing options. Since the device is capable of being programmed by either the manufacturer or the user to result in a wide variety of configurations; two processing options are provided for selection in the contract, using an altered item drawing.

3.11.1 Unprogrammed device delivered to the user. All testing shall be verified through group A testing as defined in 4.4.1 and table IIA. It is recommended that users perform subgroups 7 and 9 after programming to verify the specific program configuration.

3.11.2 Manufacturer-programmed device delivered to the user. All testing requirements and quality assurance provisions herein, including the requirements of the altered item drawing, shall be satisfied by the manufacturer prior to delivery.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Delete the sequence specified as initial (pre-burn-in) electrical parameters through interim (post-burn-in) electrical parameters of method 5004 and substitute lines 1 through 6 of table IIA herein.

b. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. For device class M the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(1) Dynamic burn-in for device class M (method 1015 of MIL-STD-883, test condition D; for circuit, see 4.2.1b herein).

c. Interim and final electrical test parameters shall be as specified in table IIA herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-PRF-38535 permits alternate in-line control testing. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. Subgroups 5 and 6 of table I of method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for initial qualification and after any process or design changes which may affect input or output capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency less than 1 MHz. Sample size is five devices with no failures on a minimum of ten worst case pins from each device.

d. O/V (latch-up) tests shall be measured only for initial qualification and after any design or process changes which may affect the performance of the device. For device class M procedures and circuits shall be maintained under document revision level control by the manufacturer and shall be made available to the preparing activity or acquiring activity upon request. For device classes Q and V, the procedures and circuits shall be under the control of the device manufacturer's technical review board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the preparing activity or acquiring activity upon request. Testing shall be on all pins, on 5 devices with zero failures. Latch-up test shall be considered destructive. Information contained in JEDEC Standard EIA/JESD 78 may be used for reference.

e. Programmed device (see 3.2.3.2) - For device class M, subgroups 7, 8A, and 8B tests shall consist of verifying the functionality of the device. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device. These tests shall have been fault graded in accordance with MIL-STD-883, test method 5012.

f. Unprogrammed devices shall be tested for programmability and dc and ac performance compliance to the requirements of group A, subgroups 1 and 7.

(1) A sample shall be selected from each wafer lot to satisfy programmability requirements. Eight devices shall be submitted to programming (see 3.2.3.1). If any device fails to program, the lot shall be rejected. At the manufacturer's option, the sample may be increased to 18 total devices with no more than two total device failures allowable.

(2) These eight devices shall also be submitted to the requirements of the specified tests of group A, subgroups 1 and 7. If any device fails, the lot shall be rejected. At the manufacturer's option, the sample may be increased to 18 total devices with no more than two total device failures allowable.

(3a) Eight devices from the programmability sample shall be submitted to the requirements of group A, subgroups 9 for binning circuit delay only. If any device fails, the lot shall be rejected. At the manufacturer's option, the sample may be increased to 18 total devices with no more than two total device failures allowable.

(3b) If the binning circuit is tested on 100 percent of the products, then the above requirement (3a) is met.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB, in accordance with MIL-PRF-38535, and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

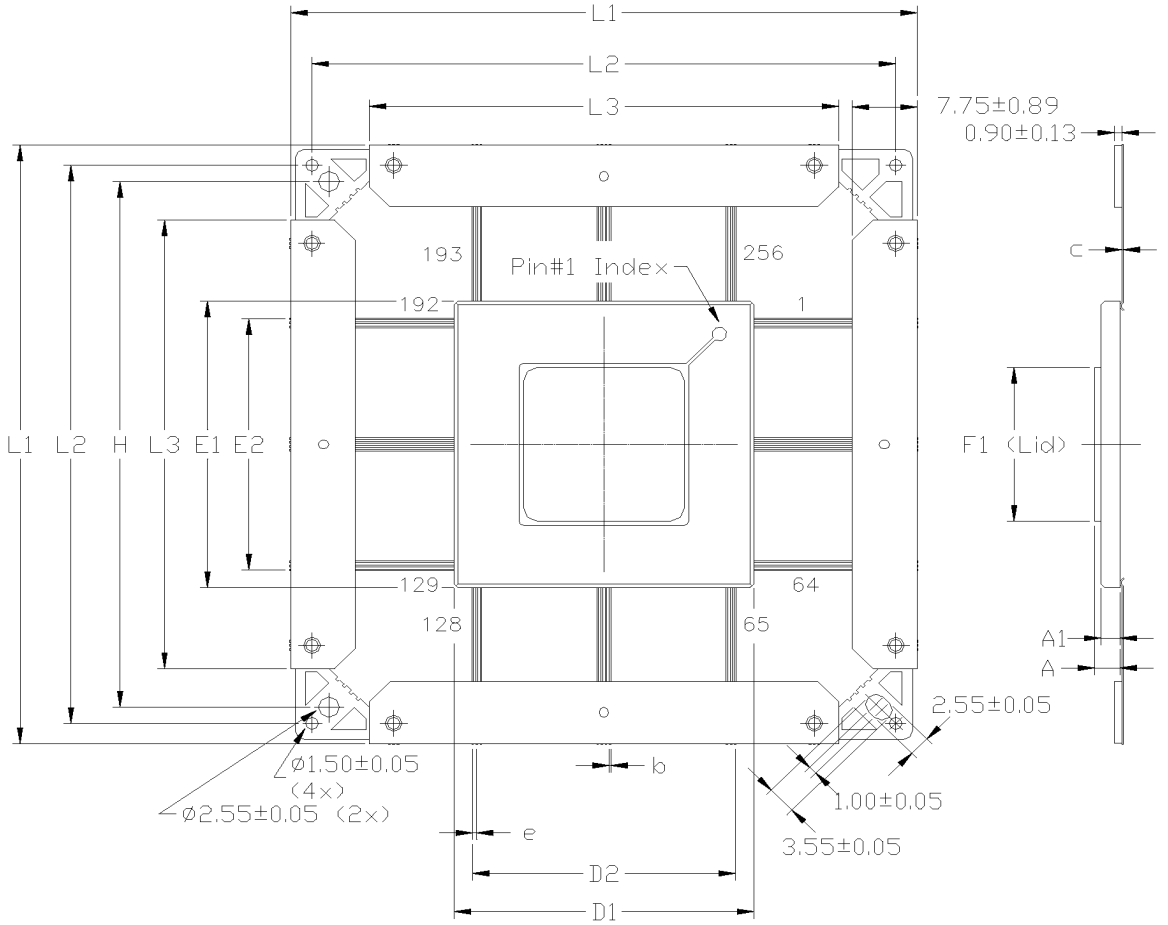
c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $4.5\ V \le V_{CC} \le 5.5\ V$ or $3.0\ V \le V_{CC} \le 3.6\ V$ $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A Subgroups	Device type	Limits		Unit
					Min	Max	
High Level output voltage	V_{OH}	V_{CC} = 3.0 V or 4.5 V, I_{OH} = -4 mA	1, 2, 3	All	3.7		V
Low level output voltage	V_{OL}	V_{CC} = 4.5 V I_{OL} = 6 mA	1, 2, 3	All		0.40	V
		V_{CC} = 3.0 V I_{OL} = 6 mA				0.48	
Low level input voltage	V_{IL}		1, 2, 3	All	-0.3	0.8	V
High level input voltage	V_{IH}		1, 2, 3	All	2.0	V_{CC} +0.3	V
Standby supply current	I_{CC}	I_O = 0 mA $V_{IN} = V_{CC}$ or GND	1, 2, 3	All		25	mA
Input leakage current	I_{IL}	$V_{IN} = V_{CC}$ or GND	1, 2, 3	All	-10	10	µA
Output leakage current	I_{OZ}	$V_O = V_{CC}$ or GND	1, 2, 3	All	-10	10	µA
I/O terminal capacitance	$C_{I/O}$	See 4.4.1c, f < 1.0 Mhz, V_{OUT} = 0 V	4	All		20	pF
Functional tests	FT 2/	See 4.4.1e	7, 8A, 8B	All			
Binning circuit delay	t_{PBLH}, t_{PBHL}	See figure 3, V_{IL} = 0 V, V_{IH} = 3.0 V, V_{CC} = 4.5 V, V_{OUT} = 1.5 V 3/	9, 10, 11	01		148.5	ns
				02		122.0	ns

1/ All tests shall be performed under the worst case condition unless otherwise specified.
2/ Devices are functionally tested using a serial scan test method. Data is shifted into the TDI pin and the TCK pin is used as a clock. The data is used to drive the inputs of the internal logic and I/O modules, allowing a complete functional test to be performed. The outputs of the module can be read by shifting out the output response or by monitoring the PRA, PRB, or TDO pins. These tests form a part of the manufacturers's test tape and shall be maintained and available at the approved source(s) of supply upon request by DSCC or the OEM.
3/ Binning circuit delay is defined as the input-to-output delay of a special path called the "binning circuit". The binning circuit consists of one input buffer plus 16 combinatorial logic modules plus one output buffer. The logic modules are distributed along the left side of the device. These modules are configured as non-inverting buffers and are connected through programmed antifuses with typical capacitive loading.

Case Outline X



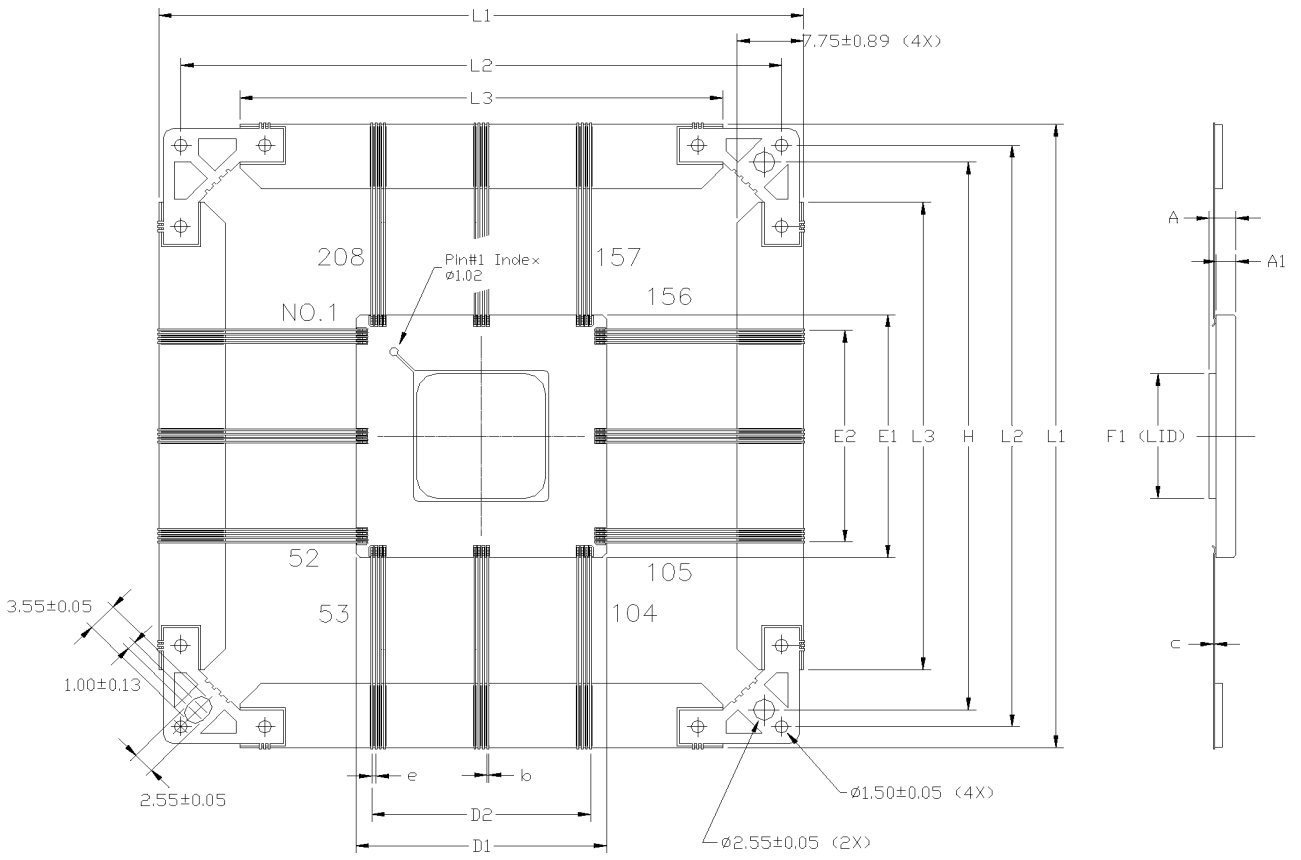
Symbol	Dimension (unit : mm)		
	Min.	Nom	Max.
A	2.42	2.80	3.18
A1	2.04	2.29	2.54
b	0.18	0.20	0.23
c	0.10	0.15	0.18
D1/E1	35.64	36.00	36.36
D2/E2	31.50 BSC		
e	0.50 BSC		
F1	19.43	19.56	19.69
L1	74.60	75.00	75.40
L2	69.87	70.00	70.13
L3	55.80	56.30	56.80
H	65.77	65.90	66.03
Weight	13 gm (typical)		

NOTES:

1. All exposed metalized areas and leads are gold plated 100 microinches (2.5 micrometer) minimum thickness over 80 to 350 microinches (2.0 to 8.9 micrometer) thickness nickel.
2. Seal ring area is connected to GND.
3. Die attach pad is connected to GND.
4. 13 gm weight is measured after tie-bar removed.
5. Tie-bar dimensions are for reference only.

FIGURE 1. Case outlines.

Case Outline Y



	Dimension (unit : mm)		
Symbol	Min.	Nom.	Max.
A	2.42	2.80	3.18
A1	2.04	2.29	2.54
b	0.18	0.20	0.23
c	0.10	0.15	0.18
D1/E1	28.96	29.21	29.46
D2/E2		25.50	
e		0.50 BSC	
F1	19.43	19.56	19.69
L1	74.60	75.00	75.40
L2	69.87	70.00	70.13
L3	55.80	56.30	56.80
H	65.77	65.90	66.03
Weight		8.6 gm (typical)	

NOTES:

1. All exposed metalized areas and leads are gold plated 100 microinches (2.5 μm) minimum thickness over 80 to 350 microinches (2.0 to 8.9 μm) thickness nickel.
2. Seal ring area is connected to GND.
3. Die attach pad is connected to GND.
4. 8.6 gm weight is measured after tie-bar removed.
5. Tie-bar dimensions are for reference only.

FIGURE 1. Case outlines.- Continued.

Case Outline X

Device Types	All	Device Types	All	Device Types	All
Terminal Number	Terminal Symbol	Terminal Number	Terminal Symbol	Terminal Number	Terminal Symbol
1	NC	44	I/O	87	I/O (WD)
2	GND	45	I/O	88	I/O (WD)
3	I/O	46	I/O	89	I/O
4	I/O	47	I/O	90	I/O
5	I/O	48	GND	91	I/O
6	I/O	49	I/O	92	I/O
7	I/O	50	I/O	93	I/O
8	I/O	51	I/O	94	I/O
9	I/O	52	I/O	95	VCCI
10	GND	53	I/O	96	VCCA
11	I/O	54	I/O	97	GND
12	I/O	55	I/O	98	GND
13	I/O	56	I/O	99	I/O
14	I/O	57	I/O	100	I/O
15	I/O	58	I/O	101	I/O
16	I/O	59	I/O	102	I/O
17	I/O	60	VCCA	103	I/O
18	I/O	61	GND	104	I/O
19	I/O	62	GND	105	I/O (WD)
20	I/O	63	NC	106	I/O (WD)
21	I/O	64	NC	107	I/O
22	I/O	65	NC	108	I/O
23	I/O	66	I/O	109	I/O (WD)
24	I/O	67	TDO, I/O	110	I/O (WD)
25	I/O	68	I/O	111	I/O
26	VCCA	69	I/O (WD)	112	QCLKA, I/O
27	I/O	70	I/O (WD)	113	I/O
28	I/O	71	I/O	114	GND
29	VCCA	72	VCCI	115	I/O
30	VCCI	73	I/O	116	I/O
31	GND	74	I/O	117	I/O
32	VCCA	75	I/O	118	I/O
33	GND	76	I/O (WD)	119	VCCI
34	TCK, I/O	77	GND	120	I/O
35	I/O	78	I/O (WD)	121	I/O (WD)
36	GND	79	I/O	122	I/O (WD)
37	I/O	80	QCLKB, I/O	123	I/O
38	I/O	81	I/O	124	I/O
39	I/O	82	I/O	125	TDI, I/O
40	I/O	83	I/O	126	TMS, I/O
41	I/O	84	I/O	127	GND
42	I/O	85	I/O	128	NC
43	I/O	86	I/O	129	NC

FIGURE 2. Terminal connections.

Device Types	All	Device Types	All	Device Types	All
Terminal Number	Terminal Symbol	Terminal Number	Terminal Symbol	Terminal Number	Terminal Symbol
130	NC	173	I/O	216	I/O (WD)
131	GND	174	I/O	217	I/O
132	I/O	175	I/O	218	PRB, I/O
133	I/O	176	I/O	219	I/O
134	I/O	177	I/O	220	CLKB, I/O
135	I/O	178	I/O	221	I/O
136	I/O	179	I/O	222	GND
137	I/O	180	GND	223	GND
138	I/O	181	I/O	224	VCCA
139	GND	182	I/O	225	VCCI
140	I/O	183	I/O	226	I/O
141	I/O	184	I/O	227	CLKA, I/O
142	I/O	185	I/O	228	I/O
143	I/O	186	I/O	229	PRA, I/O
144	I/O	187	I/O	230	I/O
145	I/O	188	MODE	231	I/O
146	I/O	189	VCCA	232	I/O (WD)
147	I/O	190	GND	233	I/O (WD)
148	I/O	191	NC	234	I/O
149	I/O	192	NC	235	I/O
150	I/O	193	NC	236	I/O
151	I/O	194	I/O	237	I/O
152	I/O	195	DCLK, I/O	238	I/O
153	I/O	196	I/O	239	I/O
154	I/O	197	I/O	240	QCLKD, I/O
155	VCCA	198	I/O	241	I/O
156	I/O	199	I/O (WD)	242	I/O (WD)
157	I/O	200	I/O (WD)	243	GND
158	VCCA	201	VCCI	244	I/O (WD)
159	VCCI	202	I/O	245	I/O
160	GND	203	I/O	246	I/O
161	I/O	204	I/O	247	I/O
162	I/O	205	I/O	248	VCCI
163	I/O	206	GND	249	I/O
164	I/O	207	I/O	250	I/O (WD)
165	GND	208	I/O	251	I/O (WD)
166	I/O	209	QCLKC, I/O	252	I/O
167	I/O	210	I/O	253	SDI, I/O
168	I/O	211	I/O (WD)	254	I/O
169	I/O	212	I/O (WD)	255	GND
170	VCCA	213	I/O	256	NC
171	I/O	214	I/O		
172	I/O	215	I/O (WD)		

FIGURE 2. Terminal connections. - Continued.

Case Outline Y

Device Types	All	Device Types	All	Device Types	All
Terminal Number	Terminal Symbol	Terminal Number	Terminal Symbol	Terminal Number	Terminal Symbol
1	GND	36	I/O	71	I/O (WD)
2	VCCA	37	I/O	72	I/O
3	MODE	38	I/O	73	I/O
4	I/O	39	I/O	74	I/O
5	I/O	40	I/O	75	I/O
6	I/O	41	I/O	76	I/O
7	I/O	42	I/O	77	I/O
8	I/O	43	I/O	78	GND
9	I/O	44	I/O	79	VCCA
10	I/O	45	I/O	80	VCCI
11	I/O	46	I/O	81	I/O
12	I/O	47	I/O	82	I/O
13	I/O	48	I/O	83	I/O
14	I/O	49	I/O	84	I/O
15	I/O	50	I/O	85	I/O (WD)
16	I/O	51	I/O	86	I/O (WD)
17	VCCA	52	GND	87	I/O
18	I/O	53	GND	88	I/O
19	I/O	54	TMS, I/O	89	I/O
20	I/O	55	TDI, I/O	90	I/O
21	I/O	56	I/O	91	QCLKB, I/O
22	GND	57	I/O (WD)	92	I/O
23	I/O	58	I/O (WD)	93	I/O (WD)
24	I/O	59	I/O	94	I/O (WD)
25	I/O	60	VCCI	95	I/O
26	I/O	61	I/O	96	I/O
27	GND	62	I/O	97	I/O
28	VCCI	63	I/O	98	VCCI
29	VCCA	64	I/O	99	I/O
30	I/O	65	QCLKA, I/O	100	I/O (WD)
31	I/O	66	I/O (WD)	101	I/O (WD)
32	VCCA	67	I/O (WD)	102	I/O
33	I/O	68	I/O	103	TDO, I/O
34	I/O	69	I/O	104	I/O
35	I/O	70	I/O (WD)	105	GND

FIGURE 2. Terminal Connections. - Continued.

Device Types	All	Device Types	All	Device Types	All
Terminal Number	Terminal Symbol	Terminal Number	Terminal Symbol	Terminal Number	Terminal Symbol
106	VCCA	141	I/O	176	I/O (WD)
107	I/O	142	I/O	177	I/O (WD)
108	I/O	143	I/O	178	PRA, I/O
109	I/O	144	I/O	179	I/O
110	I/O	145	I/O	180	CLKA, I/O
111	I/O	146	I/O	181	I/O
112	I/O	147	I/O	182	VCCI
113	I/O	148	I/O	183	VCCA
114	I/O	149	I/O	184	GND
115	I/O	150	GND	185	I/O
116	I/O	151	I/O	186	CLKB, I/O
117	I/O	152	I/O	187	I/O
118	I/O	153	I/O	188	PRB, I/O
119	I/O	154	I/O	189	I/O
120	I/O	155	I/O	190	I/O (WD)
121	I/O	156	I/O	191	I/O (WD)
122	I/O	157	GND	192	I/O
123	I/O	158	I/O	193	I/O
124	I/O	159	SDI, I/O	194	I/O (WD)
125	I/O	160	I/O	195	I/O (WD)
126	GND	161	I/O (WD)	196	QCLKC, I/O
127	I/O	162	I/O (WD)	197	I/O
128	TCK, I/O	163	I/O	198	I/O
129	GND (LP)	164	VCCI	199	I/O
130	VCCA	165	I/O	200	I/O
131	GND	166	I/O	201	I/O
132	VCCI	167	I/O	202	VCCI
133	VCCA	168	I/O (WD)	203	I/O (WD)
134	I/O	169	I/O (WD)	204	I/O (WD)
135	I/O	170	I/O	205	I/O
136	VCCA	171	QCLKD, I/O	206	I/O
137	I/O	172	I/O	207	DCLK, I/O
138	I/O	173	I/O	208	I/O
139	I/O	174	I/O		
140	I/O	175	I/O		

FIGURE 2. Terminal Connections. - Continued.

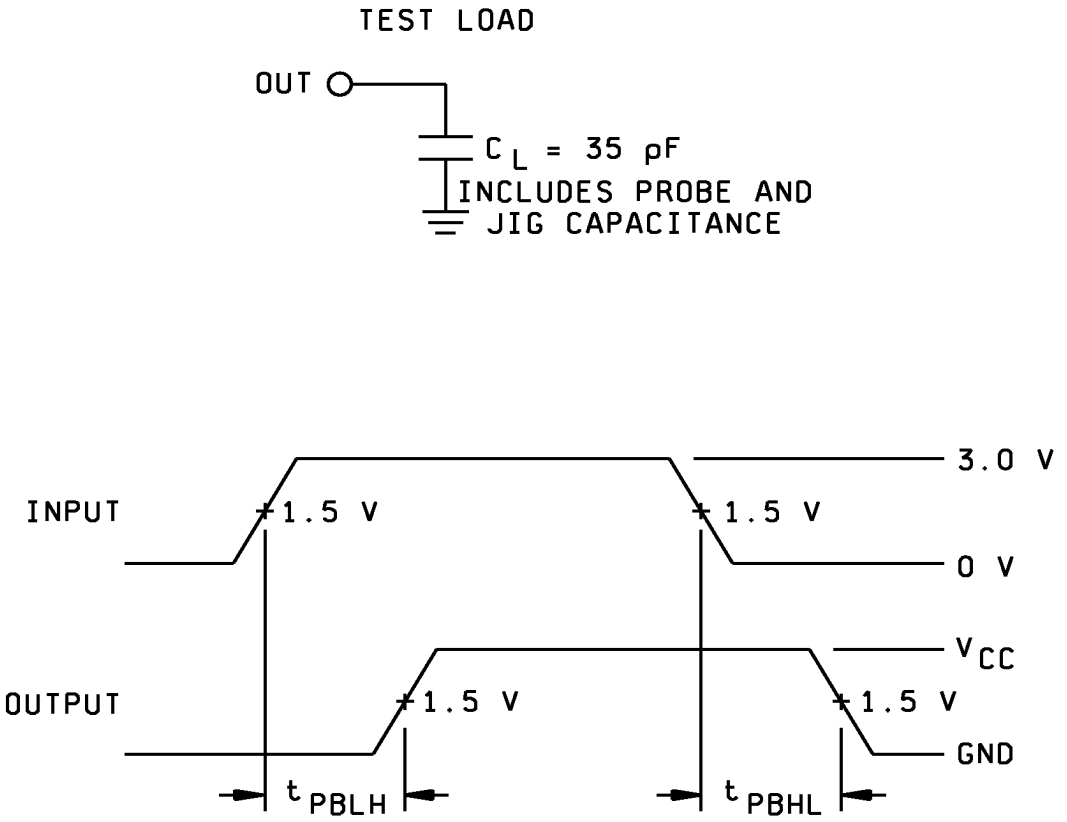


FIGURE 3. Switching test circuit and waveforms.

TABLE IIA. Electrical test requirements. 1/ 2/ 3/ 4/ 5/ 6/ 7/

Line no.	Test requirements	Subgroups (in accordance with MIL-STD-883, TM 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
		Device class M	Device class Q	Device class V
1	Interim electrical parameters (see 4.2)			1, 7, 9
2	Static burn-in (method 1015)	Not required	Not required	Required
3	Same as line 1			1*, 7* Δ
4	Dynamic burn-in (method 1015)	Required	Required	Required
5	Same as line 1			1*, 7* Δ
6	Final electrical parameters (see 4.2)	1*, 2, 3, 7*, 8A,8B,910,11	1*, 2, 3, 7*, 8A,8B, 9, 10, 11	1*, 2, 3, 7*, 8A,8B, 9, 10, 11
7	Group A test requirements (see 4.4)	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11
8	Group C end-point electrical parameters (see 4.4)	2, 3, 7, 8A, 8B	2, 3, 7, 8A, 8B	1, 2, 3, 7, 8A, 8B, 9, 10, 11 Δ
9	Group D end-point electrical parameters (see 4.4)	2, 3, 8A, 8B	2, 3, 8A, 8B	2, 3, 8A, 8B
10	Group E end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9	1, 7, 9

1/ Blank spaces indicate tests are not applicable.
2/ Any or all subgroups may be combined when using high-speed testers.
3/ Subgroups 7 and 8 functional tests shall verify the functionality for unprogrammed devices or that the altered item drawing pattern exists for programmed devices.
4/ * indicates PDA applies to subgroup 1 and 7.
5/ ** see 4.4.1c.
6/ Δ indicates delta limit (see table IIB) shall be required where specified, and the delta values shall be computed with reference to the previous interim electrical parameters (see line 1).
7/ See 4.4.1d.

TABLE IIB. Delta limits at +25°C.

Parameter 1/	Device types
	All
I_{CC}	±1 mA of specified value of table I
I_{OZ}	±2 μA of specified value of table I
t_{PBLH}, t_{PBHL}	±10 ns

1/ The above parameter shall be recorded before and after the required burn-in and life tests to determine the delta.

4.5 Delta measurements for device class V. Delta measurements, as specified in table IIA, shall be made and recorded before and after the required burn-in screens and steady-state life tests to determine delta compliance. The electrical parameters to be measured, with associated delta limits are listed in table IIB. The device manufacturer may, at his option, either perform delta measurements or within 24 hours after burn-in perform final electrical parameter tests, subgroups 1, 7, and 9.

4.6 Programming procedures. The programming procedures shall be as specified by the device manufacturer and shall be made available upon request.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0525.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA , Columbus, Ohio 43216-5000, or telephone (614) 692-0674.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-STD-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

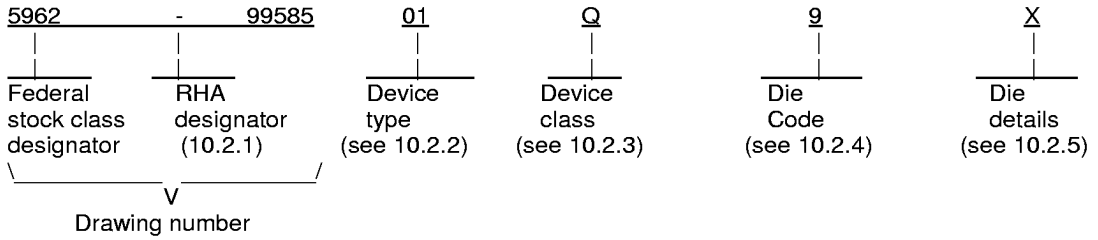
Appendix A

Appendix A forms a part of SMD 5962- 99585

10. Scope

10.1 Scope. This appendix establishes minimum requirements for microcircuit die to be supplied under the Qualified Manufacturers List (QML) Program. QML microcircuit die meeting the requirements of MIL-PRF-38535 and the manufacturers approved QML plan for use in monolithic microcircuits, multichip modules (MCMs), hybrids, electronic modules, or devices using chip and wire designs in accordance with MIL-PRF-38534 are specified herein. Two product assurance classes consisting of military high reliability (device class Q) and space application (device Class V) are reflected in the Part or Identification Number (PIN). When available a choice of Radiation Hardiness Assurance (RHA) levels are reflected in the PIN.

10.2
PIN. The PIN is as shown in the following example:



10.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

10.2.2 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function	Bin speed
01	A42MX36	36,000 gate field programmable gate array with 2,560 SRAM bits	148.5 ns

10.2.3 Device class designator. The device class designator shall be a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
Q or V	Certification and qualification to MIL-PRF-38535

10.2.4 Die code. The die code designator shall be a number 9 for all devices supplied as die only with no case outline.

10.2.5 Die details. The die details designation shall be a unique letter which designates the die's physical dimensions, bonding pad location(s) and related electrical function(s), interface materials, and other assembly related information, for each product and variant supplied to this appendix.

10.2.5.1 Die physical dimensions.

Device type	Die size	Die thickness	Die Detail	Figure Number
01	426.4 mils X 324.1 mils 1/	19±1 mils	A	A-1

1/ Add an additional 4.0 mil (100 micron) for scribeline area.

10.2.5.2 Die bonding pad locations and electrical functions.

Device type	Die Detail	Figure Number
01	A	A-1

10.2.5.3 Interface materials.

Device type	Top metalization	Backside metalization	Die Detail	Figure Number
01	Ti-cap+Al/Cu/Si,9KÅ	None (backgrind)	A	A-1

10.2.5.4 Assembly related information.

Device type	Glassivation	Die Detail	Figure Number
01	Oxide/Nitride	A	A-1

10.2.5.5 Wafer fabrication source.

Device type	Source	Die Detail	Figure Number
01	Chartered Semiconductor, Singapore	A	A-1

10.3 Absolute maximum ratings. See paragraph 1.3 within the body of this drawing for details.

10.4 Recommended operating conditions. See paragraph 1.4 within the body of this drawing for details.

20. APPLICABLE DOCUMENTS.

20.1 Government specification, standards, and handbooks. Unless otherwise specified, the following specification, standard, and handbook of the issue listed in that issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, form a part of this drawing to the extent specified herein.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Method Standard Microcircuits.

HANDBOOKS

DEPARTMENT OF DEFENSE

MIL-HDBK-103 - List of Standard Microcircuit Drawings (SMD's).

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

20.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

30. REQUIREMENTS.

30.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-389535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The Modification in the QM plan shall not effect the form, fit or function as described herein.

30.2 Design, construction and physical dimensions. The design, construction and physical dimensions shall be as specified in MIL-PRF-38535 and the manufacturer's QM plan, for device classes Q and V and herein.

30.2.1 Die physical dimensions. The die physical dimensions shall be specified in 10.2.5.1 and on figure A-1.

30.2.2 Die bonding pad locations and electrical functions. The die bonding pad locations and electrical functions shall be as specified in 10.2.5.2 and on figure A-1.

30.2.3 Interface materials. The interface materials for the die shall be as specified in 10.2.5.3 and on figure A-1.

30.2.4 Assembly related information. The assembly related information shall be as specified in 10.2.5.4 and figure A-1.

30.2.5 Truth table(s). Where technically applicable, (for die) the truth table(s) shall be as defined within paragraph 3.2.3 of the body of this document.

30.3 Electrical performance characteristics and post-irradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and post-irradiation parameter limits are as specified in table I of the body of this document.

30.4 Electrical test requirements. The wafer probe test requirements shall include functional and parametric testing sufficient to make the packaged die capable of meeting the electrical performance requirements in table I.

30.5 Marking. As a minimum, each unique lot of die, loaded in single or multiple stack of carriers, for shipment to a customer, shall be identified with the wafer lot number, the certification mark, the manufacturer's identification and the PIN listed in 10.2 herein. The certification mark shall be "QML" or "Q" as required by MIL-PRF-38535.

30.6 Certification of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 60.4 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this appendix shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and the requirements herein.

30.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuit die delivered to this drawing.

30.8 Processing options. Since the device is capable of being programmed by either the manufacturer or the user to result in a wide variety of configurations; two processing options are provided for selection in the contract, using an altered item drawing.

30.8.1 Unprogrammed die delivered to the user. All testing shall be verified through wafer probe test as defined in 40.2.

30.8.2 Manufacturer-programmed die delivered to the user. The programming integrity test shall be performed during programming. It is recommended that users perform subgroups 7 and 9 after programming to verify the specific program configuration.

40. QUALITY ASSURANCE PROVISIONS

40.1 Sampling and inspection. For device classes Q and V, die sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

40.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and as defined in the manufacturer's QM plan. As a minimum it shall consist of:

a) Wafer lot acceptance for Class V product using the criteria within MIL-STD-883 test method 5007.

b) 100% wafer probe (see paragraph 30.4)

c) 100% internal visual inspection to the applicable class Q or V criteria defined within MIL-STD-883 test method 2010 or the alternate procedures allowed within MIL-STD-883 test method 5004.

40.3 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed including groups A, B, C, D and E inspections and as specified herein except where MIL-PRF-38535 permits alternate in-line control testing.

40.3.1 Programmability. See 4.4.1.e for packaged die.

40.3.2 Group E inspection. Group E inspection is required only for parts intended to be identified as radiation assured (see 30.5 herein). RHA levels for device classes Q and V shall be as specified in MIL-PRF-38535.

50. DIE CARRIER

50.1 Die carrier requirements. The requirements for the die carrier shall be accordance with the manufacturer's QM plan or as specified in the purchase order by the acquiring activity. The die carrier shall provide adequate physical, mechanical and electrostatic protection.

60. NOTES

60.1 Intended use. Microcircuit die conforming to this drawing are intended for use in microcircuits built in accordance with MIL-PRF-38535 or MIL-PRF-38534 for government microcircuit application (original equipment), design applications and logistics purposes.

60.2 Comments. Comments on this appendix should be directed to DSCC-VA, Columbus, Ohio, 43216-5000 or telephone (614)-692-0674.

60.3 Abbreviations, symbols and definitions. The abbreviations, symbols, and definitions used herein are defined within MIL-PRF-38535 and MIL-HDBK-1331.

60.4 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed within QML-38535 have submitted a certificate of compliance (see 30.6 herein) to DSCC-VA and have agreed to this drawing.

I/O	NAME	CENTER-X	CENTER-Y
1	GNDQ	-5288.85	3617.10
2	VCC	-5288.85	3467.16
2A	VCCI	-5288.85	3334.32
3	MODE	-5288.85	3214.98
4	GND	-5288.85	3098.16
5	I/O	-5288.85	2997.99
6	I/O	-5288.85	2897.73
7	I/O	-5288.85	2797.47
8	I/O	-5288.85	2697.30
9	I/O	-5288.85	2597.04
10	I/O	-5288.85	2496.78
11	I/O	-5288.85	2396.61
12	GNDI	-5288.85	2296.35
13	I/O	-5288.85	2196.09
14	I/O	-5288.85	2095.83
15	VCCI	-5288.85	1995.66
16	I/O	-5288.85	1895.40
17	I/O	-5288.85	1795.14
18	I/O	-5288.85	1694.97
19	I/O	-5288.85	1594.71
20	I/O	-5288.85	1494.45
21	I/O	-5288.85	1394.28
21A	GNDI	-5288.85	1294.02
22	I/O	-5288.85	1193.76
23	VCC	-5288.85	1093.50
23A	VCCI	-5288.85	993.33
24	I/O	-5288.85	893.07
25	I/O	-5288.85	792.81
26	I/O	-5288.85	692.64
27	I/O	-5288.85	592.38
28	GND	-5288.85	492.12
29	I/O	-5288.85	391.95
30	I/O	-5288.85	291.69
31	I/O	-5288.85	191.43
32	I/O	-5288.85	91.17
33	GNDI	-5288.85	-9.00
34	VCCI	-5288.85	-109.26
35	VSV	-5288.85	-209.52
36	I/O	-5288.85	-309.69
37	I/O	-5288.85	-409.95
38	VCC	-5288.85	-510.21
38A	VCCI	-5288.85	-610.38
39	I/O	-5288.85	-710.64
40	I/O	-5288.85	-810.90
41	I/O	-5288.85	-911.16
42	I/O	-5288.85	-1011.33
42A	GNDI	-5288.85	-1111.59
43	I/O	-5288.85	-1211.85
44	I/O	-5288.85	-1312.02
45	I/O	-5288.85	-1412.28
46	I/O	-5288.85	-1512.54
47	I/O	-5288.85	-1612.71
48	I/O	-5288.85	-1712.97
48A	GNDI	-5288.85	-1813.23
49	I/O	-5288.85	-1913.49
50	I/O	-5288.85	-2013.66
51	I/O	-5288.85	-2113.92
52	VCCI	-5288.85	-2214.18
53	I/O	-5288.85	-2314.35
54	I/O	-5288.85	-2414.61
55	GNDI	-5288.85	-2514.87
56	I/O	-5288.85	-2615.04
57	I/O	-5288.85	-2715.30
58	I/O	-5288.85	-2815.56
59	I/O	-5288.85	-2915.82
60	I/O	-5288.85	-3015.99
61	I/O	-5288.85	-3116.34
62	I/O	-5288.85	-3225.78
63	GND	-5288.85	-3345.12
64	VCC	-5288.85	-3477.96
64A	VCCI	-5288.85	-3627.90
65	GNDQ	-4927.14	-3986.01
66	BININ	-4777.20	-3986.01
67	BINOUT	-4644.36	-3986.01
68	I/O	-4525.02	-3986.01
69	I/O	-4415.58	-3986.01
70	I/O	-4264.20	-3986.01
70A	GNDI	-4112.73	-3986.01
71	I/O	-3961.26	-3986.01
72	I/O	-3809.79	-3986.01
73	VCCI	-3658.32	-3986.01
74	I/O	-3506.85	-3986.01
75	I/O	-3355.38	-3986.01
76	I/O	-3203.91	-3986.01
77	I/O	-3052.44	-3986.01
78	GNDI	-2900.97	-3986.01
79	I/O	-2749.50	-3986.01
80	QCLKA	-2598.03	-3986.01
81	I/O	-2446.56	-3986.01
82	I/O	-2295.09	-3986.01
83	I/O	-2143.71	-3986.01
84	I/O	-1992.24	-3986.01

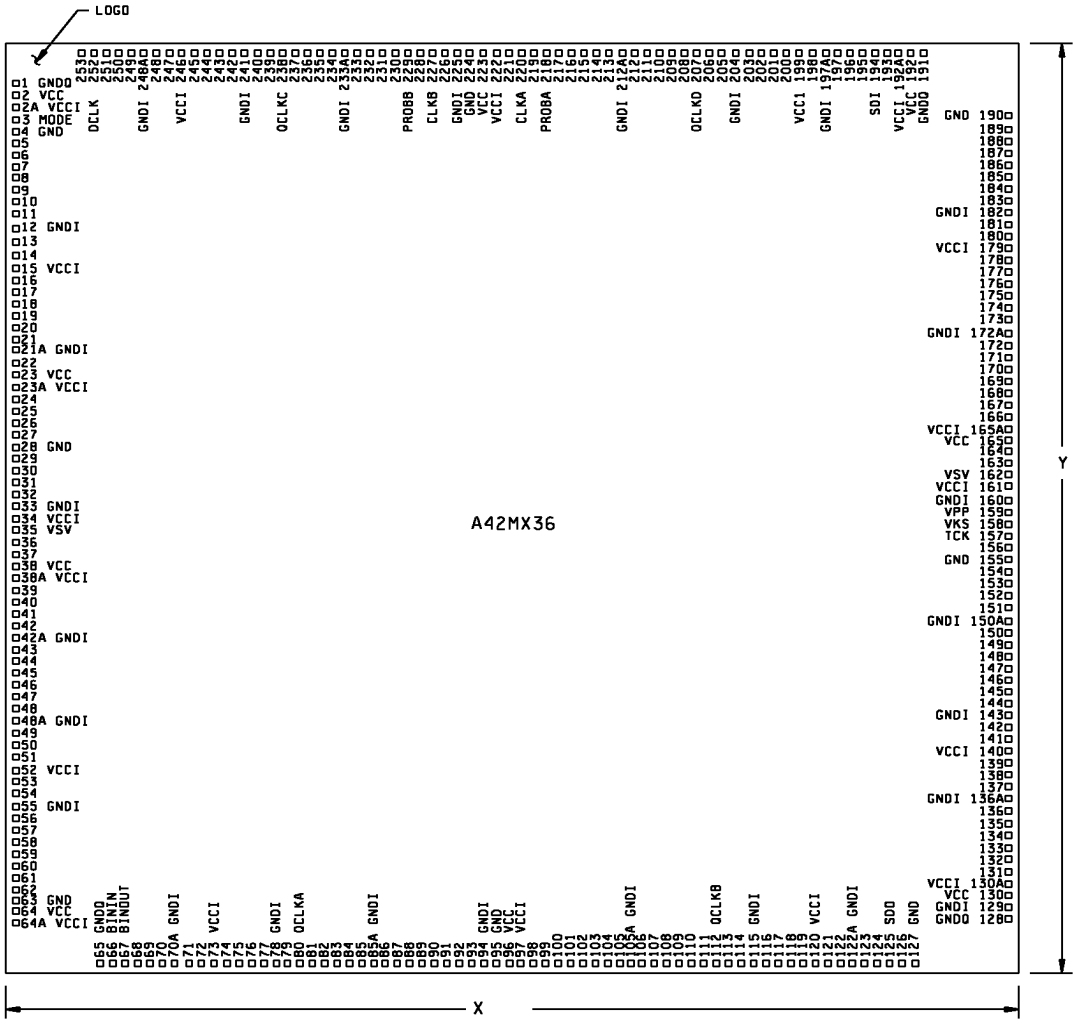
Figure A-1. Bond Pad Locations and Functions for Device 01

I/O	NAME	CENTER-X	CENTER-Y
85	I/O	-1840.77	-3986.01
85A	GNDI	-1689.30	-3986.01
86	I/O	-1537.83	-3986.01
87	I/O	-1386.36	-3986.01
88	I/O	-1234.89	-3986.01
89	I/O	-1083.42	-3986.01
90	I/O	-931.95	-3986.01
91	I/O	-780.48	-3986.01
92	I/O	-629.01	-3986.01
93	I/O	-477.54	-3986.01
94	GNDI	-326.07	-3986.01
95	GND	-174.60	-3986.01
96	VCC	-23.22	-3986.01
97	VCCI	128.25	-3986.01
98	I/O	279.72	-3986.01
99	I/O	431.19	-3986.01
100	I/O	582.66	-3986.01
101	I/O	734.13	-3986.01
102	I/O	885.60	-3986.01
103	I/O	1037.07	-3986.01
104	I/O	1188.54	-3986.01
105	I/O	1340.01	-3986.01
105A	GNDI	1491.48	-3986.01
106	I/O	1642.95	-3986.01
107	I/O	1794.42	-3986.01
108	I/O	1945.89	-3986.01
109	I/O	2097.27	-3986.01
110	I/O	2248.74	-3986.01
111	I/O	2400.21	-3986.01
112	QCLKB	2551.68	-3986.01
113	I/O	2703.15	-3986.01
114	I/O	2854.62	-3986.01
115	GNDI	3006.09	-3986.01
116	I/O	3157.56	-3986.01
117	I/O	3309.03	-3986.01
118	I/O	3460.50	-3986.01
119	I/O	3611.97	-3986.01
120	VCCI	3763.44	-3986.01
121	I/O	3914.91	-3986.01
122	I/O	4066.38	-3986.01
122A	GNDI	4217.85	-3986.01
123	I/O	4369.32	-3986.01
124	I/O	4478.76	-3986.01
125	SDO	4640.85	-3986.01
126	I/O	4773.69	-3986.01
127	GND	4923.63	-3986.01
128	GNDQ	5288.94	-3627.90
129	GNDI	5288.94	-3477.96
130	VCC	5288.94	-3345.12
130A	VCCI	5288.94	-3225.78
131	I/O	5288.94	-3116.34
132	I/O	5288.94	-3010.95
133	I/O	5288.94	-2905.47
134	I/O	5288.94	-2799.99
135	I/O	5288.94	-2694.60
136	I/O	5288.94	-2589.12
136A	GNDI	5288.94	-2483.64
137	I/O	5288.94	-2378.16
138	I/O	5288.94	-2272.77
139	I/O	5288.94	-2167.29
140	VCCI	5288.94	-2061.81
141	I/O	5288.94	-1956.42
142	I/O	5288.94	-1850.94
143	GNDI	5288.94	-1745.46
144	I/O	5288.94	-1639.98
145	I/O	5288.94	-1534.59
146	I/O	5288.94	-1429.11
147	I/O	5288.94	-1323.63
148	I/O	5288.94	-1218.24
149	I/O	5288.94	-1112.76
150	I/O	5288.94	-1007.28
150A	GNDI	5288.94	-901.80
151	I/O	5288.94	-796.41
152	I/O	5288.94	-690.93
153	I/O	5288.94	-585.45
154	I/O	5288.94	-479.97
155	GND	5288.94	-374.58
156	I/O	5288.94	-269.10
157	TCK	5288.94	-163.62
158	VKS	5288.94	-58.23
159	VPP	5288.94	47.25
160	GNDI	5288.94	152.73
161	VCCI	5288.94	258.21
162	VSV	5288.94	363.60
163	I/O	5288.94	469.08
164	I/O	5288.94	574.56
165	VCC	5288.94	679.95
165A	VCCI	5288.94	785.43
166	I/O	5288.94	890.91
167	I/O	5288.94	996.39
168	I/O	5288.94	1101.78
169	I/O	5288.94	1207.26

Figure A-1. Bond Pad Locations and Functions for Device 01 - Continued.

I/O	NAME	CENTER-X	CENTER-Y
170	I/O	5288.94	1312.74
171	I/O	5288.94	1418.13
172	I/O	5288.94	1523.61
172A	GNDI	5288.94	1629.09
173	I/O	5288.94	1734.57
174	I/O	5288.94	1839.96
175	I/O	5288.94	1945.44
176	I/O	5288.94	2050.92
177	I/O	5288.94	2156.40
178	I/O	5288.94	2261.79
179	VCCI	5288.94	2367.27
180	I/O	5288.94	2472.75
181	I/O	5288.94	2578.14
182	GNDI	5288.94	2683.62
183	I/O	5288.94	2789.10
184	I/O	5288.94	2894.58
185	I/O	5288.94	2999.97
186	I/O	5288.94	3105.54
187	I/O	5288.94	3214.98
188	I/O	5288.94	3334.32
189	I/O	5288.94	3467.16
190	GND	5288.94	3617.10
191	GNDQ	4923.63	3986.01
192	VCC	4773.69	3986.01
192A	VCCI	4640.85	3986.01
193	I/O	4521.51	3986.01
194	SDI	4412.07	3986.01
195	I/O	4262.49	3986.01
196	I/O	4112.91	3986.01
197	I/O	3963.24	3986.01
197A	GNDI	3813.66	3986.01
198	I/O	3663.99	3986.01
199	VCCI	3514.41	3986.01
200	I/O	3364.74	3986.01
201	I/O	3215.16	3986.01
202	I/O	3065.49	3986.01
203	I/O	2915.91	3986.01
204	GNDI	2766.33	3986.01
205	I/O	2616.66	3986.01
206	I/O	2467.08	3986.01
207	QCLKD	2317.41	3986.01
208	I/O	2167.83	3986.01
209	I/O	2018.16	3986.01
210	I/O	1868.58	3986.01
211	I/O	1718.91	3986.01
212	I/O	1569.33	3986.01
212A	GNDI	1419.66	3986.01
213	I/O	1270.08	3986.01
214	I/O	1120.50	3986.01
215	I/O	970.83	3986.01
216	I/O	821.25	3986.01
217	I/O	671.58	3986.01
218	PROBA	522.00	3986.01
219	I/O	372.33	3986.01
220	CLKA	222.75	3986.01
221	I/O	73.08	3986.01
222	VCCI	-76.50	3986.01
223	VCC	-226.08	3986.01
224	GND	-375.75	3986.01
225	GNDI	-525.33	3986.01
226	I/O	-675.00	3986.01
227	CLKB	-824.58	3986.01
228	I/O	-974.25	3986.01
229	PROBB	-1123.83	3986.01
230	I/O	-1273.50	3986.01
231	I/O	-1423.08	3986.01
232	I/O	-1572.75	3986.01
233	I/O	-1722.33	3986.01
233A	GNDI	-1871.91	3986.01
234	I/O	-2021.58	3986.01
235	I/O	-2171.16	3986.01
236	I/O	-2320.83	3986.01
237	I/O	-2470.41	3986.01
238	QCLKC	-2620.08	3986.01
239	I/O	-2769.66	3986.01
240	I/O	-2919.33	3986.01
241	GNDI	-3068.91	3986.01
242	I/O	-3218.49	3986.01
243	I/O	-3368.16	3986.01
244	I/O	-3517.74	3986.01
245	I/O	-3667.41	3986.01
246	VCCI	-3816.99	3986.01
247	I/O	-3966.66	3986.01
248	I/O	-4116.24	3986.01
248A	GNDI	-4265.91	3986.01
249	I/O	-4415.58	3986.01
250	I/O	-4525.02	3986.01
251	I/O	-4644.36	3986.01
252	DCLK	-4777.20	3986.01
253	I/O	-4927.14	3986.01

Figure A-1. Bond Pad Locations and Functions for Device 01 - Continued.



Note:
1. All dimensions are in micrometer
2. The die center is the coordinate origin (0,0).
3. VSV, VKS and Vpp pins are used for programming. For normal operation, these pins should be connected to Vcc or GND.
4. Wire bond pad opening (glass free) is 68 x 68 micron.

Figure A-1. Bond Pad Locations and Functions for Device 01 - Continued.

STANDARD MICROCIRCUIT DRAWING SOURCE APPROVAL BULLETIN

DATE: **99-07-13**

Approved sources of supply for SMD 5962-99585 are listed below for immediate acquisition only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535.

Standard microcircuit 1/ drawing PIN	Vendor CAGE number	Vendor similar 2/ PIN
5962-9958501QXC	0J4Z0	A42MX36-CQ256B
5962-9958501QYC	0J4Z0	A42MX36-CQ208B
5962-9958502QXC	0J4Z0	A42MX36-1CQ256B
5962-9958502QYC	0J4Z0	A42MX36-1CQ208B
5962-9958501Q9A	0J4Z0	A42MX36-DIE

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed, contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
0J4Z0	Actel Corporation 955 East Arques Ave. Sunnyvale, CA 94086