

REVISIONS																			
LTR	DESCRIPTION														DATE (YR-MO-DA)				APPROVED
A	Add case outline U. Add note 2/ to sheet 2. Add note 5/ to table IA. Add note 6/ to table WHWL. Make corrections to notes on sheets 11 and 13. Add note 3 to figure 3. Add note 2 to figure 5. Read Cycle. Add note 6 to figure 5. Write Cycle. Make correction to note 5 of figure 6. Add vendor CAGE 34168 as source of supply for case outline U. Editorial corrections throughout.														97-06-12				Raymond Monnin

REV																			
SHEET																			
REV	A	A	A	A	A	A	A	A	A	A	A	A	A	A					
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28					

REV STATUS OF SHEETS				REV		A	A	A	A				A		A	A	A	A	A
				SHEET		1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A STANDARD MICROCIRCUIT DRAWING THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE AMSC N/A	PREPARED BY Jeff Bowling CHECKED BY Jeff Bowling APPROVED BY Ray Monnin DRAWING APPROVAL DATE 96-11-26 REVISION LEVEL A	DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216 MICROCIRCUIT, MEMORY, DIGITAL, RADIATION- HARDENED, CMOS/SOI, 32K X 8 STATIC RAM, MONOLITHIC SILICON <table border="1" style="width: 100%; border-collapse: collapse; margin-top: 10px;"> <tr> <td style="width: 20%;">SIZE A</td> <td style="width: 20%;">CAGE CODE 67268</td> <td style="width: 60%; text-align: center;">5962-95845</td> </tr> </table> SHEET 1 OF 28	SIZE A	CAGE CODE 67268	5962-95845
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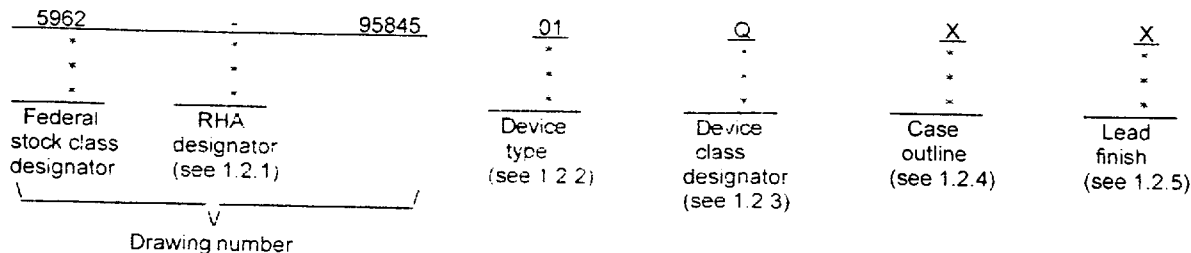
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1 SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number 1/	Circuit function	Input/output levels	Chip enable 2/	Access time
01		32K X 8 CMOS/SOI SRAM	CMOS	Dual	25 ns
02		32K X 8 CMOS/SOI SRAM	TTL	Dual	25 ns
03		32K X 8 CMOS/SOI SRAM	CMOS	Dual	25 ns
04		32K X 8 CMOS/SOI SRAM	TTL	Dual	25 ns
05		32K X 8 CMOS/SOI SRAM	CMOS	Dual	20 ns
06		32K X 8 CMOS/SOI SRAM	TTL	Dual	20 ns

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	GDIP1-T28 or CDIP2-T28	28	Dual-in-line
Y	See figure 1	28	Flat pack
Z	See figure 1	36	Flat pack
U	See figure 1	36	Flat pack

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1/ Generic numbers are listed on the Standard Microcircuit Drawing Source Approval Bulletin at the end of this document and will also be listed in QML-38535.

2/ Any device type ordered in case outlines X or Y is single chip enable.

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1.3 Absolute maximum ratings. 3/ 4/

Supply voltage range (V_{CC})	-0.5 V dc to +6.5 V dc
DC input voltage range (V_{IN})	-0.5 V dc to $V_{CC} + 0.5$ V dc
DC output voltage range (V_{OUT})	-0.5 V dc to $V_{CC} + 0.5$ V dc
Storage temperature range	-65°C to +150°C
Lead temperature (soldering, 5 seconds)	+270°C
Thermal resistance, junction-to-case (Θ_{JC}):	
Case X	See MIL-STD-1835
Cases Y, Z, and U	2.0° C/watt
Output voltage applied to high Z state	-0.5 V dc to $V_{CC} + 0.5$ V dc
Maximum power dissipation (P_D)	2 watts
Maximum junction temperature (T_J)	+175°C

1.4 Recommended operating conditions.

Supply voltage range (V_{CC})	4.5 V dc (min) to 5.5 V dc (max)
Supply voltage (V_{SS})	0.0 V dc
High level input voltage range (V_{IH}):	
Device type 01, 03, 05 (CMOS levels)	0.7 x V_{CC} to $V_{CC} + 0.3$ V dc
Device type 02, 04, 06 (TTL levels)	2.2 V dc to $V_{CC} + 0.3$ V dc
Low level input voltage range (V_{IL}):	
Device type 01, 03, 05 (CMOS levels)	-0.3 V dc to 0.3 x V_{CC}
Device type 02, 04, 06 (TTL levels)	-0.3 V dc to 0.8 V dc
Case operating temperature range (T_C)	-55°C to +125°C

1.5 Digital logic testing for device classes Q and V.

Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012)	100 percent
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2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

MILITARY

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Microcircuit Case Outlines.

3/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

4/ All voltages referenced to V_{SS} (V_{SS} = ground), unless otherwise specified.

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HANDBOOKS

MILITARY

- MIL-HDBK-103 - List of Standard Microcircuit Drawings (SMD's).
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issue of the documents which are DoD adopted are those listed in the issue of the DODISS cited in the solicitation. Unless otherwise specified, the issues of documents not listed in the DODISS are the issues of the documents cited in the solicitation.

AMERICAN SOCIETY FOR TESTING AND MATERIALS (ASTM)

- ASTM Standard F1192-88 - Standard Guide for the Measurement of Single Event Phenomena from Heavy Ion Irradiation of Semiconductor Devices.

(Applications for copies of ASTM publications should be addressed to the American Society for Testing and Materials, 1916 Race Street, Philadelphia, PA 19103).

(Non-Government standards and other publications are normally available from the organizations that prepare or distribute the documents. These documents also may be available in or through libraries or other informational services.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing shall take precedence.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Truth table(s). The truth table(s) shall be as specified on figure 3.

3.2.4 Radiation exposure circuit. The radiation exposure circuit shall be as specified on figure 6.

3.2.5 Functional tests. Various functional tests used to test this device are contained in the appendix. If the test patterns cannot be implemented due to test equipment limitations, alternate test patterns to accomplish the same results shall be allowed. For device class M, alternate test patterns shall be maintained under document revision level control by the manufacturer and shall be made available to the preparing or acquiring activity upon request. For device classes Q and V alternate test patterns shall be under the control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the preparing or acquiring activity upon request.

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3.2.6 Die overcoat. Polyimide and silicone coatings are allowable as an overcoat on the die for alpha particle protection only. Each coated microcircuit inspection lot (see inspection lot as defined in MIL-PRF-38535) shall be subjected to and pass the internal moisture content test at 5000 ppm (see method 1018 of MIL-STD-883). The frequency of the internal water vapor testing shall not be decreased unless approved by the preparing activity for class M. The TRB will ascertain the requirements as provided by MIL-PRF-38535 for classes Q and V. Samples may be pulled any time after seal.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table IA and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table IA.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-973.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 41 (see MIL-PRF-38535, appendix A).

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

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TABLE IA. Electrical performance characteristics

Test	Symbol	Conditions -55°C ≤ T _C ≤ +125°C 4.5 V ≤ V _{CC} ≤ 5.5 V unless otherwise specified	Group A subgroups	Device Type	Limits		Unit
					Min	Max	
High level output voltage	V _{OH}	V _{CC} = 4.5 V, I _{OH} = -5 mA, V _{IL} = 1.35 V, V _{IH} = 3.15 V	1, 2, 3	01,03, 05	4.2		V
		V _{CC} = 4.5 V, I _{OH} = -4 mA, V _{IL} = 0.8 V, V _{IH} = 2.2 V		02,04, 06	4.2		
		M,D,L,R,F,G,H	1 1/		2/		
Low level output voltage	V _{OL}	V _{CC} = 4.5 V, I _{OL} = 10 mA, V _{IL} = 1.35 V, V _{IH} = 3.15 V	1, 2, 3	01,03, 05		0.4	V
		V _{CC} = 4.5 V, I _{OL} = 8 mA, V _{IL} = 0.8 V, V _{IH} = 2.2 V		02,04, 06		0.4	
		M,D,L,R,F,G,H	1 1/			2/	
Input leakage current	I _{ILK}	V _{CC} = 5.5 V, V _{IN} = 0.0 V to 5.5 V, all other pins at 0.0 V	1, 2, 3	All	-5	5	μA
		M,D,L,R,F,G,H	1 1/		2/	2/	
Output leakage current	I _{OLK}	V _{CC} = 5.5 V, V _{OUT} = 0.0 V to 5.5 V, all other pins at 0.0 V	1, 2, 3	All	-10	10	μA
		M,D,L,R,F,G,H	1 1/		2/	2/	
Data retention voltage	V _{DR}	V _{CC} = 2.5 V	1, 2, 3	All	2.5		μA
		M,D,L,R,F,G,H	1 1/		2/		
Operating supply current	I _{CC1}	V _{CC} = 5.5 V, f = f _{MAX} 4/, S = GND, E = V _{CC} 5/, no output loading	1, 2, 3	All		160	mA
		M,D,L,R,F,G,H	1 1/			2/	
Supply current (deselected)	I _{CC2}	V _{CC} = 5.5 V, f = f _{MAX} 4/, S = V _{CC} , E = GND 5/	1, 2, 3	All		1.5	mA
		M,D,L,R,F,G,H	1 1/			2/	
Supply current (standby)	I _{CC3}	V _{CC} = 5.5 V, f = 0.0 Mhz, S = V _{CC} , E = GND	1, 2, 3	All		1.5	mA
		M,D,L,R,F,G,H	1 1/			2/	
Data retention current	I _{CC4}	V _{CC} = 2.5 V	1, 2, 3	01,02, 05,06		500	μA
		V _{CC} = 3.0 V		03,04		330	
		M,D,L,R,F,G,H	1 1/			2/	

See footnotes at end of table.

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TABLE 1A. Electrical performance characteristics - continued.

Test	Symbol	Conditions 3/ -55°C ≤ T _C ≤ +125°C 4.5 V ≤ V _{CC} ≤ 5.5 V unless otherwise specified	Group A subgroups	Device Type	Limits		Unit
					Min	Max	
Input capacitance 6/	C _{IN}	V _I = 5.0 V or 0.0 V, T _A = +25°C, see 4.4.1d, f = 1.0 Mhz	4	All		7	pF
Output capacitance 6/	C _{OUT}	V _O = 5.0 V or 0.0 V, T _A = +25°C, see 4.4.1d, f = 1.0 Mhz	4	All		9	pF
Functional tests		See 4.4.1c	7,8A,8B	All			
		M,D,L,R,F,G,H	7 1/		2/		
Read cycle time	t _{AVAV}		9,10,11	All	25		ns
		M,D,L,R,F,G,H	9 1/		2/		
Address access time	t _{AVQV}		9,10,11	All		25	ns
		M,D,L,R,F,G,H	9 1/			2/	
Chip enable/select access time 5/	t _{EHQV} t _{SLQV}		9,10,11	All	25		ns
		M,D,L,R,F,G,H	9 1/		2/		
Output hold after address change	t _{AVQX}		9,10,11	All	3		ns
		M,D,L,R,F,G,H	9 1/		2/		
Output enable access time	t _{GLQV}		9,10,11	All		9	ns
		M,D,L,R,F,G,H	9 1/			2/	
Chip enable/select to output active 5/ 7/	t _{EHQX} t _{SLQX}		9,10,11	All	5		ns
		M,D,L,R,F,G,H	9 1/		2/		
Output enable to output active	t _{GLQX}		9,10,11	All	0		ns
		M,D,L,R,F,G,H	9 1/		2/		
Chip disable/deselect to output disable 5/ 8/	t _{ELQZ} t _{SHQZ}		9,10,11	All		10	ns
		M,D,L,R,F,G,H	9 1/			2/	
Output enable to output disable 8/	t _{GHQZ}		9,10,11	All		9	ns
		M,D,L,R,F,G,H	9 1/			2/	
Write enable to output disable 8/	t _{WLQZ}		9,10,11	All		9	ns
		M,D,L,R,F,G,H	9 1/			2/	

See footnotes at end of table.

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TABLE 1A. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 3/ -55°C ≤ T _C ≤ +125°C 4.5 V ≤ V _{CC} ≤ 5.5 V unless otherwise specified	Group A subgroups	Device Type	Limits		Unit
					Min	Max	
Data setup to end of write	t _{DVWH}		9,10,11	All	15		ns
		M,D,L,R,F,G,H	9 1/		2/		
Data hold after end of write	t _{WHDX}		9,10,11	All	0		ns
		M,D,L,R,F,G,H	9 1/		2/		
Output active after end of write	t _{WHQX}		9,10,11	All	5		ns
		M,D,L,R,F,G,H	9 1/		2/		
Write cycle time 9/ 10/	t _{AVAV}		9,10,11	01-04	25		ns
				05,06	20		
		M,D,L,R,F,G,H	9 1/		2/		
Chip enable/select to end of write 5/	t _{EHWH} t _{SLWH}		9,10,11	All	20		ns
		M,D,L,R,F,G,H	7 1/		2/		
Address setup to end of write	t _{AVWH}		9,10,11	All	20		ns
		M,D,L,R,F,G,H	9 1/		2/		
Address setup to start of write	t _{AVWL}		9,10,11	All	0		ns
		M,D,L,R,F,G,H	9 1/		2/		
Write pulse width	t _{WLWH}		9,10,11	All	20		ns
		M,D,L,R,F,G,H	9 1/		2/		
Address hold after end of write	t _{WHAX}		9,10,11	All	0		ns
		M,D,L,R,F,G,H	9 1/		2/		
Write disable pulse width 6/	t _{WHWL}		9,10,11	All	5		ns
		M,D,L,R,F,G,H	9 1/		2/ 5/		

- 1/ When performing postirradiation electrical measurements for any RHA level T_A = +25°C. Limits shown are guaranteed at T_A = +25°C ±5°C. The M, D, L, R, F, G, and H in the test condition column are the postirradiation limits for the device types specified in the device types column.
- 2/ Preirradiation values for RHA marked devices shall also be the postirradiation values, unless otherwise specified.
- 3/ AC measurements assume transition times ≤ 1 ns/V. For output load circuit, see figure 4 and for timing waveforms, see figure 5.
- 4/ f_{MAX} = 1/t_{AVAV} (minimum read cycle time).
- 5/ Input E and timing parameters t_{EHQV}, t_{EHQX}, t_{ELQZ}, and t_{EHWH} do not apply to devices in case outline X or Y.
- 6/ Tested initially and after any design or process changes which may affect that parameter, and therefore shall be guaranteed to the limits specified in table 1A.
- 7/ Transition is measured ±500 mV from steady-state voltage.
- 8/ Transition is measured ±400 mV from steady-state voltage.
- 9/ Outputs disabled.
- 10/ t_{AVAV} = t_{WLWH} + t_{WHWL}.

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TABLE IB. SEP test limits. 1/ 2/

Device type	$T_A =$ Temperature $\pm 10^\circ\text{C}$	Memory pattern	$V_{CC} = 4.5\text{ V}$		Bias for latch-up test $V_{CC} = 5.5\text{ V}$ no latch-up LET = 3/
			Effective LET no upsets [MeV/(mg/cm ²)]	Maximum device cross section (cm ²) LET = 190	
All	+125°C	4/	≥ 75	≤ 0.056	≥ 120

1/ For SEP test conditions, see 4.4.4 herein.

2/ Technology characterization and model verification supplemented by in-line data may be used in lieu of end-of-line testing. Test plan must be approved by TRB and qualifying activity.

3/ Worst case temperature $T_A = +125^\circ\text{C}$.

4/ Testing shall be performed using checkerboard and checkerboard bar test patterns.

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Case Y

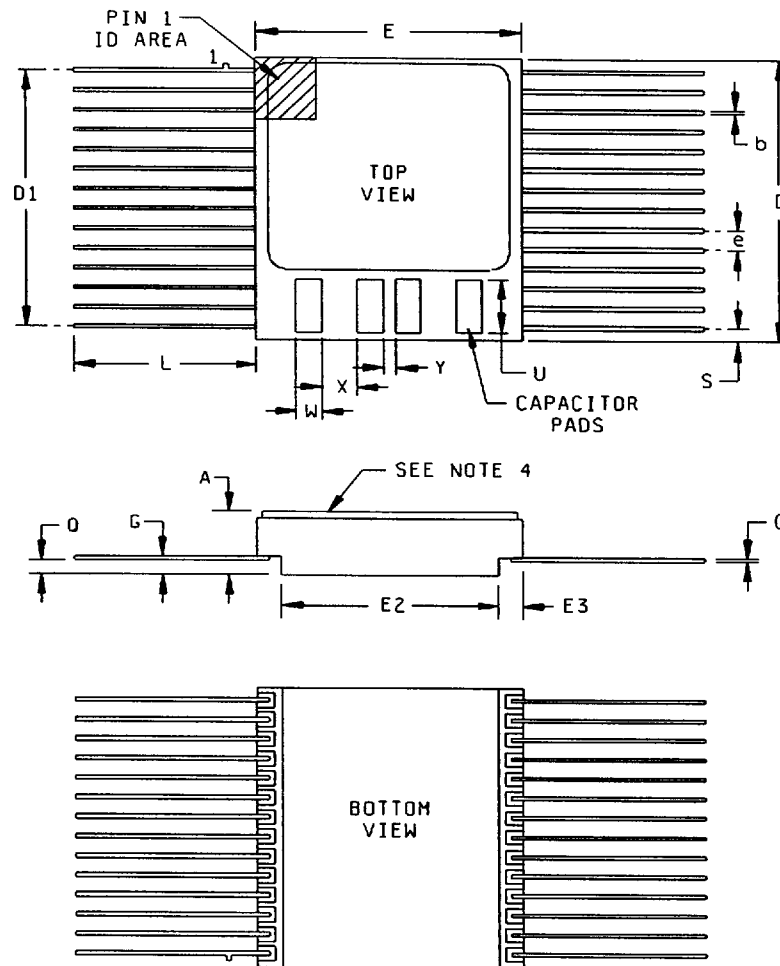


FIGURE 1. Case outlines - continued.

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Case Y - continued

Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	2.29	3.05	.090	.120
b	0.38	0.48	.015	.019
C	0.08	0.15	.003	.006
D	18.08	18.49	.712	.728
D1	16.38	16.64	.645	.655
E	12.52	12.88	.493	.507
E2	9.45	9.86	.372	.388
E3	1.52 REF		.060 BSC	
e	1.27 BSC		.050 BSC	

Symbol	Millimeters		Inches	
	Min	Max	Min	Max
G	0.79	0.99	.031	.039
L	7.49	—	.295	—
Q	0.66	1.14	.026	.045
S	0.89	1.40	.035	.055
U	3.30 REF		.130 REF	
W	1.27 REF		.050 REF	
X	1.91 REF		.075 REF	
Y	0.25 REF		.010 REF	

- NOTES: 1. Lid tied to V_{SS} .
 2. The indicated terminal pad is P1. Terminal pads are numbered clockwise (bottom view) through P4.

FIGURE 1. Case outlines - Continued.

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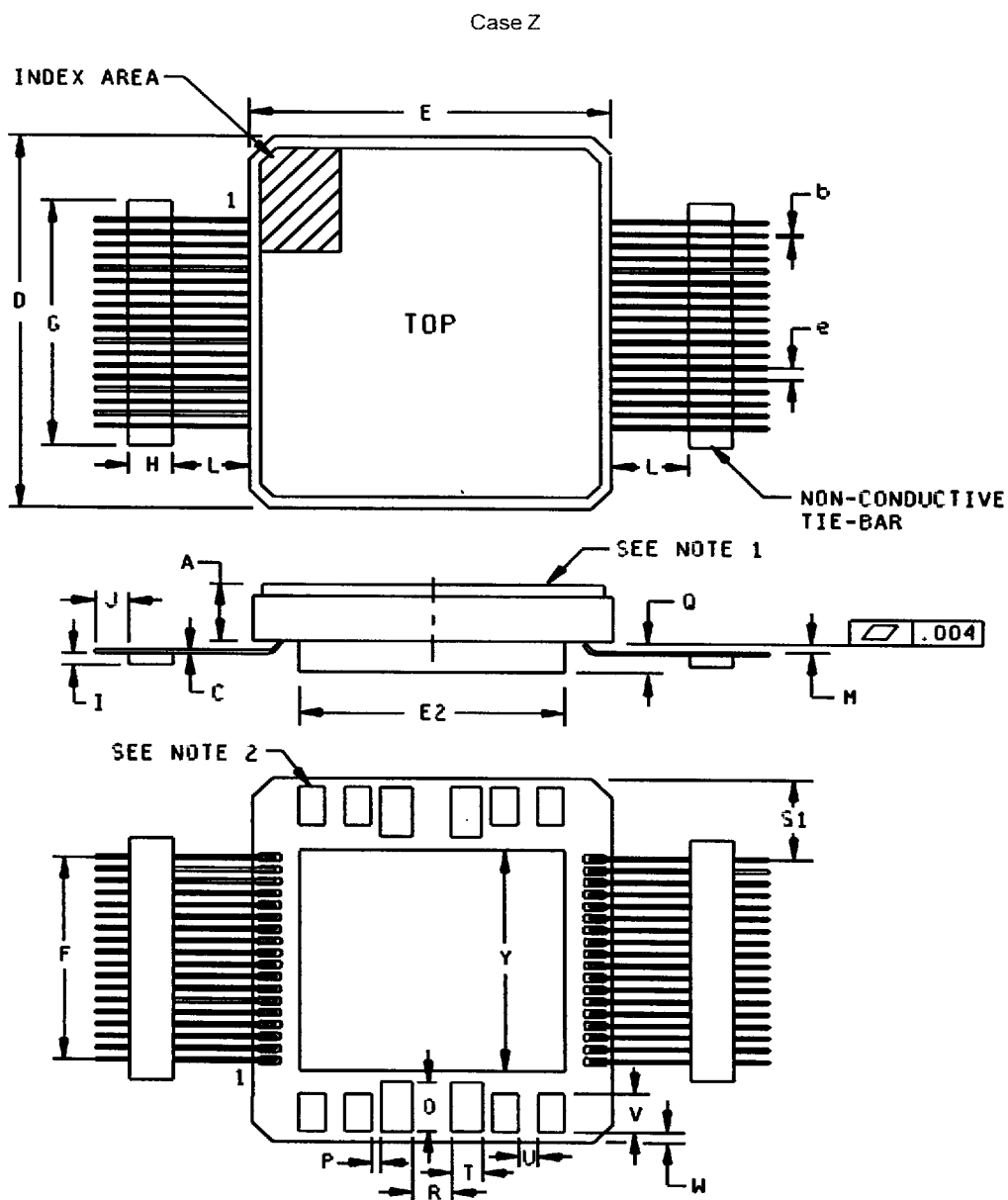


FIGURE 1. Case outlines.

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Case Z - continued

Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	2.16	2.67	.085	.105
b	0.15	0.25	.006	.010
C	0.127	0.191	.0050	.0075
D	16.26	16.76	.640	.660
E	15.85	16.18	.623	.637
E2	11.43 REF		.450 REF	
e	0.635 BSC		.025 BSC	
F	10.67	10.92	.420	.430
G	13.34 REF		.525 REF	
H	3.43 REF		.135 REF	
I	0.64	0.89	.025	.035
J	2.03 REF		.080 REF	

Symbol	Millimeters		Inches	
	Min	Max	Min	Max
L	6.86	7.62	.270	.300
M	0.13	0.28	.005	.011
O	2.29 REF		.090 REF	
P	0.38 REF		.38 REF	
Q	1.02	1.52	.040	.060
R	1.91 REF		.075 REF	
S1	2.62	3.12	.103	.123
T	1.27 REF		.050 REF	
U	0.76 REF		.030 REF	
V	2.03 REF		.080 REF	
W	0.13 REF		.005 REF	
Y	10.16 REF		.400 REF	

- NOTES: 1. Lid tied to V_{SS} .
 2. The indicated terminal pad is P1. Terminal pads are numbered clockwise (bottom view) through P12.

FIGURE 1. Case outlines - continued.

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Case U

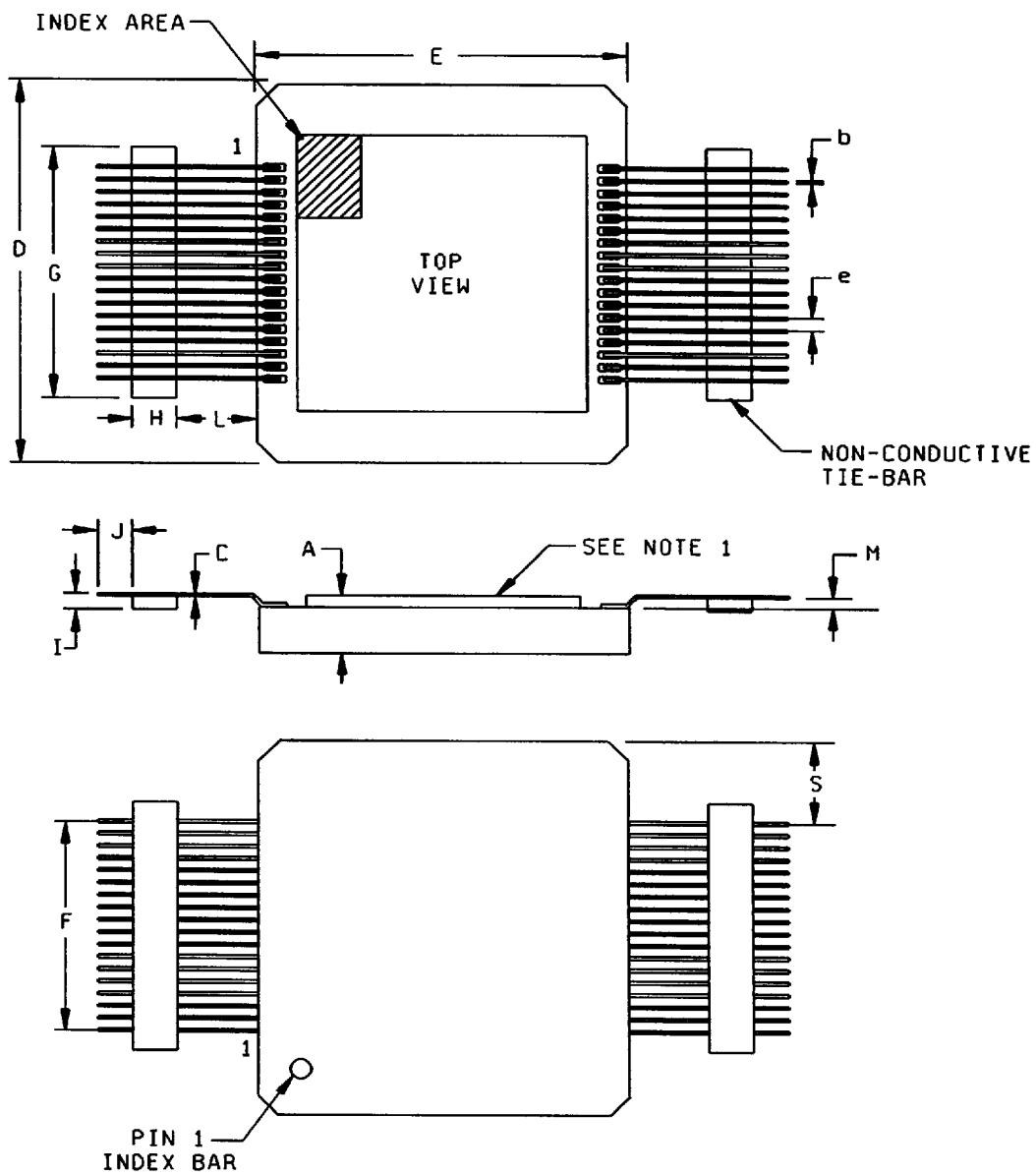


FIGURE 1. Case outlines - continued.

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MICROCIRCUIT DRAWING
DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 42316-5000

SIZE
A

5962-95845

REVISION LEVEL
A

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Case U - continued

Symbol	Millimeters		Inches	
	Min	Max	Min	Max
A	1.91	2.41	.075	.095
b	0.15	0.25	.006	.010
C	0.127	0.191	.0050	.0075
D	16.26	16.76	.640	.660
E	15.85	16.18	.623	.637
e See note 2	0.635 BSC		.025 BSC	
F See note 2	10.67	10.92	.420	.430

Symbol	Millimeters		Inches	
	Min	Max	Min	Max
G	13.34 REF		.525 REF	
H	3.43 REF		.135 REF	
I	0.64	0.89	.025	.035
J	2.03 REF		.080 REF	
L	6.86	7.37	.270	.290
M	0.15	0.30	.006	.012
S	2.62	3.12	.103	.123

- NOTES: 1. Lid tied to V_{SS} .
 2. Dimensions e and F are measured at tie bar.

FIGURE 1. Case outlines - continued.

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Device type	All			
Case outline	X	Y	Z	U
Terminal no.	Terminal symbol			
1	A ₁₄	A ₁₄	GND	GND
2	A ₁₂	A ₁₂	V _{CC}	V _{CC}
3	A ₇	A ₇	A ₁	A ₁
4	A ₆	A ₆	A ₀	A ₀
5	A ₅	A ₅	A ₁₀	A ₁₀
6	A ₄	A ₄	A ₉	A ₉
7	A ₃	A ₃	A ₇	A ₇
8	A ₂	A ₂	A ₈	A ₈
9	A ₁	A ₁	A ₁₁	A ₁₁
10	A ₀	A ₀	A ₁₂	A ₁₂
11	I/O ₁	I/O ₁	A ₁₃	A ₁₃
12	I/O ₂	I/O ₂	A ₁₄	A ₁₄
13	I/O ₃	I/O ₃	I/O ₁	I/O ₁
14	GND	GND	I/O ₂	I/O ₂
15	I/O ₄	I/O ₄	I/O ₃	I/O ₃
16	I/O ₅	I/O ₅	NC	NC
17	I/O ₆	I/O ₆	V _{CC}	V _{CC}
18	I/O ₇	I/O ₇	GND	GND
19	I/O ₈	I/O ₈	GND	GND
20	S	S	V _{CC}	V _{CC}
21	A ₁₀	A ₁₀	I/O ₄	I/O ₄
22	G	G	I/O ₅	I/O ₅
23	A ₁₁	A ₁₁	I/O ₆	I/O ₆
24	A ₉	A ₉	I/O ₇	I/O ₇
25	A ₈	A ₈	I/O ₈	I/O ₈
26	A ₁₃	A ₁₃	S	S
27	W	W	A ₂	A ₂
28	V _{CC}	V _{CC}	G	G
29	—	—	A ₆	A ₆
30	—	—	A ₅	A ₅
31	—	—	A ₄	A ₄
32	—	—	A ₃	A ₃
33	—	—	E	E
34	—	—	W	W
35	—	—	V _{CC}	V _{CC}
36	—	—	GND	GND
P1	—	V _{CC}	V _{CC}	—
P2	—	GND	GND	—
P3	—	V _{CC}	GND	—
P4	—	GND	V _{CC}	—
P5	—	—	V _{CC}	—
P6	—	—	GND	—
P7	—	—	GND	—
P8	—	—	V _{CC}	—
P9	—	—	V _{CC}	—
P10	—	—	GND	—
P11	—	—	GND	—
P12	—	—	V _{CC}	—

FIGURE 2. Terminal connections.

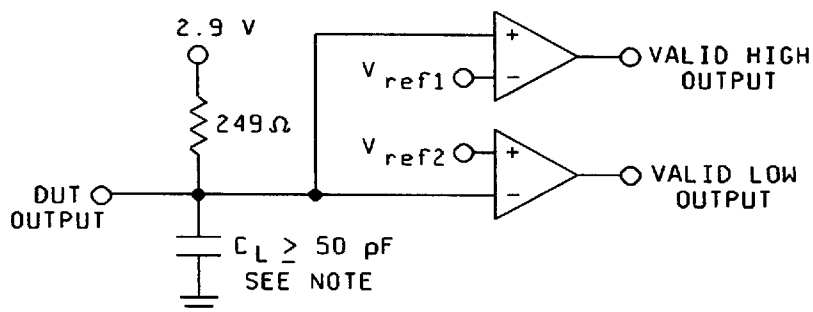
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Mode	Inputs (see notes 1 and 2)					Power
	E (see note 3)	$\overline{S}$	$\overline{W}$	$\overline{G}$	I/O	
Write	High	Low	Low	Don't care	Data in	Active
Read	High	Low	High	Low	Data out	Active
Standby	Don't care	High	Don't care	Don't care	High Z	Standby
Standby (see note 4)	Low	Don't care	Don't care	Don't care	High Z	Standby

NOTES:

1. V_{IN} for Don't Care inputs = V_{IL} OR V_{IH} .
2. When $\overline{G}$ = high, I/O is High-Z.
3. Input E does not apply to devices in case outline X or Y.
4. When in standby mode, $\overline{S} = V_{CC}$ and E = GND input levels to dissipate minimum standby power. All other input levels may float.

FIGURE 3. Truth table.



AC test conditions

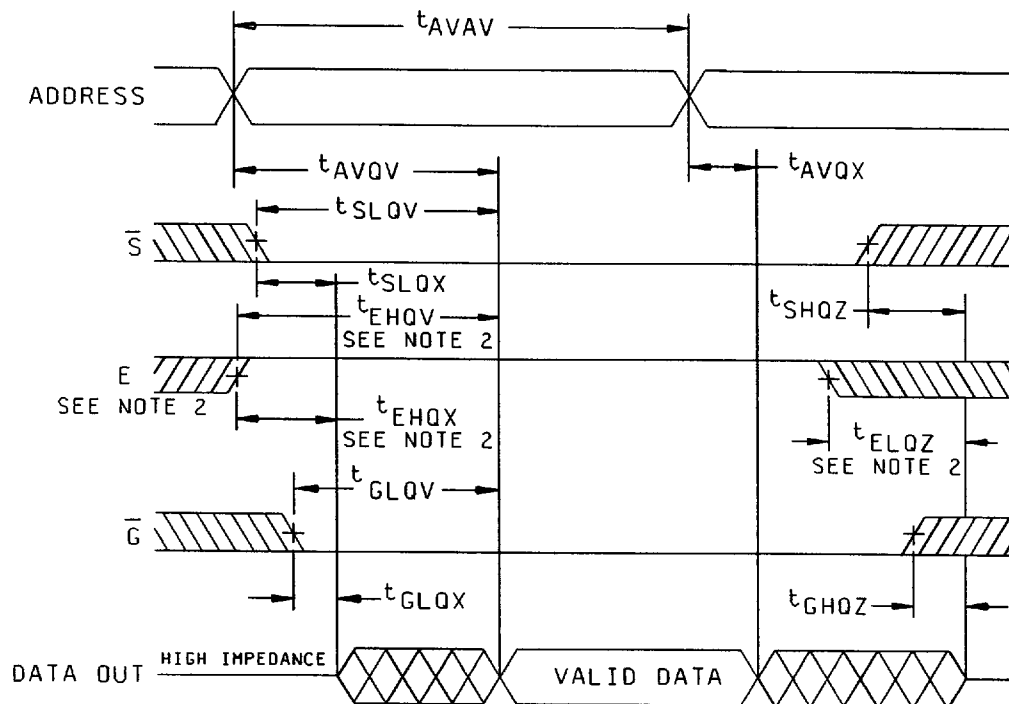
	Device types	
	01,03,05	02,04,06
Input pulse levels	0.5 V to $V_{CC} - 0.5$ V	0 V to 3 V
Input rise and fall times	< 1 ns/V	< 1 ns/V
Input timing reference	$V_{CC}/2$	1.5 V
Output timing reference	1.5 V	$V_{CC}/2$

NOTES: Capacitance includes scope and jig (minimum values).

FIGURE 4. Output load circuit (see note).

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Read cycle (see note 1)



NOTES:

1. $\bar{W}$ is high for read cycle.
2. Input E and timing parameters t_{EHQV} , t_{EHQX} , and t_{ELQZ} do not apply to devices in case outline X or Y.

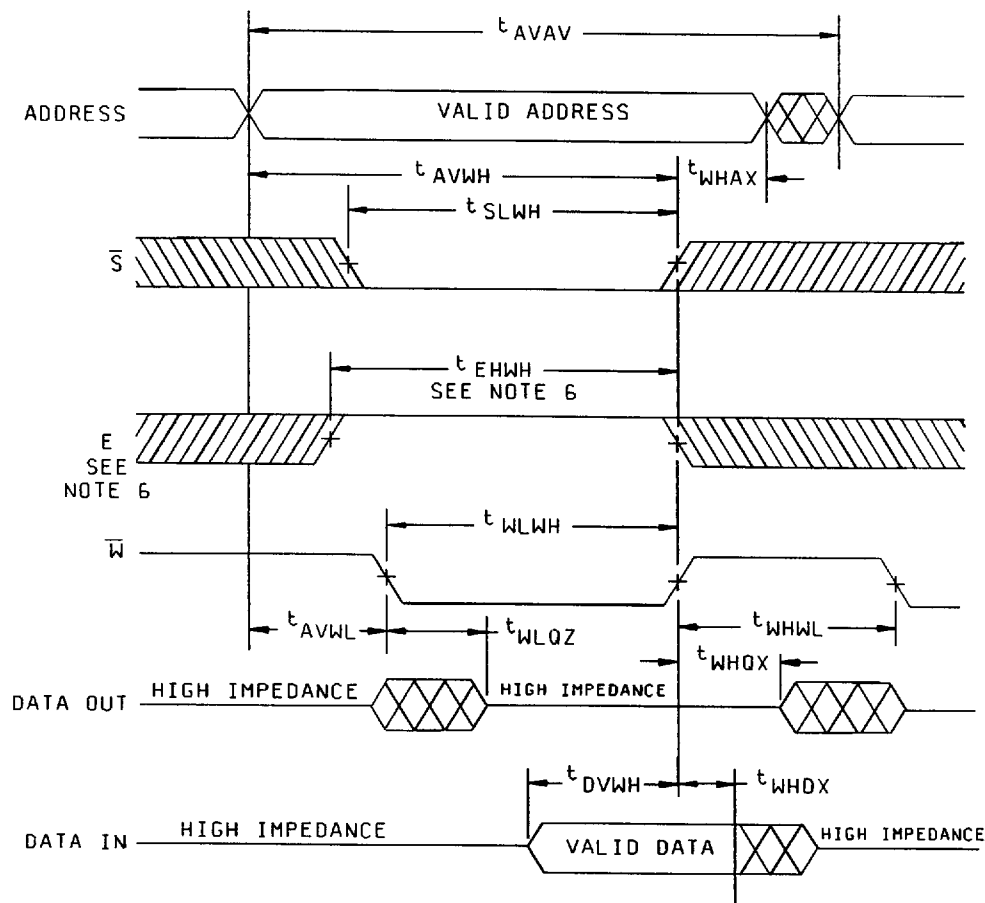
FIGURE 5. Timing waveforms

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APR 97

9004708 0029601 955

Write cycle (see notes 1, 2, 3, 4, and 5)



NOTES:

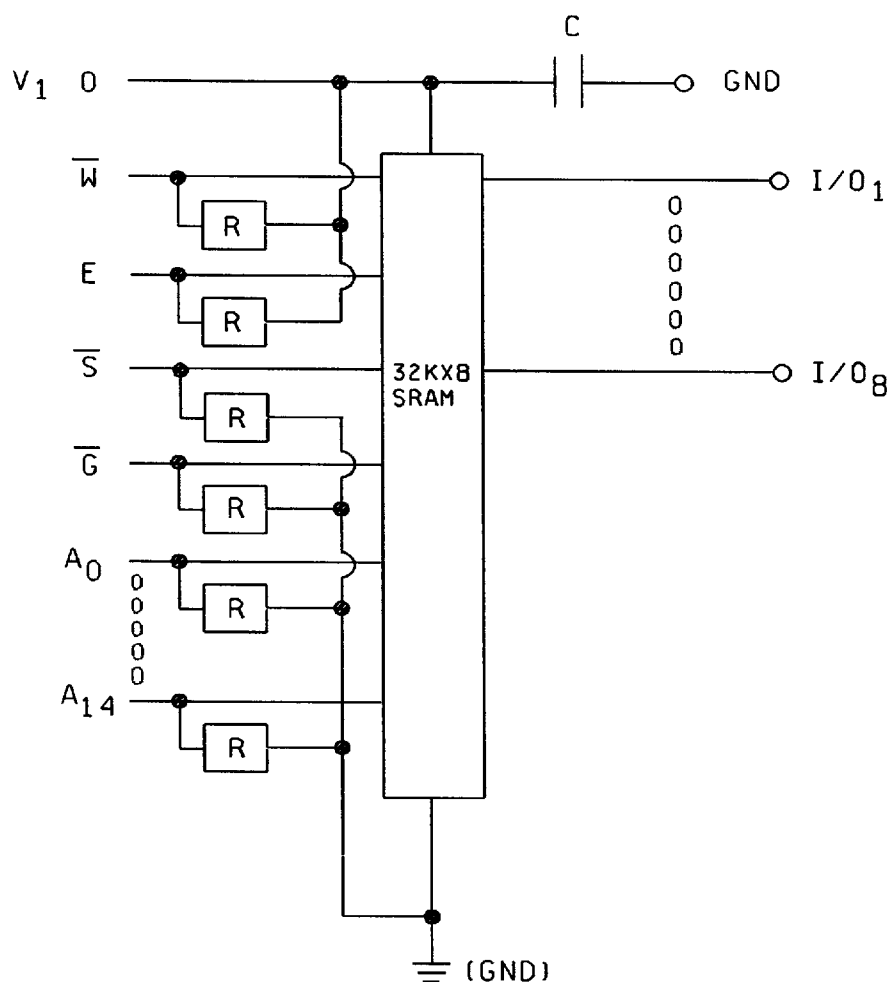
1. Write cycle data is latched by the first occurrence of $\bar{S}$ high, E low or $\bar{W}$ high.
2. $\bar{S}$ high, E low, or $\bar{W}$ high must occur while address transitions.
3. Write cycle time is guaranteed for toggling $\bar{S}$ and E or holding $\bar{S}$ or E, or both, in active state.
4. The worst case timing sequence of $t_{WLQZ} + t_{DVWH} + t_{WHWL} =$ the write cycle time (t_{AVAV}).
5. $\bar{G}$ high will eliminate the I/O output from becoming active (t_{WLQZ}).
6. Input E and timing parameter t_{EWHH} do not apply to devices in case outline X or Y.

FIGURE 5. Timing waveforms - continued.

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APR 97

9004708 0029602 891



NOTES:

1. Power pins connected to V_1 .
2. The absolute voltage ratings of 1.3 shall not be exceeded.
3. ESD precautions shall be followed.
4. The pattern in the memory array will be checkerboard for irradiation and accelerated aging tests.
5. Pin conditions (input E does not apply to devices in case outline X or Y):

$\bar{S} = \text{GND}$ $\bar{W} = V_{CC}$ $\bar{G} = \text{GND}$
 $E = V_{CC}$ $A_0 - A_{14} = \text{GND}$ $I/O_1 - I/O_8 = \text{FLOATING}$
 $V_1 = V_{CC}$ $R = 10 \text{ k}\Omega \pm 10\%$ $C = 0.1 \mu\text{F} \pm 10\%$
 $V_{CC} = 5.0 \text{ V}$

FIGURE 6. Radiation exposure circuit (see notes)

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TABLE IIA. Electrical test requirements 1/ 2/ 3/ 4/ 5/ 6/

Line no.	Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
		Device class M	Device class Q	Device class V
1	Interim electrical parameters (see 4.2)			1,7,9
2	Static burn-in I and II (method 1015)	Not required	Not required	Required
3	Same as line 1			1*,7* Δ
4	Dynamic burn-in (method 1015)	Required	Required	Required
5	Same as line 1			1*,7* Δ
6	Final electrical parameters	1*,2,3,7*,8A,8B,9,10,11	1*,2,3,7*,8A,8B,9,10,11	1*,2,3,7*,8A,8B,9,10,11
7	Group A test requirements	1,2,3,4**,7,8A,8B,9,10,11	1,2,3,4**,7,8A,8B,9,10,11	1,2,3,4**,7,8A,8B,9,10,11
8	Group C end-point electrical parameters	2,3,7,8A,8B	1,2,3,7,8A,8B	1,2,3,7,8A,8B,9,10,11 Δ
9	Group D end-point electrical parameters	2,3,8A,8B	1,7,9	1,7,9
10	Group E end-point electrical parameters	1,7,9	1,7,9	1,7,9

1/ Blank spaces indicate tests are not applicable.

2/ Any or all subgroups may be combined when using high-speed testers.

3/ Subgroups 7 and 8 functional tests shall verify the truth table.

4/ * indicates PDA applies to subgroup 1 and 7.

5/ ** see 4.4.1d.

6/ Δ indicates delta limit (see table IIB) shall be required where specified, and the delta values shall be computed with reference to the previous interim electrical parameters (see line 1). For device class V performance of delta limits shall be as specified in the manufacturer's QM plan.

TABLE IIB. Delta limits at +25°C.

Test 1/	Device types
	All
I _{CC3} standby	±10% of specified value in table IA
I _{ILK} , I _{OLK}	±10% of specified value in table IA

1/ The above parameters shall be recorded before and after the required burn-in and life tests to determine the delta.

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4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

- a. Delete the sequence specified as initial (preburn-in) electrical parameters through interim (postburn-in) electrical parameters of method 5004 and substitute lines 1 through 6 of table IIA herein.
- b. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.
 - (1) Dynamic burn-in (method 1015 of MIL-STD-883, test condition D; for circuit, see 4.2.1b herein).
- c. Interim and final electrical parameters shall be as specified in table IIA herein.

4.2.2 Additional criteria for device classes Q and V.

- a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.
- b. Interim and final electrical test parameters shall be as specified in table IIA herein.
- c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-PRF-38535 permits alternate in-line control testing. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

- a. Tests shall be as specified in table IIA herein.
- b. Subgroups 5 and 6 of table I of method 5005 of MIL-STD-883 shall be omitted.
- c. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).
- d. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured only for initial qualification and after any process or design changes which may affect input or output capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency of 1 MHz. Sample size is 15 devices with no failures, and all input and output terminals tested.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

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4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

- a. Test condition D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.
- b. $T_A = +125^{\circ}\text{C}$, minimum.
- c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

- a. End-point electrical parameters shall be as specified in table IIA herein.
- b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table IA at $T_A = +25^{\circ}\text{C} \pm 5^{\circ}\text{C}$, after exposure, to the subgroups specified in table IIA herein.
- c. For device class M subgroups 1 and 2 of table V method 5005 of MIL-STD-883, and for device classes Q and V subgroups 1 and 2 of table C-I or Table B-I (appendix B) of MIL-PRF-38535, shall be tested as appropriate for device construction.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019 and as specified herein.

4.4.4.1.1 Accelerated aging test. Accelerated aging shall be performed on all devices requiring a RHA level greater than 5K rads(Si). The post-anneal end point electrical parameter limits shall be as specified in table IA herein and shall be the pre-irradiation end point electrical parameter limit at $25^{\circ}\text{C} \pm 5^{\circ}\text{C}$. Testing shall be performed at initial qualification and after any design or process changes which may effect the RHA response of the device.

4.4.4.2 Transient dose rate upset.

- a. For device types 01, 02, 05, and 06, devices shall be capable of retaining stored data during and after exposure to a transient ionizing radiation pulse of $<1\mu\text{s}$ up to and including 10^9 Rads (Si)/sec when applied under recommended operating conditions.
- b. For device types 03 and 04, devices shall be capable of retaining stored data during and after exposure to a transient ionizing radiation pulse of $<1\mu\text{s}$ up to and including 10^9 Rads (Si)/sec when applied under recommended operating conditions.
- c. The dose rate upset specification is valid only if the V_{DD} to V_{SS} potential difference applied to the package remains within the recommended operation range during transient radiation.

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- d. Transient dose rate survivability - The device shall not be rendered permanently incapable of meeting any functional or electrical specifications by a 50 ns transient ionizing radiation pulse of up to and including 10^{11} Rads (Si)/sec for device types 01, 02, 05, 06 and 10^{12} Rads (Si)/sec for device types 03 and 04 when applied under recommended operating conditions. The current conducted during the pulse in the SRAM inputs, outputs, and particularly power supply may significantly exceed the normal operating levels.

4.4.4.3 Single event phenomena (SEP). SEP testing shall be required on class V devices. SEP testing shall be performed on the SEC or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latchup characteristics. Test four devices with zero failures. ASTM standard F1192 may be used as a guideline when performing SEP testing. The test conditions for SEP are as follows:

- The ion beam angle of incidence shall be normal to the die surface and 60 degrees to the normal, inclusive (i.e., $0^\circ \leq \text{angle} \leq 60^\circ$). No shadowing of the ion beam due to fixturing or package related effects is allowed.
- The fluence shall be greater than 100 errors or $\geq 10^7$ ions/cm².
- The flux shall be between 10^2 and 10^5 ion/cm²/s. The cross section shall be verified to be flux independent by measuring the cross section at two flux rates which differ by at least an order of magnitude.
- The particle range shall be ≥ 20 microns in silicon.
- The test temperature shall be $+25^\circ\text{C}$ and the maximum rated operating temperature $\pm 10^\circ\text{C}$.
- Bias conditions shall be $V_{CC} = 4.5\text{ V dc}$ for the upset measurements and $V_{CC} = 5.5\text{ V dc}$ for the latchup measurements.
- For SEP test limits see table IB herein.

4.5 Delta measurements for device class V. Delta measurements, as specified in table IIA, shall be made and recorded before and after the required burn-in screens and steady-state life tests to determine delta compliance. The electrical parameters to be measured, with associated delta limits are listed in table IIB. The device manufacturer may, at his option, either perform delta measurements or within 24 hours after burn-in perform final electrical parameter tests, subgroups 1, 7, and 9.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0525.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43216-5000, or telephone (614) 692-0674.

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6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535, MIL-HDBK-1331, and herein.

C_{IN}, C_{OUT} Input and bidirectional output capacitance, terminal-to-GND.
 GND Ground zero voltage potential.
 I_{CC} Supply current.
 I_{IL} Input current low.
 I_{IH} Input current high.
 T_C Case temperature.
 T_A Ambient temperature.
 V_{CC} Positive supply voltage.
 OV Latch-up over-voltage.

6.5.1 Timing parameter abbreviations. All timing abbreviations use lower case characters with upper case character subscripts. The initial character is always "t" and is followed by four descriptors. These characters specify two signal points arranged in a "from-to" sequence that define a timing interval. The two descriptors for each signal specify the signal name and the signal transition. The format is as follows:

	t	X	X	X	X
		-	-	-	-
		*	*	*	*
Signal name from which interval is defined _____		*	*	*	*
Transition direction for first signal _____			*	*	*
Signal name to which interval is defined _____				*	*
Transition direction for second signal _____					*

a. Signal definitions:

A = Address input bus	S = Chip select
D = Data in	G = Output enable
Q = Data out	E = Chip enable
W = Write enable	

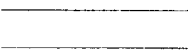
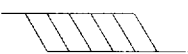
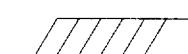
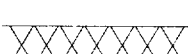
b. Transition definitions:

H = Transition to high
 L = Transition to low
 V = Transition to valid
 X = Transition to invalid or don't care
 Z = Transition to off (high impedance)

6.5.2 Timing limits. The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

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6.5.3 Waveforms

Waveform symbol	Input	Output
	MUST BE VALID	WILL BE VALID
	CHANGE FROM H TO L	WILL CHANGE FROM H TO L
	CHANGE FROM L TO H	WILL CHANGE FROM L TO H
	DON'T CARE ANY CHANGE PERMITTED	CHANGING STATE UNKNOWN
		HIGH IMPEDANCE

6.5.4 Additional information. When specified in the purchase order or contract, a copy of the following additional data shall be supplied.

- RHA upset levels.
- Test conditions (SEP).
- Number of upsets (SEP).
- Number of transients (SEP).
- Occurrence of latchup (SEP).

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

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APPENDIX

FUNCTIONAL ALGORITHMS

10. SCOPE

10.1 Scope. Functional algorithms are test patterns which define the exact sequence of events used to verify proper operation of a random access memory (RAM). Each algorithm serves a specific purpose for the testing of the device. It is understood that all manufacturers do not have the same test equipment; therefore, it becomes the responsibility of each manufacturer to guarantee that the test patterns described herein are followed as closely as possible, or equivalent patterns be used that serve the same purpose. Each manufacturer should demonstrate that this condition will be met. Algorithms shall be applied to the device in a topologically pure fashion. This appendix is a mandatory part of the specification. The information contained herein is intended for compliance.

20. APPLICABLE DOCUMENTS. This section is not applicable to this appendix.

30. ALGORITHMS

30.1 Algorithm A (pattern 1).

30.1.1 Checkerboard, checkerboard-bar.

- Step 1. Load memory with a checkerboard data pattern by incrementing from location 0 to maximum.
- Step 2. Read memory, verifying the output checkerboard pattern by incrementing from location 0 to maximum.
- Step 3. Load memory with a checkerboard-bar pattern by incrementing from location 0 to maximum.
- Step 4. Read memory, verifying the output checkerboard-bar pattern by incrementing from location 0 to maximum.

30.2 Algorithm B (pattern 2).

30.2.1 March.

- Step 1. Load memory with background data, incrementing from minimum to maximum address locations (All "0's").
- Step 2. Read data in location 0.
- Step 3. Write complement data to location 0.
- Step 4. Read complement data in location 0.
- Step 5. Repeat steps 2 through 4 incrementing X-fast sequentially, for each location in the array.
- Step 6. Read complement data in maximum address location.
- Step 7. Write data to maximum address location.
- Step 8. Read data in maximum address location.
- Step 9. Repeat steps 6 through 8 decrementing X-fast sequentially for, each location in the array.
- Step 10. Read data in location 0.
- Step 11. Write complement data to location 0.
- Step 12. Read complement data in location 0.
- Step 13. Repeat steps 10 through 12 decrementing X-fast sequentially for each location in the array.
- Step 14. Read complement data in maximum address location.
- Step 15. Write data to maximum address location.
- Step 16. Read data in maximum address location.
- Step 17. Repeat steps 14 through 16 incrementing X-fast sequentially for each location in the array.
- Step 18. Read background data from memory, decrementing X-fast from maximum to minimum address locations.

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30.3 Algorithm C (pattern 3).

30.2.1 XY March.

- Step 1. Load memory with background data, incrementing from minimum to maximum address locations (All "0's").
- Step 2. Read data in location 0.
- Step 3. Write complement data to location 0.
- Step 4. Read complement data in location 0.
- Step 5. Repeat steps 2 through 4 incrementing Y-fast sequentially, for each location in the array.
- Step 6. Read complement data in maximum address location.
- Step 7. Write data to maximum address location.
- Step 8. Read data in maximum address location.
- Step 9. Repeat steps 6 through 8 decrementing X-fast sequentially for each location in the array.
- Step 10. Read data in location 0.
- Step 11. Write complement data to location 0.
- Step 12. Read complement data in location 0.
- Step 13. Repeat steps 10 through 12 decrementing Y-fast sequentially for each location in the array.
- Step 14. Read complement data in maximum address location.
- Step 15. Write data to maximum address location.
- Step 16. Read data in maximum address location.
- Step 17. Repeat steps 14 through 16 incrementing X-fast sequentially for each location in the array.
- Step 18. Read background data from memory, decrementing Y-fast from maximum to minimum address locations.

30.4 Algorithm D (pattern 4).

30.4.1 CEDES - CE deselect checkerboard, checkerboard-bar.

- Step 1. Load memory with a checkerboard data pattern by incrementing from location 0 to maximum.
- Step 2. Deselect device, attempt to load memory with checkerboard-bar data pattern by incrementing from location 0 to maximum.
- Step 3. Read memory, verifying the output checkerboard pattern by incrementing from location 0 to maximum.
- Step 4. Load memory with a checkerboard-bar pattern by incrementing from location 0 to maximum.
- Step 5. Deselect device, attempt to load memory with checkerboard data pattern by incrementing from location 0 to maximum.
- Step 6. Read memory, verifying the output checkerboard-bar pattern by incrementing from location 0 to maximum.

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STANDARD MICROCIRCUIT DRAWING SOURCE APPROVAL BULLETIN

DATE: 97-06-12

Approved sources of supply for SMD 5962-95845 are listed below for immediate acquisition only and shall be added to MIL-HDBK-103 and QML-38535 during the next revisions. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revisions of MIL-HDBK-103 and QML-38535.

Standard microcircuit drawing PIN <u>1</u> /	Vendor CAGE number	Vendor similar PIN <u>2</u> /
5962R9584501QXC	34168	HX6256/RQRC
5962R9584501VXC	34168	HX6256/RVRC
5962F9584501QXC	34168	HX6256/RQFC
5962F9584501VXC	34168	HX6256/RVFC
5962H9584501QXC	34168	HX6256/RQHC
5962H9584501VXC	34168	HX6256/RVHC
5962R9584501QYC	34168	HX6256/NQRC
5962R9584501VYC	34168	HX6256/NVRC
5962F9584501QYC	34168	HX6256/NQFC
5962F9584501VYC	34168	HX6256/NVFC
5962H9584501QYC	34168	HX6256/NQHC
5962H9584501VYC	34168	HX6256/NVHC
5962R9584501QZC	34168	HX6256/XQRC
5962R9584501VZC	34168	HX6256/XVRC
5962F9584501QZC	34168	HX6256/XQFC
5962F9584501VZC	34168	HX6256/XVFC
5962H9584501QZC	34168	HX6256/XQHC
5962H9584501VZC	34168	HX6256/XVHC
5962R9584502QXC	34168	HX6256/RQRT
5962R9584502VXC	34168	HX6256/RVRT
5962F9584502QXC	34168	HX6256/RQFT
5962F9584502VXC	34168	HX6256/RVFT
5962H9584502QXC	34168	HX6256/RQHT
5962H9584502VXC	34168	HX6256/RVHT

See footnotes at end of list.

Standard microcircuit drawing PIN <u>1</u> /	Vendor CAGE number	Vendor similar PIN <u>2</u> /
5962R9584502QYC	34168	HX6256/NQRT
5962R9584502VYC	34168	HX6256/NVRT
5962F9584502QYC	34168	HX6256/NQFT
5962F9584502VYC	34168	HX6256/NVFT
5962H9584502QYC	34168	HX6256/NQHT
5962H9584502VYC	34168	HX6256/NVHT
5962R9584502QZC	<u>2</u> /	HX6256/XQRT
5962R9584502VZC	<u>2</u> /	HX6256/XVRT
5962F9584502QZC	<u>2</u> /	HX6256/XQFT
5962F9584502VZC	<u>2</u> /	HX6256/XVFT
5962H9584502QZC	<u>2</u> /	HX6256/XQHT
5962H9584502VZC	<u>2</u> /	HX6256/XVHT
5962R9584502QUC	34168	HX6256/PQRT
5962R9584502VUC	34168	HX6256/PVRT
5962F9584502QUC	34168	HX6256/PQFT
5962F9584502VUC	34168	HX6256/PVFT
5962H9584502QUC	34168	HX6256/PQHT
5962H9584502VUC	34168	HX6256/PVHT
5962R9584503QZC	34168	HX6356/XQRC
5962R9584503VZC	34168	HX6356/XVRC
5962F9584503QZC	34168	HX6356/XQFC
5962F9584503VZC	34168	HX6356/XVFC
5962H9584503QZC	34168	HX6356/XQHC
5962H9584503VZC	34168	HX6356/XVHC
5962R9584504QZC	<u>2</u> /	HX6356/XQRT
5962R9584504VZC	<u>2</u> /	HX6356/XVRT
5962F9584504QZC	<u>2</u> /	HX6356/XQFT
5962F9584504VZC	<u>2</u> /	HX6356/XVFT
5962H9584504QZC	<u>2</u> /	HX6356/XQHT
5962H9584504VZC	<u>2</u> /	HX6356/XVHT

See footnotes at end of list.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962R9584504QUC	34168	HX6356/PQRT
5962R9584504VUC	34168	HX6356/PVRT
5962F9584504QUC	34168	HX6356/PQFT
5962F9584504VUC	34168	HX6356/PVFT
5962H9584504QUC	34168	HX6356/PQHT
5962H9584504VUC	34168	HX6356/PVHT
5962R9584505QXC	3/	HX6256/RQRC20
5962R9584505VXC	3/	HX6256/RVRC20
5962F9584505QXC	3/	HX6256/RQFC20
5962F9584505VXC	3/	HX6256/RVFC20
5962H9584505QXC	3/	HX6256/RQHC20
5962H9584505VXC	3/	HX6256/RVHC20
5962R9584505QYC	3/	HX6256/NQRC20
5962R9584505VYC	3/	HX6256/NVRC20
5962F9584505QYC	3/	HX6256/NQFC20
5962F9584505VYC	3/	HX6256/NVFC20
5962H9584505QYC	3/	HX6256/NQHC20
5962H9584505VYC	3/	HX6256/NVHC20
5962R9584505QZC	3/	HX6256/XQRC20
5962R9584505VZC	3/	HX6256/XVRC20
5962F9584505QZC	3/	HX6256/XQFC20
5962F9584505VZC	3/	HX6256/XVFC20
5962H9584505QZC	3/	HX6256/XQHC20
5962H9584505VZC	3/	HX6256/XVHC20
5962R9584506QXC	3/	HX6256/RQRT20
5962R9584506VXC	3/	HX6256/RVRT20
5962F9584506QXC	3/	HX6256/RQFT20
5962F9584506VXC	3/	HX6256/RVFT20
5962H9584506QXC	3/	HX6256/RQHT20
5962H9584506VXC	3/	HX6256/RVHT20

See footnotes at end of list.

Standard microcircuit drawing PIN <u>1/</u>	Vendor CAGE number	Vendor similar PIN <u>2/</u>
5962R9584506QYC	<u>3/</u>	HX6256/NQRT20
5962R9584506VYC	<u>3/</u>	HX6256/NVRT20
5962F9584506QYC	<u>3/</u>	HX6256/NQFT20
5962F9584506VYC	<u>3/</u>	HX6256/NVFT20
5962H9584506QYC	<u>3/</u>	HX6256/NQHT20
5962H9584506VYC	<u>3/</u>	HX6256/NVHT20
5962R9584506QZC	<u>3/</u>	HX6256/XQRT20
5962R9584506VZC	<u>3/</u>	HX6256/XVRT20
5962F9584506QZC	<u>3/</u>	HX6256/XQFT20
5962F9584506VZC	<u>3/</u>	HX6256/XVFT20
5962H9584506QZC	<u>3/</u>	HX6256/XQHT20
5962H9584506VZC	<u>3/</u>	HX6256/XVHT20

- 1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. The device manufacturers listed herein are authorized to supply alternate lead finishes "A", "B", or "C" at their discretion. Contact the listed approved source of supply for further information.
- 2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
- 3/ Not available from an approved source of supply.

Vendor CAGE
number

34168

Vendor name
and address

Honeywell Inc.
Solid State Electronics Center
12001 State Hwy 55
Plymouth, MN 55441

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