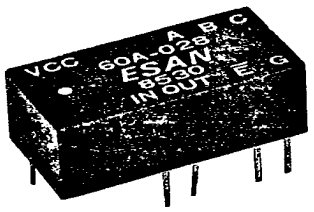
Programmable Delay Line (TTL)

60A Series

- **16 Pin Dip Package**
- **Digitally Programmable in 8 Delay Steps (3 Bits)**



PART NO.	ZERO STEP (ns)	MAXIMUM DELAY (ns)	PER STEP (ns)
60A-007	7±2	14±2	1±0.5
60A-014	〃	21±2	2±0.6
60A-021	〃	28±2	3±0.7
60A-028	〃	35±2	4±0.8
60A-035	〃	42±2.1	5±1.0
60A-042	〃	49±2.4	6±1.2
60A-049	〃	56±2.8	7±1.4
60A-056	〃	63±3.1	8±1.6
60A-063	〃	70±3.5	9±1.8
60A-070	〃	77±3.8	10±2.0
60A-077	〃	84±4.2	11±2.0
60A-084	7±2	91±4.5	12±2.0

- Operating Temperature : 0°C to 70°C (−550C ~ +125°C on request)
- Temperature Coefficient : 500 ppm/°C
- Logic 1 Input Voltage : 2V min; 5.5v max
- Logic 1 Input Current : 100μA @2.4V, 2mA @5.5V
- Logic 0 Input Voltage : 0.8V max
- Logic 0 Input Current : −4mA max
- Logic 1 Output Voltage : 2.4V min
- Logic 0 Output Voltage : 0.4V max
- Rise Time : 4ns max

Test Conditions:

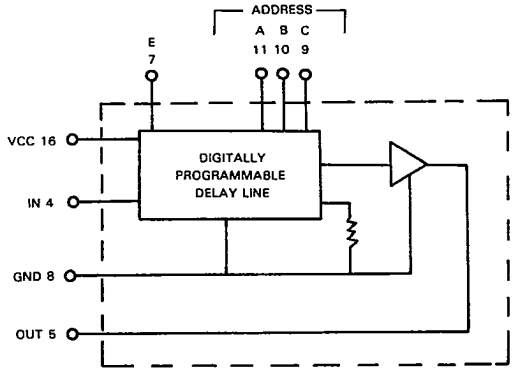
- Vcc = 5.0VDC, Temp. 25°C
- Time delay measured at the 1.5 volt level of the leading edge
- Rise time measured from .75V to 2.4 volts
- Output loaded with 15pf
- Input pulse width: 3 * max time delay
- Pulse amplitude: 3.0 volts
- Pulse spacing: 1000ns

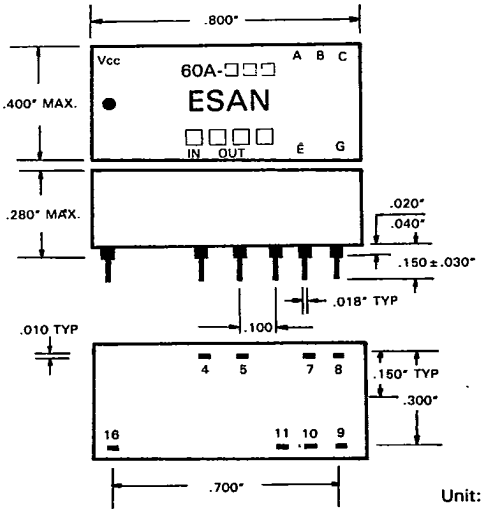
Truth Table

Enable	ADDRESS (BIT NO.) C	B	A	DELAY OUT
0	0	0	0	T_0
0	0	0	1	T_1
0	0	1	0	T_2
0	0	1	1	T_3
0	1	0	0	T_4
0	1	0	1	T_5
0	1	1	0	T_6
0	1	1	1	T_7
1	ϕ	ϕ	ϕ	0

1 = High
0 = Low
ϕ 0 = Don't care

T_0 Reference or inherent delay of circuit.
T_1 to T_7 = Multiplier of incremental delay.





Unit: Inch