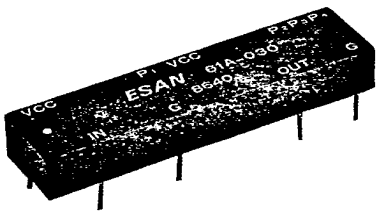
Programmable Delay Line (TTL)

61A Series

- **32 Pin Dip Package**
- **Digitally Programmable in 16 Delay Steps (4 Bits)**



Specifications:

- Operating Temperature : 0°C to 70°C (−55°C~ +125°C on request)
- Temperature Coefficient : 300 ppm/°C
- Logic 1 Input Voltage : 2V min; 5.5V max
- Logic 1 Input Current : 100μA @ 2.4V, 2mA @5.5V
- Logic 0 Input Voltage : 0.8V max
- Logic 0 Input Current : −4mA max
- Logic 1 Output Voltage : 2.4V min
- Logic 0 Output Voltage : 0.4V max
- Rise Time : 4NS max
- Delay Tolerance : ±5% or 2ns Whichever is greater

Test Conditions:

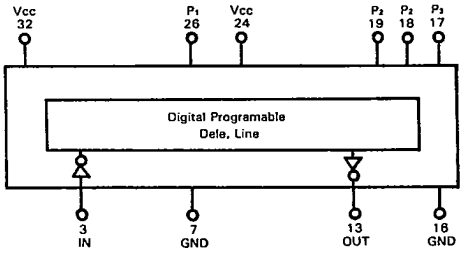
- Vcc = 5.0VDC, Temp. 25°C
- Time delay measured at the 1.5 volt level of the leading edge
- Rise time measured from .75V to 2.4 volts
- Output loaded with 15pf
- Input pulse width: 3 × max time delay
- Pulse amplitude: 3.0 volts
- Pulse spacing: 1000ns

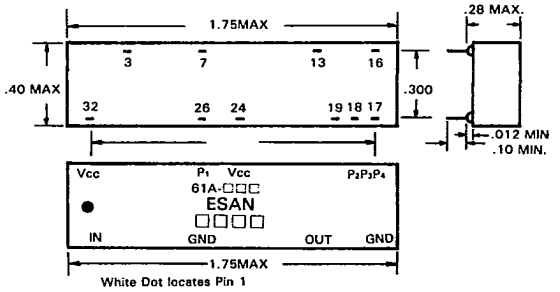
PART NO.	ZERO STEP (ns)	MAXIMUM DELAY (ns)	PER STEP (ns)
61A-015	15±2	30	1±0.5
61A-030	"	45	2±0.6
61A-045	"	60	3±0.7
61A-060	"	75	4±0.8
61A-070	"	90	5±1.0
61A-090	"	105	6±1.2
61A-105	"	120	7±1.4
61A-120	"	135	8±1.6
61A-135	"	150	9±1.8
61A-150	15±2	165	10±2.0

Truth Table

ADDRESS 4	3	2	1	DELAY OUT
0	0	0	0	T_0
0	0	0	1	T_1
0	0	1	0	T_2
0	0	1	1	T_3
0	1	0	0	T_4
0	1	0	1	T_5
0	1	1	0	T_6
0	1	1	1	T_7
1	0	0	0	T_8
1	0	0	1	T_9
1	0	1	0	T_{10}
1	0	1	1	T_{11}
1	1	0	0	T_{12}
1	1	0	1	T_{13}
1	1	1	0	T_{14}
1	1	1	1	T_{15}

0 = Logic 0 1 = Logic
T_0 = Reference inherent delay of unit.
T_1 – T_{15} Multiplier of incremental delay.





Unit: Inch