

4-25

BURN-IN CONDITIONS:

$V_{CC} = 5.0 \text{ V(min)}/6.0 \text{ V(max)}$, $R_1 = 39.2 \text{ k}\Omega \pm 20\%$, $C_1 = 0.1 \text{ }\mu\text{F} \pm 20\%$,
 $V_H = 3.0 \text{ V(min)}/5.0 \text{ V(max)}$, $V_L = -0.5 \text{ V(min)}/0.0 \text{ V(max)}$,

CP1: 100 kHz CP6: 3.125 kHz CP11: 97.66 Hz CP16: 3.052 Hz
 CP2: 50 kHz CP7: 1.563 kHz CP12: 48.83 Hz CP17: 1.526 Hz
 CP3: 25 kHz CP8: 0.781 kHz CP13: 24.41 Hz CP18: 0.763 Hz
 CP4: 12.5 kHz CP9: 0.391 kHz CP14: 12.21 Hz CP19: 0.382 Hz
 CP5: 6.25 kHz CP10: 0.195 kHz CP15: 6.104 Hz CP20: 0.191 Hz

PIN NAME and FUNCTIONS

$A_0 - A_{16}$	Address Inputs
$\bar{W}$	Write Enable
$\bar{E}$, E	Chip Enable
$\bar{G}$	Output Enable
DQ ₀ - DQ ₇	Data Input/Outputs
V_{CC}	+ 5.0 V Power Supply
V_{SS}	Ground
N.C.	No Connection

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum rated voltages to this high-impedance circuit.

PIN ASSIGNMENTS

Function	DIL 875-01	LCC 766C-01	FP	Burn-In (Condition-D)
N.C.	1	1	1	N.C.
A ₁₆	2	2	2	CP2
A ₁₄	3	3	3	CP3
A ₁₂	4	4	4	CP4
A ₇	5	5	5	CP5
A ₆	6	6	6	CP6
A ₅	7	7	7	CP7
A ₄	8	8	8	CP8
A ₃	9	9	9	CP9
A ₂	10	10	10	CP10
A ₁	11	11	11	CP11
A ₀	12	12	12	CP12
DQ ₀	13	13	13	CP20 to R ₁
DQ ₁	14	14	14	CP20 to R ₁
DQ ₂	15	15	15	CP20 to R ₁
V_{SS}	16	16	16	GND
DQ ₃	17	17	17	CP20 to R ₁
DQ ₄	18	18	18	CP21 to R ₁
DQ ₅	19	19	19	CP21 to R ₁
DQ ₆	20	20	20	CP21 to R ₁
DQ ₇	21	21	21	CP21 to R ₁
$\bar{E}$	22	22	22	GND
A ₁₀	23	23	23	CP18
$\bar{G}$	24	24	24	CP19
A ₁₁	25	25	25	CP17
A ₉	26	26	26	CP16
A ₈	27	27	27	CP15
A ₁₃	28	28	28	CP14
$\bar{W}$	29	29	29	CP1
E	30	30	30	HIGH
A ₁₅	31	31	31	CP13
V_{CC}	32	32	32	V_{CC} , C ₁ to GND

TRUTH TABLE

$\bar{E}_1$	E ₂	$\bar{G}$	$\bar{W}$	Mode	V_{CC} Current	DQ Pin	Data Operation
H	X	X	X	Not Selected	I_{SB1}, I_{SB2}	High Z	Don't Care
X	L	X	X	Not Selected	I_{SB1}, I_{SB2}	High Z	Don't Care
L	H	H	H	Read Suppressed	I_{CCA}	High Z	Don't Care
L	H	L	H	Read	I_{CCA}	Active	D _{OUT}
L	H	X	L	Write	I_{CCA}	High Z	D _{IN}

X = Don't Care

MOTOROLA SC MEMORY/ASI 65E D

COMMERCIAL PLUS AND MIL/AERO APPLICATIONS MEMORY DATA

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	- 0.5 to + 7.0	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{IN}, V_{OUT}	- 0.5 to $V_{CC} + 0.5$	V
Output Current	I_{OUT}	± 20	mA
Power Dissipation	P_D	1.0	W
Temperature Under Bias ($T_A = 25^\circ\text{C}$)	T_{bias}	- 55 to +125	$^\circ\text{C}$
Storage Temperature Range	T_{stg}	- 65 to +150	$^\circ\text{C}$
Operating Temperature Range	T_A	- 55 to +125	$^\circ\text{C}$

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

($V_{CC} = 5.0 \text{ V} \pm 10\%$, $T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Nominal	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.2	3.0	$V_{CC} + 0.3$	V
Input Low Voltage	V_{IL}	- 0.5 *	0.0	0.8	V

* $V_{IL}(\text{min}) = -0.5 \text{ Vdc}$; $V_{IL}(\text{min}) = -3.0 \text{ Vdc}$ (pulse width $\leq 20 \text{ ns}$)

DC CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Unit
Input Leakage Current (All Inputs, $V_{in} = 0$ to V_{CC})	$I_{kg(I)}$	—	—	± 10	μA
Output Leakage Current ($\bar{E} = V_{IH}$, $V_{OUT} = 0$ to V_{CC})	$I_{kg(O)}$	—	—	± 10	μA
AC Supply Current ($I_{OUT} = 0 \text{ mA}$)	6226A-25: $t_{AVAV} = 25 \text{ ns}$	I_{CCA}	—	140	mA
	6226A-30: $t_{AVAV} = 30 \text{ ns}$	I_{CCA}	—	140	mA
	6226A-35: $t_{AVAV} = 35 \text{ ns}$	I_{CCA}	—	135	mA
	6226A-45: $t_{AVAV} = 45 \text{ ns}$	I_{CCA}	—	125	mA
	6226A-55: $t_{AVAV} = 55 \text{ ns}$	I_{CCA}	—	125	mA
	6226A-70: $t_{AVAV} = 70 \text{ ns}$	I_{CCA}	—	120	mA
	6226A-100: $t_{AVAV} = 100 \text{ ns}$	I_{CCA}	—	110	mA
TTL Standby Current ($\bar{E} = V_{IH}$, No Restrictions on Other Inputs)	I_{SB1}	—	—	25	mA
CMOS Standby Current ($\bar{E} \geq V_{CC} - 2.0 \text{ V}$, No Restrictions on Other Inputs)	I_{SB2}	—	—	10	mA
Output Low Voltage ($I_{OL} = 8.0 \text{ mA}$)	V_{OL}	—	—	0.4	V
Output High Voltage ($I_{OH} = -4.0 \text{ mA}$)	V_{OH}	2.4	—	—	V

MOTOROLA SC MEMORY/ASI 65E D

COMMERCIAL PLUS AND MIL/AERO APPLICATIONS MEMORY DATA

CAPACITANCE ($f = 1.0 \text{ MHz}$, $dV = 3.0 \text{ V}$, $T_A = 25^\circ\text{C}$, Periodically Sampled Rather Than 100% Tested)				
Characteristic		Symbol	Typ	Max
Input Capacitance	All Inputs Except $\bar{E}$, E and DQ	C_{in}	4.0	6.0
			5.0	7.0
I/O Capacitance	DQ	$C_{I/O}$	5.0	7.0
				Unit
				pF
				pF

MOTOROLA SC (MEMORY/ASI) 65E D

AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V $\pm$ 10%, T_A = -55°C to +125°C, Unless Otherwise Noted)

Input Timing Measurement Reference Level	1.5 V
Input Pulse levels	0 to 3.0 V
Input Rise/Falls Time	$\geq 5.0 \text{ ns}$
Output Timing Measurement Reference Level	1.5 V
Output Load	See Figure 1A

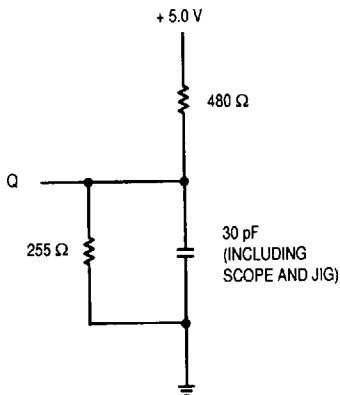
AC TEST LOADS
OR EQUIVALENT

Figure 1A.

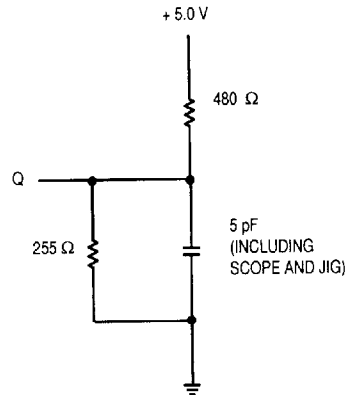


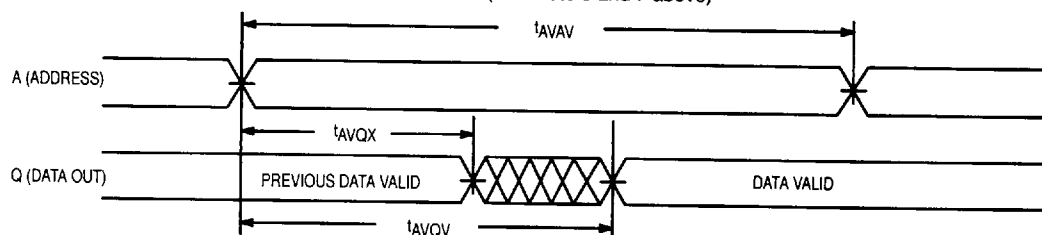
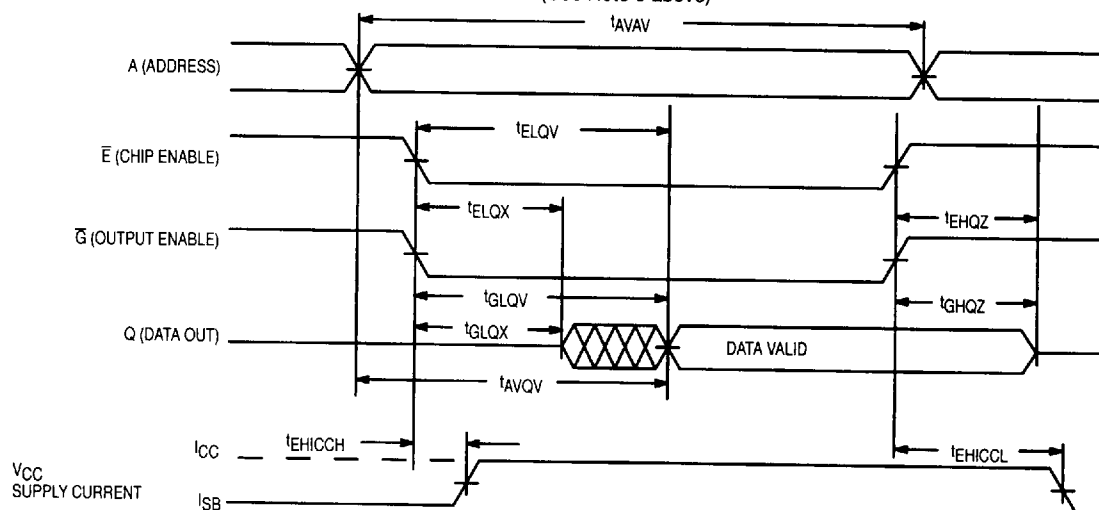
Figure 1B.

READ CYCLE (See Note 1)

Parameter	Symbol Standard	Symbol Alternate	6226A-25		6226A-30		6226A-35		6226A-45		Unit	Notes
			Min	Max	Min	Max	Min	Max	Min	Max		
Read Cycle Time	t_{AVAV}	t_{RC}	25	—	30	—	35	—	45	—	ns	2, 5, 7
Address Access Time	t_{AVQV}	t_{AA}	—	25	—	30	—	35	—	45	ns	5, 7
Chip Select Access Time	t_{ELQV}	t_{ACS}	—	25	—	30	—	35	—	45	ns	6
Output Enable Access Time	t_{GLQV}	t_{OE}	—	10	—	10	—	15	—	20	ns	5
Prior Output Hold Time After Address Change	t_{AVQX}	t_{OH}	3.0	—	3.0	—	3.0	—	3.0	—	ns	5, 7
Output High Z after Chip Enable	t_{ELQX}	t_{CLZ}	3.0	—	3.0	—	3.0	—	3.0	—	ns	3, 4, 6, 7
Output High Z after Chip Disable	t_{EHQZ}	t_{CHZ}	—	10	—	10	—	15	—	20	ns	3, 4, 7
Output High Z after Output Enable	t_{GLQX}	t_{OLZ}	0	—	0	—	0	—	0	—	ns	3, 4, 5
Output High Z after Output Disable	t_{GHQZ}	t_{OHZ}	0	10	0	10	0	15	0	20	ns	3, 4, 5
Power Up Time	t_{ELICCH}	t_{PU}	0	—	0	—	0	—	0	—	ns	4
Power Down Time	t_{EHICCL}	t_{PD}	—	25	—	30	—	35	—	45	ns	4

NOTES:

1. $\bar{W}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transitioning address.
3. Transition is measured ± 500 mV from steady-state voltage with load of Figure 1B.
4. These parameters are periodically sampled and not 100% tested.
5. Device is continuously selected ($E_1 = V_{IL}$, $E_2 = V_{IH}$).
6. Address valid prior to coincident with E_1 going low/ E_2 going high.
7. Outputs are continuously enabled ($\bar{G} = V_{IL}$).

READ CYCLE 1 (See Note 5 and 7 above)**READ CYCLE 2** (See Note 6 above)

READ CYCLE (See Note 1)										
Parameter	Symbol Standard	Symbol Alternate	6226A-55		6226A-70		6226A-100		Unit	Notes
			Min	Max	Min	Max	Min	Max		
Read Cycle Time	tAVAV	tRC	55	—	70	—	100	—	ns	2, 5, 7
Address Access Time	tAVQV	tAA	—	55	—	70	—	100	ns	5, 7
Chip Select Access Time	tELQV	tACS	—	55	—	70	—	100	ns	6
Output Enable Access Time	tGLQV	tOE	—	20	—	25	—	25	ns	5
Prior Output Hold Time After Address Change	tAVQX	tOH	3.0	—	3.0	—	3.0	—	ns	5, 7
Output High Z after Chip Enable	tELQX	tCLZ	3.0	—	3.0	—	3.0	—	ns	3, 4, 6, 7
Output High Z after Chip Disable	tEHQZ	tCHZ	—	20	—	30	—	30	ns	3, 4, 7
Output High Z after Output Enable	tGLQX	tOLZ	0	—	0	—	0	—	ns	3, 4, 5
Output High Z after Output Disable	tGHQZ	tOHZ	0	20	0	30	0	30	ns	3, 4, 5
Power Up Time	tELICCH	tPU	0	—	0	—	0	—	ns	4
Power Down Time	tEHICCL	tPD	—	55	—	70	—	100	ns	4

NOTES:

1. $\bar{W}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transitioning address.
3. Transition is measured ± 500 mV from steady-state voltage with load of Figure 1B.
4. These parameters are periodically sampled and not 100% tested.
5. Device is continuously selected ($E_1 = V_{IL}$, $E_2 = V_{IH}$).
6. Address valid prior to coincident with E_1 going low/ E_2 going high.
7. Outputs are continuously enabled ($\bar{G} = V_{IL}$).

MOTOROLA SC MEMORY/ASI 65E D

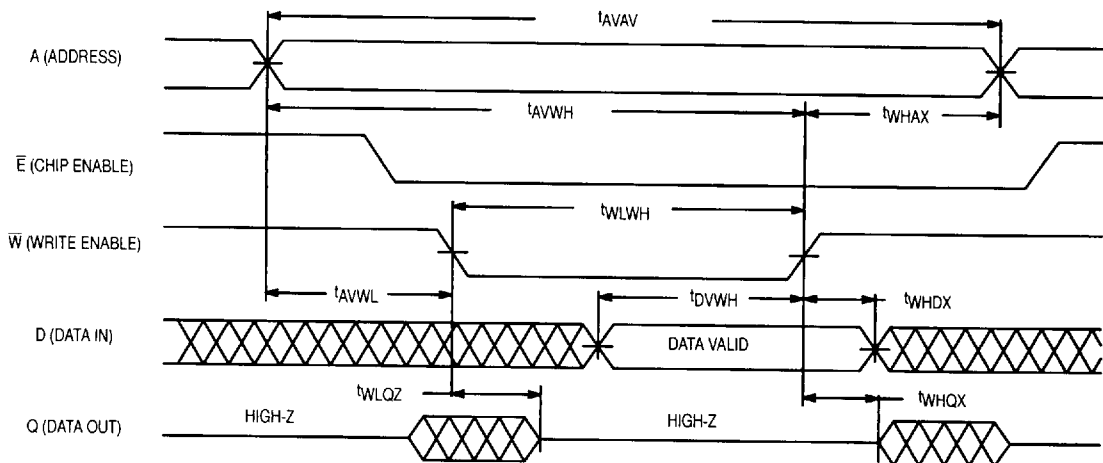
WRITE CYCLE 1 ($\overline{W}$ Controlled, See Note 1)												
Parameter	Symbol Standard	Symbol Alternate	6226A-25		6226A-30		6226A-35		6226A-45		Unit	Notes
			Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	tAVAV	tWC	25	—	30	—	35	—	45	—	ns	2
Write Address Setup Time	tAVWL	tWAS	0	—	0	—	0	—	0	—	ns	—
Write Address Valid to End of Write	tAVWH	tAW	20	—	20	—	25	—	35	—	ns	—
Write Pulse Width	tWLWH	tWP	20	—	20	—	30	—	35	—	ns	—
Write Data Valid to End of Write	tDVWH	tDWS	15	—	15	—	20	—	25	—	ns	—
Write Data Hold Time	tWHDX	tDWH	0	—	0	—	0	—	0	—	ns	—
Write Enable Time	tWLQZ	tWZ	0	10	0	10	0	15	0	20	ns	4
Output High Z after Write Disable	tWHQX	tWHZ	5.0	—	5.0	—	5.0	—	5.0	—	ns	4
Write Address Hold Time	tWHAX	tWAH	5.0	—	5.0	—	5.0	—	5.0	—	ns	—

NOTES:

1. A write occurs during the overlap of $\bar{W}$ low while continuously E_1 is low and E_2 high.
2. All write cycle timing is referenced from the last valid address to the first transitioning address.
3. Transition is measured ± 500 mV from steady-state voltage with load of Figure 1B.
4. Parameters is sampled and not 100% tested.

WRITE CYCLE 1 ($\bar{W}$ Controlled, See Note 1)

Parameter	Symbol Standard	Symbol Alternate	6226A-55		6226A-70		6226A-100		Unit	Notes
			Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	55	—	70	—	100	—	ns	2
Write Address Setup Time	t_{AVWL}	t_{WAS}	0	—	0	—	0	—	ns	—
Write Address Valid to End of Write	t_{AVWH}	t_{AW}	35	—	45	—	45	—	ns	—
Write Pulse Width	t_{WLWH}	t_{WP}	35	—	40	—	40	—	ns	—
Write Data Valid to End of Write	t_{DVWH}	t_{DWS}	30	—	35	—	40	—	ns	—
Write Data Hold Time	t_{WDHX}	t_{DWH}	0	—	0	—	0	—	ns	—
Write Enable Time	t_{WLQZ}	t_{WZ}	0	20	0	35	0	35	ns	4
Output High Z after Write Disable	t_{WHQX}	t_{WHZ}	5.0	—	5.0	—	5.0	—	ns	4
Write Address Hold Time	t_{WHAX}	t_{WAH}	5.0	—	5.0	—	5.0	—	ns	—

WRITE CYCLE 1 ($\bar{W}$ Controlled)**TIMING LIMITS****MOTOROLA SC (MEMORY/ASI 65E D**

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, response delays from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device should never provide data later than that time.

WRITE CYCLE 2 ($\bar{E}$ Controlled, See Note 1)

Parameter	Symbol Standard	Symbol Alternate	6226A-25		6226A-30		6226A-35		6226A-45		Unit	Notes
			Min	Max	Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	25	—	30	—	35	—	45	—	ns	2
Chip Select Address Setup Time	t_{AVEL}	t_{CAS}	0	—	0	—	0	—	0	—	ns	—
Chip Enable Address Valid Time	t_{AVEH}	t_{AC}	20	—	20	—	25	—	35	—	ns	—
Chip Enable Write Pulse Width	t_{ELEH}	t_{CW}	20	—	20	—	25	—	35	—	ns	3
Write Start before Chip Disable Time	t_{ELWH}	t_{CWW}	20	—	20	—	25	—	35	—	ns	—
Write Data Valid to End of Chip Enable	t_{DVEH}	t_{DCS}	15	—	15	—	20	—	25	—	ns	—
Write Data Hold Time after Chip Disable	t_{EHDX}	t_{DCH}	0	—	0	—	0	—	0	—	ns	—
Write Address Hold Time after Chip Disable	t_{EHAX}	t_{CAH}	5.0	—	5.0	—	5.0	—	5.0	—	ns	—

NOTES:

1. A write occurs during the overlap of $\bar{E}_1$ low and E_2 high while $\bar{W}$ is preconditioned low.
2. All write cycle timing is referenced from the last valid address to the first transitioning address.
3. $\bar{W}$ remains low when chip enable pulse applies to write memory. Verify memory contents in the next upcoming Read Cycles.

Parameter	Symbol Standard	Symbol Alternate	6226A-55		6226A-70		6226A-100		Unit	Notes
			Min	Max	Min	Max	Min	Max		
Write Cycle Time	t_{AVAV}	t_{WC}	55	—	70	—	100	—	ns	2
Chip Select Address Setup Time	t_{AVEL}	t_{CAS}	0	—	0	—	0	—	ns	—
Chip Enable Address Valid Time	t_{AVEH}	t_{AC}	35	—	45	—	45	—	ns	—
Chip Enable Write Pulse Width	t_{ELEH}	t_{CW}	35	—	40	—	40	—	ns	3
Write Start before Chip Disable Time	t_{ELWH}	t_{CWW}	35	—	45	—	45	—	ns	—
Write Data Valid to End of Chip Enable	t_{DVEH}	t_{DCS}	30	—	35	—	40	—	ns	—
Write Data Hold Time after Chip Disable	t_{EHDX}	t_{DCH}	0	—	0	—	0	—	ns	—
Write Address Hold Time after Chip Disable	t_{EHAX}	t_{CAH}	5.0	—	5.0	—	5.0	—	ns	—

MOTOROLA SC MEMORY/ASI 65E D**WRITE CYCLE 2** ($\bar{E}$ Controlled)