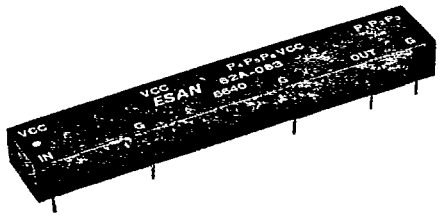
Programmable Delay Line (TTL)

62A Series

• 48 Pin Dip Package • Digitally Programmable in 64 Delay Steps (4 Bits)



PART NO.	ZERO STEP (ns)	MAX. DELAY (ns)	PER STEP (ns)
62A-063	20±2	83	1±0.5
62A-126	20±2	146	2±0.6
62A-189	20±2	209	3±0.7
62A-252	20±2	272	4±0.8
62A-315	20±2	335	5±1.0
62A-378	20±2	398	6±1.2
62A-441	20±2	461	7±1.4
62A-504	20±2	524	8±1.6
62A-567	20±2	587	9±1.8
62A-630	20±2	650	10±2.0

Specifications:

- Operating Temperature : 0°C to 70°C
- Temperature Coefficient : 300 ppm/°C
- Logic 1 Input Voltage : 2V min; 5.5v max
- Logic 1 Input Current : 100μA @ 2.4V, 2mA @5.5V
- Logic 0 Input Voltage : 0.8V max
- Logic 0 Input Current : −4mA max
- Logic 1 Output Voltage : 2.4V min
- Logic 0 Output Voltage : 0.4V max
- Rise Time : 4ns max

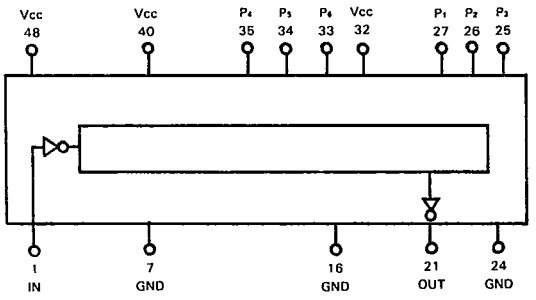
Test Conditions:

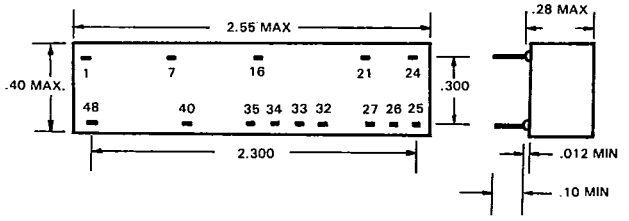
- Vcc = 5.0VDC, Temp. 25°C
- Time delay measured at the 1.5 volt level of the leading edge
- Rise time measured from .75V to 2.4 volts
- Output koaded with 15pf
- Input pulse width: 3 * max time delay
- Pulse amplitude: 3.0 volts
- Pulse spacing: 1000ns

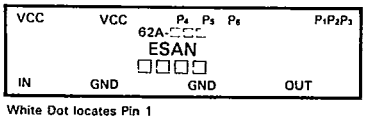
Truth Table

ADDRESS 6	5	4	3	2	1	DELAY OUT
0	0	0	0	0	0	T_0
0	0	0	0	0	1	T_1
0	0	0	0	1	0	T_2
0	0	0	0	1	1	T_3
0	0	0	1	0	0	T_4
0	0	0	1	0	1	T_5
0	0	0	1	1	0	T_6
0	0	0	1	1	1	T_7
0	0	1	0	0	0	T_8
0	0	1	1	1	1	T_{15}
0	1	0	0	0	0	T_{16}
0	1	1	1	1	1	T_{22}
1	0	0	0	0	0	T_{23}
1	1	1	1	1	1	T_{63}

1 = Logic 1 = Logic 1
T_0 = Reference or inherent delay of unit
$T_1 \rightarrow T_{63}$ Multiplier of incremental delay.







White Dot locates Pin 1

Unit: Inch