53/63RS1681/A

2048x8 High Performance
Registered PROM with Synchronous Enable

Advanced Micro Devices

FEATURES/BENEFITS

- **Synchronous output enable**
- **Edge-triggered "D" registers**
- **Versatile 1:16 user programmable initialization words**
- **8-bit-wide in 24-pin SKINNYDIP® for high board density**
- **Simplifies system timing**
- **Faster cycle times**
- **16 mA I_{OL} output drive capability**
- **Reliable titanium-tungsten fuses (TIW), with programming yields typically greater than 98%**

APPLICATIONS

- **Microprogram control store**
- **State sequencers**
- **Next address generation**
- **Mapping PROM**
- **Programmable Logic Element (PLE™) 11 inputs, 8 Registered Outputs, 2048 product terms**

GENERAL DESCRIPTION

The 53/63RS1681 and 53/63RS1681A are 2Kx8 PROMS with on-chip "D" type registers, versatile output enable control through synchronous enable inputs and flexible start up sequencing through programmable initialization words.

Data is transferred into the output registers on the rising edge of the clock. Provided that the synchronous ($\overline{ES}$) enable is low, the data will appear at the outputs. Prior to the positive clock edge, register data are not affected by changes in addressing or synchronous enable inputs.

Memory expansion and data control is made flexible with synchronous enable inputs. Outputs may be set to the high impedance state by setting $\overline{ES}$ HIGH before the rising clock edge occurs. When V_{CC} power is first applied the synchronous enable flip-flop will be in the set condition causing the outputs to be in the high impedance state.

The flexible initialization feature allows start up and time out sequencing with 1:16 programmable words to be loaded into the output registers. With the synchronous INITIALIZE ($\overline{IS}$) pin LOW, one of the 16 column words (A3–A0) will be set in the output registers independent of the row addresses (A10–A4). With all $\overline{IS}$ column words (A3–A0) programmed to the same pattern, the $\overline{IS}$ function will be independent of both row and column addressing and may be used as a single pin control. With all $\overline{IS}$ words programmed HIGH a PRESET function is performed. The unprogrammed state of $\overline{IS}$ words are LOW, presenting a CLEAR with $\overline{IS}$ pin LOW.

SELECTION GUIDE

Memory		Package		Performance	Part Number	
Size	Organization	Pins	Type		0°C to +75°C	–55°C to +125°C
16K	2048x8	24 (28)	CD 3024 PD 3024 PL 028 CL 028 CFM 024	Enhanced	63RS1681A	53RS1681A
				Standard	63RS1681	53RS1681

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PLE™ is a trademark of Advanced Micro Devices

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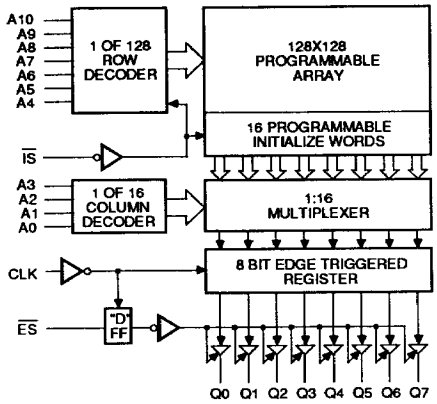
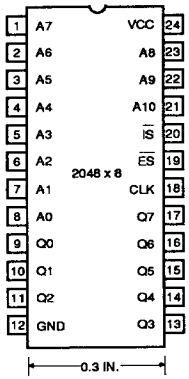
BLOCK DIAGRAM



PIN CONFIGURATIONS



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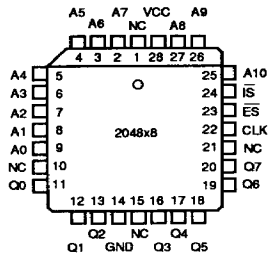

Plastic Chip Carrier

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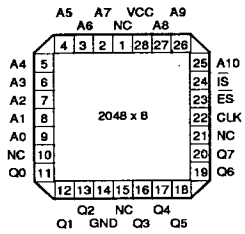

Leadless Chip Carrier

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ABSOLUTE MAXIMUM RATINGS

	Operating	Programing
Supply voltage V_{CC}	−0.5 V to 7 V	12 V
Input voltage	−1.5 V to 7 V	7 V
Input current	−30 mA to +5 mA	
Off-state output voltage	−0.5 V to 5.5 V	12 V
Storage temperature	−65°C to +150°C	

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods of time may affect reliability. Absolute Maximum Ratings are for system design reference; parameters given are not tested.

Operating Conditions

Symbol	Parameter	Typ†	Military †				Commercial				Unit
			53RS1681A		53RS1681		63RS1681A		63RS1681		
			Min	Max	Min	Max	Min	Max	Min	Max	
t_w	Width of clock (high or low)	10	20		20		20		20		ns
$t_{s(A)}$	Setup time from address to clock	28	40		45		35		40		ns
$t_{s(\overline{ES})}$	Setup time from $\overline{ES}$ to clock	7	15		15		15		15		ns
$t_{s(\overline{IS})}$	Setup time from $\overline{IS}$ to clock	20	30		35		25		30		ns
$t_{h(A)}$	Hold time address to clock	−5	0		0		0		0		ns
$t_{h(\overline{ES})}$	Hold time ($\overline{ES}$)	−3	5		5		5		5		ns
$t_{h(\overline{IS})}$	Hold time ($\overline{IS}$)	−5	0		0		0		0		ns
V_{CC}	Supply voltage	5	4.5	5.5	4.5	5.5	4.75	5.25	4.75	5.25	V
T_A	Operating temperature*	25	−55	125	−55	125	0	75	0	75	°C

* *This is defined as the instant-on case temperature*

† *Military burn-in is in accordance with the current revision of MIL-STD-883, Test Method 1015, Conditions A through E. Test conditions are selected at AMD's option.*

Electrical Characteristics Over Operating Conditions. For APL Products, Group A, Subgroups 1, 2, 3 are tested unless otherwise noted.

Symbol	Parameter	Test Conditions			Min	Typ†	Max	Unit
V_{IL}	Low-level input voltage**						0.8	V
V_{IH}	High-level input voltage**				2.0			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = –18 mA				–1.2	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.4 V				–0.25	mA
I_{IH}	High level input current	V_{CC} = MAX	V_I = V_{CC} MAX				40	µA
V_{OL}	Low-level output voltage	V_{CC} = MIN	I_{OL} = 16 mA				0.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN	Com	I_{OH} = –3.2 mA	2.4			V
			Mil	I_{OH} = –2 mA				
I_{OZL}	Off-state output current	V_{CC} = MAX	V_O = 0.4 V				–40	µA
I_{OZH}			V_O = 2.4 V				40	
I_{OS}	Output short-circuit current*	V_{CC} = 5V	V_O = 0 V		–20		–90	mA
I_{CC}	Supply current	V_{CC} = MAX. All inputs TTL. All outputs open.				140	185	mA

Switching Characteristics Over Operating Conditions and Using Standard Test Load. For APL Products, Group A, Subgroups 9, 10, 11 are tested unless otherwise noted.††

Symbol	Parameter	Typ†	Military				Commercial				Unit
			53RS1681A		53RS1681		63RS1681A		63RS1681		
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{CLK}	Clock to output delay	10		20		25		15		20	ns
t_{ESA}	Clock to output access time (ES)	15		30		35		25		30	ns
t_{ESR}	Clock to output recovery time (ES)	15		30		35		25		30	ns

* *Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.*

** *V_{IL} and V_{IH} are input conditions of output tests and are not themselves directly tested. V_{IL} and V_{IH} are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.*

† *Typicals at 5.0 V V_{CC} and 25°C T_A.*

†† *Subgroups 7 and 8 apply to Functional tests.*

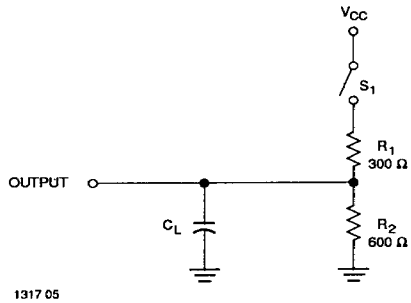

Figure 1. Switching Test Load

WAVEFORM	INPUTS	OUTPUTS
	DON'T CARE: CHANGE PERMITTED	CHANGING: STATE UNKNOWN
	NOT APPLICABLE	CENTER LINE IS HIGH IMPEDANCE STATE
	MUST BE STEADY	WILL BE STEADY

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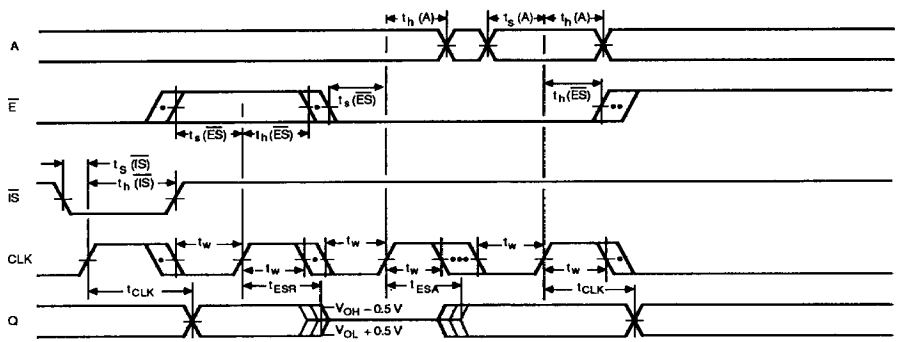
Figure 2. Definition of Timing Diagrams



NOTES:
1. INPUT PULSE AMPLITUDE 0 V TO 3.0 V.
2. INPUT RISE AND FALL TIMES 2–5 ns FROM 0.8 V TO 2.0 V.
3. INPUT ACCESS MEASURED AT THE 1.5 V LEVEL.
4. SWITCH S_1 CLOSED, C_L = 30 pF AND MEASURED AT 1.5 V OUTPUT LEVEL FOR ALL TESTS EXCEPT t_{ESA} AND t_{ESR}.
5. t_{ESA} IS MEASURED AT THE 1.5 V OUTPUT LEVEL WITH C_L = 30 pF. S_1 IS OPEN FOR HIGH IMPEDANCE TO "1" TEST, AND CLOSED FOR HIGH IMPEDANCE TO "0" TEST.

   t_{ESR} IS TESTED WITH C_L = 5 pF. S_1 IS OPEN FOR "1" TO HIGH IMPEDANCE TEST, MEASURED AT V_{OH} – 0.5 V OUTPUT LEVEL; S_1 IS CLOSED FOR "0" TO HIGH IMPEDANCE TEST, MEASURED AT V_{OL} + 0.5 V OUTPUT LEVEL.

Figure 3. Definition of Waveforms