FOUR (60 Hz) DIGITAL to SYNCHRO/RESOLVER CONVERTERS (1.2 VA)
TWO-SPEED or SINGLE-SPEED or COMBINATION (PROGRAMMABLE)
16 BIT RESOLUTION; WRAP-AROUND SELF TEST, PROGRAMMABLE ROTATION
TO COMMERCIAL OR MILITARY SPECIFICATIONS

FEATURES:
- 16-bit resolution
- 2 arc-minutes accuracy at full-load
- 4 and 2-channel versions
- Programmable 2-speed ratios (2 to 255) and angle rotation
- Continuous background BIT testing with Reference and Signal loss detection
- Power-On Self-Test (POST)
- Outputs can be turned ON/OFF
- Transformer isolated
- Watchdog timer and soft reset
- Either A32, A24 or A16 address
- Geographical Addressing
- I/O via front panel, P2, or both
- No adjustments or trimming required
- Part Number, S/N, Date Code, & Revision in permanent memory

DESCRIPTION:

This high density intelligent DSP-based VME card incorporates four separate transformer isolated Digital-to-Synchro converters with 1.2 VA drive capability, wrap-around self-test, and signal/reference loss detection. Either one common or four separate reference inputs can be specified. This card offers two-speed configuration and constant rotation that includes a start and a stop angle. Transformer isolation enables user to ground one of the outputs without effecting performance. External amplifiers, to handle 30 VA from 50 Hz to 400 Hz, can seamlessly be integrated. If Geographical Addressing is part of the overall system, this card will respond, otherwise the board DIP switches will be activated to set base address. A watchdog timer is provided to monitor the processor. This model will drive passive loads such as CT's etc. A green LED is provided on front panel "F" models only, to visually indicate proper card performance. Analog outputs can be specified either via P2, front panel or both. Part #, S/N, Date Code, and Revision are located in permanent memory locations.

Major diagnostics are incorporated to offer substantial improvements to system reliability, because the user is alerted (within 5 seconds) to channel malfunctions. This approach reduces bus traffic, because the Status Registers do not require constant polling. See Programming Instructions for further details.

The D2 Test initiates automatic background BIT testing that compares the output of each channel against the commanded input to a test accuracy of 0.05° and monitors each Output and Reference. A failure triggers an Interrupt (if enabled) and results are available in Status Registers. The testing is totally transparent to the user, requires no external programming, has no effect on the standard operation of this card and can be enabled or disabled via the bus.

The D3 Test starts a BIT test that generates and tests 72 different angles, to a testing accuracy of 0.05°. Results can be read from Status Registers. External reference is required. Testing requires no external programming, and can be Initiated or terminated via the bus. CAUTION: Outputs are active during this test. Check connected loads for possible interaction.

Power-On Self-Test (POST), if enabled, initiates the D3 Test upon turn-on and is enabled/disabled via the bus.

The "C" version operates from 0°C to +70°C and is populated with standard high quality commercial semiconductors. The "M" version, used for severe environmental conditions, operates from -55°C to +85°C and is populated with high quality extended temperature semiconductors. Conduction cooling, using a thermal plane and wedge locks, can be specified. A stiffener improves vibration response. Both sides of the board can be conformally coated. All “M” boards are burned in for 24 hours and cycled from -55°C to +85°C.

SPECIFICATIONS (applies to each channel)

Resolution:	16 bits (.0055°)
Accuracy:	±2 arc-minutes, no load to full load
Output format:	(See part number), transformer isolated
Output voltage:	90 V_{L-L}
Output load:	1.2 VA max./Channel. Short circuit protected (5000 Ω reactive at 90 V_{L-L} Synchro).
Regulation:	5% max, no load to Full load
Ratio:	Set any ratio between 2 and 255
Rotation:	Continuous rotation or programmable Start and Stop angles. 0 to ±13.6 RPS with a resolution of 0.15°/sec. Step size is 16 bits (0.0055)° up to 1.5 RPS, then linearly increases to 12 bits (0.088°) at 13.6 RPS
Reference input voltage:	115 Vrms, 60 Hz or 400 Hz, transformer isolated.
Reference current:	1 ma max./Channel
Phase shift:	5° max. between output and reference.
Settling time:	Less than 100 micro seconds
VME Data transfer:	Data transfers within 200 ns
Interrupts:	Interface implements a single Interrupt capability. One of seven priority lines can be selected.
Power (From P1):	+ 5 VDC at 0.4 A ±12 VDC at .8 A average, 2 A peak (for 4 channels). Power supplies must be able to supply peak power without current limiting..
Temperature, operating:	"C" =0°C to +70°C; "M" =-55°C to +85°C (see part number)
Temperature, storage:	-55°C to +105°C
Size:	6U (9.2") height, 8HP (1.6") width. 233.4 mm x 40.6 mm x 160 mm deep

PROGRAMMING INSTRUCTIONS:

I/O CONFIGURATION:

The VMEbus interface will respond to A32:D16, A24:D16 and A16:D16 DTB cycles.

A32 mode: Unit responds to address modifiers 0A, 0D, 0E and 09. Base address can be set anywhere in the 4 Gigabyte address space on 256 byte boundaries.

A24 mode: Responds to address modifiers 3A, 3D, 3E and 39. Base address can be set anywhere in the 16 Megabyte address space on 256 byte boundaries.

A16 mode: Responds to address modifiers 2A, 2D, 2E and 29. Base address can be set anywhere in the 64 K byte address space on 256 byte boundaries.

Geographical Addressing: When Geographical Addressing is enabled (see Part Number), the card will respond to address modifier 2Fh for A24 Address mode, where the 5 MSBs of the A24 address are the 5 bits defined by the slot in VME back plane. The Card can optionally be interrogated at 2Fh to determine resource requirements and available functionally. Using address modifier 2Fh, the following need to be written to the card:

1) the base address the card should respond to
2) the address modifier (A16, A24, A32)
3) then enable the card.

For example : If the card is in slot # 10 the 5 MSBs are 01010 so the address of the CSR Registers are :
0101 0 111 1111 1111 xxxx xxxx or 57FFxx h (xx is CSR Register offset)

Write to address 57FF63 h, the A31 – A24 base address bits , for example 01h
Write to address 57FF67 h, the A23 – A16 base address bits, for example 02h
Write to address 57FF6B h, the A15 – A8 base address bits, for example 04h
Write to address 57FF6F h, the address modifier you wish to respond to shifted up 2 bits , for example 28h(0A<< 2)
Then Write to address 57FFFBh , 10h to enable the card.
The card will now respond to the base address (010204 in the example) and address modifier (0A in example) programmed. The base address and address modifier can be changed at any time.

ADDRESS = BASE + OFFSET

00	Ch.1	write	1E	Test (D2) verify	read/write	52	Stop angle Ch.2	read/write	80	Ratio, Ch.1/2	read/write
02	Ch 2	write	20	Interrupt Level	read/write	54	Stop angle Ch.3	read/write	82	Ratio, Ch.3/4	read/write
04	Ch.3	write	22	Interrupt vector	read/write	56	Stop angle Ch.4	read/write	88	Status, Ext. amp.	read
06	Ch.4	write	28	Active channels	read/write	60	Rotation rate Ch.1	read/write	90	Outputs ON/OFF	read/write
10	Status, Signal	read	2C	Save	read/write	62	Rotation rate Ch.2	read/write	92	External / Internal	read write
12	Status, Reference	read	2E	Test enable	read/write	64	Rotation rate Ch.3	read/write	94	Power-on POST test	read/write
14	Status, Test	read	30	Wrap-around Ch. 1	read	66	Rotation rate Ch.4	read/write	9A	Watchdog timer	read/write
16	Part number	read	32	Wrap-around Ch. 2	read	70	Rotation, Mode	read/write	9C	Soft reset	write
18	Serial number	read	34	Wrap-around Ch. 3	read	72	Rotation, Initiate,	write			
1A	Date code	read	36	Wrap-around Ch. 4	read	74	Rotation, Stop	write			
1C	Rev level	read	50	Stop angle Ch.1	read/write	76	Rotation completed	read			

	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Data	180	90	45	22.5	11.25	5.625	2.813	1.406	.703	.352	.176	.088	.044	.022	.011	.0055
Outputs, ON/OFF	Ch.1	Ch.2	Ch.3	Ch.4	X	X	X	X	X	X	X	X	X	X	X	X
Test Enable	X	X	X	X	X	X	X	X	X	X	X	X	D3	D2	X	X
Rotation, Mode	Ch.1	Ch.2	Ch.3	Ch.4	X	X	X	X	X	X	X	X	X	X	X	X
Rotation, INITIATE	Ch.1	Ch.2	Ch.3	Ch.4	X	X	X	X	X	X	X	X	X	X	X	X
Rotation, STOP	Ch.1	Ch.2	Ch.3	Ch.4	X	X	X	X	X	X	X	X	X	X	X	X
Rotation completed	Ch.1	Ch.2	Ch.3	Ch.4	X	X	X	X	X	X	X	X	X	X	X	X
Active channels	Ch.1	Ch.2	Ch.3	Ch.4	X	X	X	X	X	X	X	X	X	X	X	X
Status, Reference	Ch.1	Ch.2	Ch.3	Ch.4	X	X	X	X	X	X	X	X	X	X	X	X
Status, Signal	Ch.1	Ch.2	Ch.3	Ch.4	X	X	X	X	X	X	X	X	X	X	X	X
Status, Test	Ch.1	Ch.2	Ch.3	Ch.4	X	X	X	X	X	X	X	X	X	X	X	X
External/Internal	Ch.1	Ch.2	Ch.3	Ch.4	X	X	X	X	X	X	X	X	X	X	X	X
Status, Ext. amp.	Ch.1	Ch.2	Ch.3	Ch.4	X	X	X	X	X	X	X	X	X	X	X	X

At **Power-On** or **System Reset**, all parameters are restored to last saved setup, and if POST is enabled**,** a D3 Test is initiated.

Enter Active Channels: Set the bit, corresponding to each channel to be monitored during BIT testing, in the Active Channel Register at 28h. “1”=active; “0”=not used. Omitting this step will produce false alarms because unused channels will set faults.

Save Setup: The current setup can be saved by writing 5555h to the Save Register at 2Ch. This location will automatically clear to 0000h when the save is completed (within 5 seconds). When save is elected, all parameters are saved, however, any parameter can be changed at will. Saving is optional. If not saved, reenter parameters at each power up.

To restore factory shipped parameters, write AAAAh to the Save Register at 2Ch followed by System Reset. Note: After a SAVE or RESTORE, poll 2Ch and do not perform any other operation until word is at "0".

Enter Interrupt Levels into 20h as an 16-bit binary number. 0= no interrupt; 1-7 indicates priority levels.

Any error will latch Status Register and trigger an Interrupt. When Interrupt is acknowledged, additional errors will set another Interrupt. Reading will unlatch registers. Now, let us consider what happens when a status bit changes before registers are read For example, if a reference loss was detected and latched into registers and subsequent scans find that the reference was reconnected, then this status change will be held in background until registers are read. Within 250ms registers will be updated with the background data.

Interrupt Vector: Write 16-bit word (0-255) to Interrupt Vector register at 22h.

Write Angle: For single-speed applications (Ratio=1), write 16-bit binary data (or 16-bit 2’s compliment data) to address 0000h for Ch.1; to 02h for Ch.2 etc. For two-speed applications, write only to first channel of channel pair (Coarse speed), card will set angle of second channel (fine speed), to the Coarse angle multiplied by the ratio. Note: writing to input angle registers will stop any rotation operation in effect, on that channel

Ratio: Enter the desired ratio, as a binary number, in the Ratio Register corresponding to the pair of channels to be used as a two-speed channel. Example: Single speed = 1; 36:1 = 100100.

ON/OFF: Set the bit, corresponding to each channel to be turned on, to "1" in Outputs On/Off Register at 90h. To turn OFF a channel set corresponding bit to "0". Default is OFF.

Read Wrap-around Angles: Read addresses 30h to 3Eh. AVAILABLE AT ALL TIMES.

Rotation Rate: Write to the corresponding Rotation Rate Register a 2's compliment number representing the desired rotation rate, LSB = 0.15°/sec.
Ex: 12 RPS =. (12 x 360°/0.15° = 28800 = 7080h), -12 RPS = (-12 x 360°/0.15° = -28800 = 8F80h)
Step size is 16 bits (0.0055°) for up to 1.5 RPS, then linearly increases to 12 bits (0.088°) at 13.6 RPS.

Rotation Mode, Continuous or Start/Stop: For continuous rotation, set the corresponding channel bits to "1" in the Rotation Mode Register at 70h. For rotation to cease at a designated stop angle, set the bit to "0".

Write Stop Angles: Write 16-bit binary data to appropriate address (50h to 5Eh). After a channel reaches the stop angle it will stop rotating, and remain at that angle until a new input angle is set. If rotation is initiated again the angle will start rotating again, from the present angle.

Initiate Rotation: First set the Rotation Rate Registers, and Rotation Mode Register, for each channel that is to rotate. Then set the corresponding bit for each channel to start rotating, to a "1", in the Rotation Initiate Register at 72h. This will initiate rotation of each channel (that have their corresponding bit set to "1") at the same time.

Stop Rotation: Set the corresponding bit for each channel to be stopped, to a "1", in the Rotation Stop Register at 74h. Channel will remain at the stopped angle until new input angles are set, or rotation is again initiated.

Rotation Completed: Read Rotation Completed Register at 76h. Each bit corresponds to a given channel, "1"=rotation completed, "0"=rotation in process.

D2 Test Enable : Writing "1" to D2 of Test Enable Register at 2Eh initiates automatic background BIT testing that checks the output accuracy of each channel, by comparing the measured output angle, before the output transformer, to the commanded angle, and monitors each Reference and Signal. An Interrupt (if enabled) will be set to indicate an accuracy problem or Signal/Reference loss and the results can be read from Status Registers within 2 seconds. A "0" deactivates this test. The testing is totally transparent to the user, requires no external programming, has no effect on the standard operation of this card and can be enabled or disabled via the bus. Card will write 55h (every 2 seconds) to D2 Test Verify Register at 1Eh when D2 is enabled. User can periodically clear to 00h and then read 1Eh again, after 2 seconds, to verify that BIT testing is activated. This test continuously sequences between the eight channels on the card with each output being measured for approx. 180 mSec. If the measured angle has an error greater the 0.05º (0.1º for external amplifiers), a flag will be set in the appropriate register. If the input angle is stepped more then 0.05º during a test cycle, the test cycle will not generally indicate an error.

D3 Test Enable : Writing "1" to D3 of Test Enable Register at 2Eh initiates a BIT test that generates and tests 72 different angles to a test accuracy of 0.05°. External reference is required. An Interrupt (if enabled) will be set to indicate an accuracy problem or Signal or Reference loss. Results are available in Status Registers. Test cycle takes about 30 seconds and D3 changes from "1" to "0" when test is complete. The testing requires no external programming, and can be initiated or terminated via the bus. CAUTION: Outputs must be ON during this test and are therefore active. Check connected loads for possible interaction.

Power-On Self-Test (POST) will initiate the D3 Test on Power-On, if POST is enabled and saved. Enable by writing "1" or Disable by writing "0" to POST Register at 94h and then Save Setup.

Status, Test: Check the corresponding bit of the Test Status Register at 14h, for status of BIT testing for each active channel. A "1" =Accuracy OK; "0" =failed (test cycle takes 2 seconds for accuracy error).

Status, Ref: Check the corresponding bit of the Ref Status Register at 12h, for status of the reference input for each active channel. A "1" =Ref. ON, "0" = Ref. Loss (Reference loss is detected after 2 seconds).

Status, Sig: Check the corresponding bit of the Sig Status Register at 10h, for status of the input signals for each active channel. A "1" = Signal ON, "0" = Signal loss (Signal loss is detected after 2 seconds).

Status, Ext. Amp: Check the corresponding bit of the Ext Amp Status Register at 88h, for status of BIT testing for each active channel that has the External Amp enabled. A "1"= Accuracy OK; "0" =failed.

External/Internal: When wrap-around BIT test capability is required for external Synchro amplifiers, set the bit, corresponding to each channel that has an external amplifier to be monitored, to "1" in the External/Internal Register at 92h. Default is Internal.

Soft Reset (Level sensitive): Writing "1" to 9Ch initiates and holds software reset state. Then, writing "0" initiates reboot (takes 400 ms). Power-On or a hardware RESET, sets 'reset' bit, at 9Ch to "0".

Watchdog Timer: This feature monitors the watchdog timer register at 9Ah. When it detects that a code has been received, that code will be inverted within 100 µSec. The inverted code stays in the register until replaced by a new code. User, after 100 µSec. should look for the inverted code to confirm that the processor is operating.

Serial Number: At 18h, is read as a 16-bit binary word.

Date Code: Read as a decimal number at 1Ah. The four digits represent YYWW (Year,Year,Week.Week).

Rev: At 1Ch.
Example

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	0	1	1	0	0	0	0	1	1	0	0	0	1
DSP Rev 1.1						FPGA Rev 3						PC Rev 1			

Front panel Connectors:

J1: DC37P; Mate: DC37S

Pin	Ch.1	Pin	Ch.2	Pin	Ch.3	Pin	Ch.4
37	S1	34	S1	31	S1	28	S1
36	S2	33	S2	30	S2	27	S2
19	S3	16	S3	13	S3	10	S3
18	S4	15	S4	12	S4	9	S4
35	RHi	32	∗RHi	29	∗RHi	26	∗RHi
17	RLo	14	∗RLo	11	∗RLo	8	∗RLo
1	Chassis						

J2: DC37P; Mate: DC37S

Pin	Ext. amp	Pin	Ext. amp	Pin	Ext. amp
1	Sine Hi Ch.1	21	Common	13	Sine Hi Ch.4
2	Common	22	Cos Hi Ch.2	14	Common
20	Cos Hi Ch.1	4	Sine Hi Ch.3	32	Cos Hi Ch.4
3	Sine Hi Ch.2	5	Common		
37	Chassis	23	Cos Hi Ch.3		

P2 Connector: 160 pin

Pin	Designation	Pin	Designation	Pin	Designation	Pin	Designation	Pin	Designation	Pin	Designation
18c	S1 Ch. 1	32c	S3 Ch. 3	28c	∗RHi Ch. 2	4d	Common	13d	Common	15z	On/Off Lo Ch.4
22c	S3 Ch. 1	26c	S2 Ch. 3	30c	∗RLo Ch. 2	5d	Cos Hi Ch.1	14d	Cos Hi Ch.4	1a	BIT Hi Ch. 1
20c	S2 Ch. 1	31c	S4 Ch. 3	31a	∗RHi Ch. 3	6d	Sine Hi Ch.2	1z	On/Off Hi Ch.1	2a	BIT Lo Ch. 1
24c	S4 Ch. 1	18a	S1 Ch. 4	32a	∗RLo Ch. 3	7d	Common	3z	On/Off Lo Ch.1	3a	BIT Hi Ch. 2
10c	S1 Ch. 2	22a	S3 Ch. 4	30a	∗RHi Ch. 4	8d	Cos Hi Ch.2	5z	On/Off Hi Ch.2	4a	BIT Lo Ch. 2
14c	S3 Ch. 2	20a	S2 Ch. 4	29a	∗RLo Ch. 4	9d	Sine Hi Ch.3	7z	On/Off Lo Ch.2	5a	BIT Hi Ch. 3
12c	S2 Ch. 2	24a	S4 Ch. 4	28a		10d	Common	9z	On/Off Hi Ch.3	5c	BIT Lo Ch. 3
16c	S4 Ch. 2	29c	RHi Ch. 1	27a		11d	Cos Hi Ch.3	11z	On/Off Lo Ch.3	6a	BIT Hi Ch. 4
25c	S1 Ch. 3	27c	RLo Ch. 1	3d	Sine Hi Ch.1	12d	Sine Hi Ch.4	13z	On/Off Hi Ch.4	6c	BIT Lo Ch. 4

S4 pins used only with Resolvers. BIT inputs are used for external amplifiers. Do not connect to any undesignated pins.

∗ These inputs are supplied only as individual reference inputs when specified in the part number. Normally, all references are common and brought in on pins 17&35 or 29c&27c respectively.

NOTE: P2 is ALWAYS active

The board contains two green LED's that are for factory use only. Two miniature test connectors, are used to download programming data. Do not interface to these two connectors unless factory instructed to be used for field modification.

PART NUMBER DESIGNATION

64DS2 - X X X X X X - 00

TOTAL NUMBER OF CHANNELS
2 = 2 D/S Channels
4 = 4 D/S Channels

ENVIRONMENTAL
C = 0°C to +70°C
M = -55°C to +85°C
H = M With Removable Conformal Coating
J = M With Permanent Conformal Coating
K = C With Removable Conformal Coating

FORMAT
S = Synchro

MECHANICAL
F = Front Panel I/O and P2 I/O
P = P2 I/O Only
W = P With Wedgelocks
V = VME64 Front Panel I/O

REFERENCE INPUTS
1 = One Common Reference Input
2 = Individual Reference Inputs

OPTIONS
0 = None
1 = Geographical Addressing Enabled
9 = Custom Design (See Separate Spec)

CODE