



COMMODORE SEMICONDUCTOR GROUP

a division of Commodore Business Machines, Inc.
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HMOS

6510 MICROPROCESSOR WITH I/O

DESCRIPTION

The 6510 is a low-cost microprocessor capable of solving a broad range of small-systems and peripheral-control problems at minimum cost to the user.

An 8-bit Bi-Directional I/O Port is located on-chip with the Output Register at Address 0001 and the Data-Direction Register at Address 0000. The I/O Port is bit-by-bit programmable.

The Three-State sixteen-bit Address Bus allows Direct Memory Accessing (DMA) and multi-processor systems sharing a common memory.

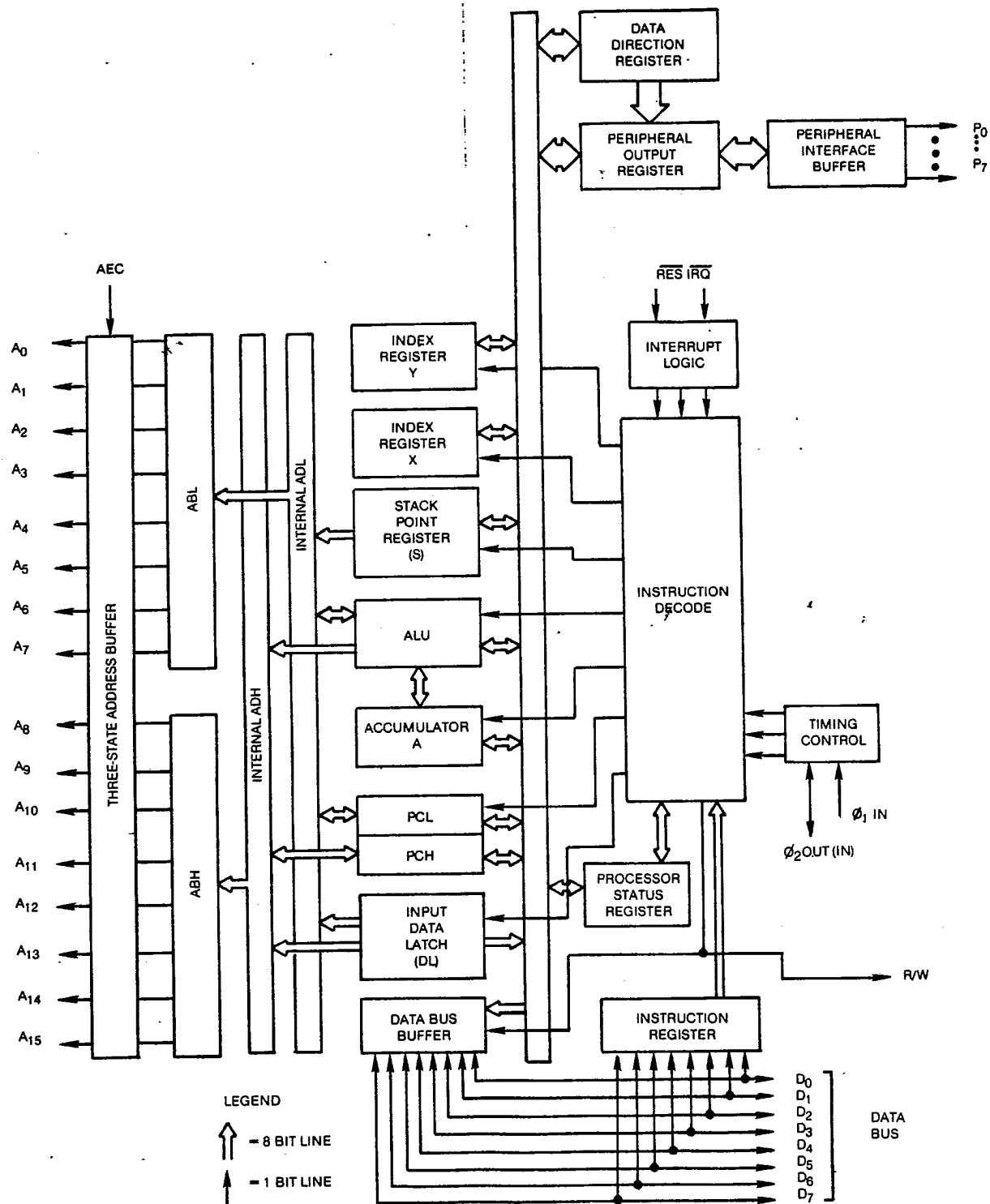
The internal processor architecture is identical to the Commodore Semiconductor Group 6502 to provide software compatibility.

FEATURES OF THE 6510 . . .

- 8-Bit Bi-Directional I/O Port
- Single +5 volt supply
- HMOS, silicon gate, depletion load technology
- Eight bit parallel processing
- 56 Instructions
- Decimal and binary arithmetic
- Thirteen addressing modes
- True indexing capability
- Programmable stack pointer
- Variable length stack
- Interrupt capability
- 8 Bit Bi-Directional Data Bus
- Addressable memory range of up to 65K bytes
- Direct memory access capability
- Bus compatible with M6800
- Pipeline architecture
- 1 MHz, 2MHz and 3 MHz operation
- Use with any type or speed memory
- 4 MHz operation availability expected in 1986.
- Also available in two phase clock input format.

PIN CONFIGURATION

RES	1	40	ϕ_2 OUT
ϕ_1 IN	2	39	R/W
\overline{IRQ}	3	38	DB ₀
AEC	4	37	DB ₁
VCC	5	36	DB ₂
A ₀	6	35	DB ₃
A ₁	7	34	DB ₄
A ₂	8	33	DB ₅
A ₃	9	32	DB ₆
A ₄	10	31	DB ₇
A ₅	11	30	P ₀
A ₆	12	29	P ₁
A ₇	13	28	P ₂
A ₈	14	27	P ₃
A ₉	15	26	P ₄
A ₁₀	16	25	P ₅
A ₁₁	17	24	P ₆
A ₁₂	18	23	P ₇
A ₁₃	19	22	A ₁₃
VSS	20	21	A ₁₄



6510 CHARACTERISTICS

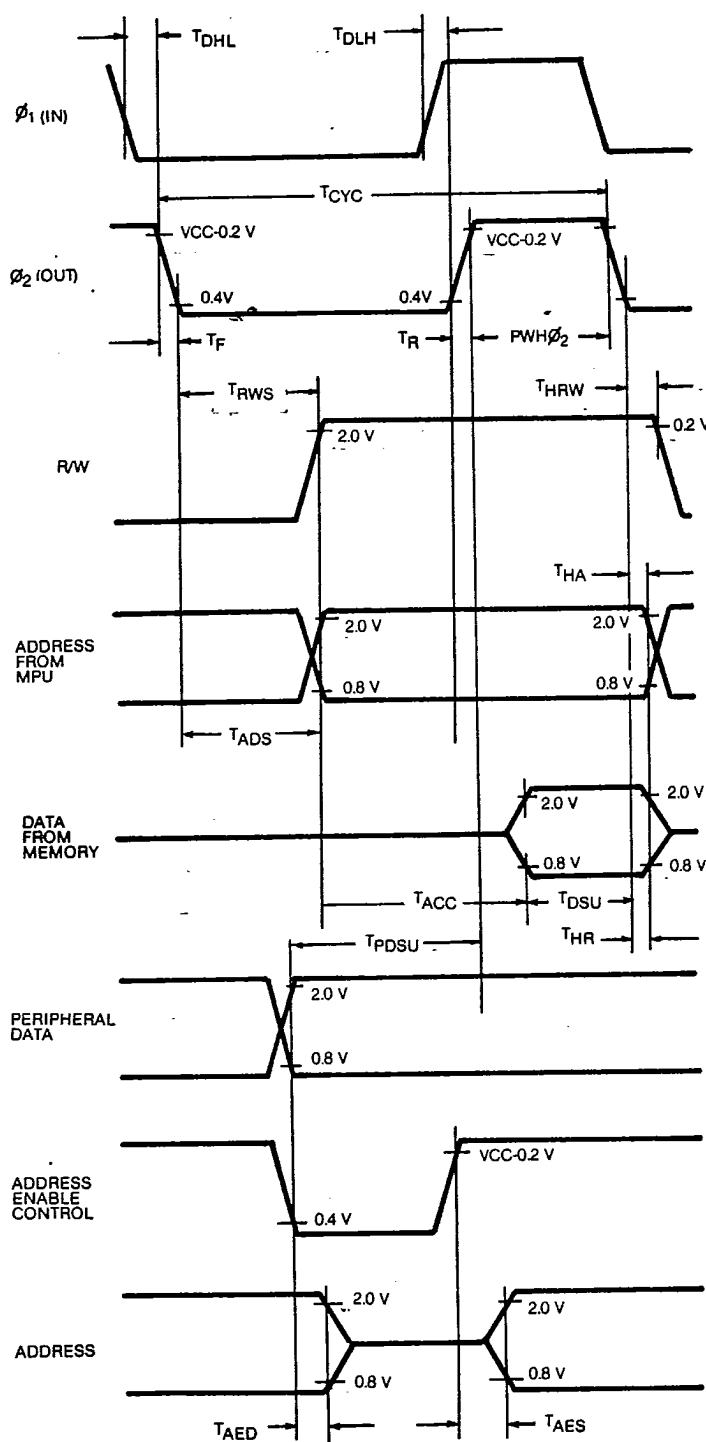
MAXIMUM RATINGS

RATING	SYMBOL	VALUE	UNIT
SUPPLY VOLTAGE	V_{CC}	-0.3 to +7.0	Vdc
INPUT VOLTAGE	V_{in}	-0.3 to +7.0	Vdc
OPERATING TEMPERATURE	T_A	0 to +70	°C
STORAGE TEMPERATURE	T_{STG}	-55 to +150	°C

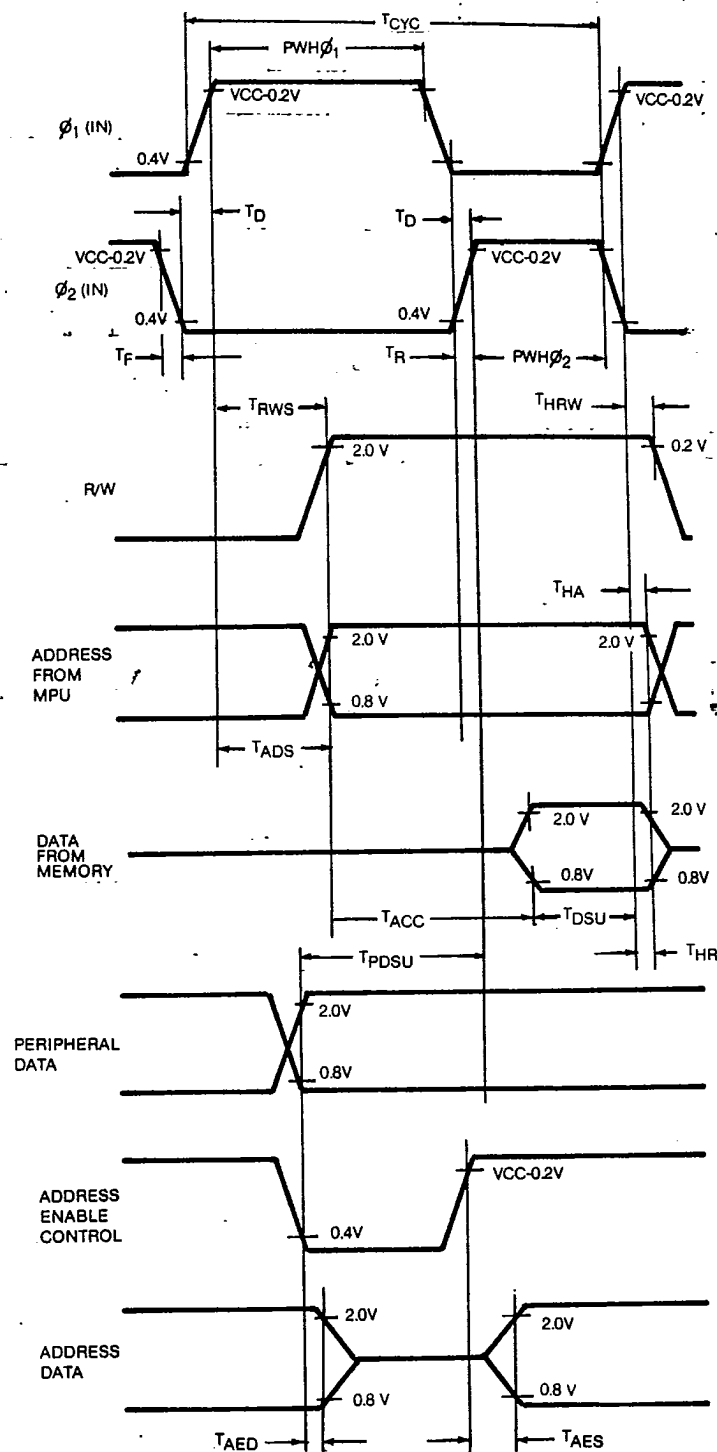
This device contains input protection against damage due to high static voltages or electric fields; however, precautions should be taken to avoid application of voltages higher than the maximum rating.

ELECTRICAL CHARACTERISTICS ($V_{CC} = 5.0V \pm 5\%$, $V_{SS} = 0$, $T_A = 0^\circ$ to $+70^\circ C$)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNIT
Input High Voltage $\phi_1, \phi_2(in)$	V_{IH}	$V_{CC} - 0.2$	—	$V_{CC} + 1.0V$	Vdc
Input High Voltage $\overline{RES}, P_0-P_7, \overline{IRQ}, Data$		$V_{SS} + 2.0$	—	—	Vdc
Input Low Voltage $\phi_1, \phi_2(in)$	V_{IL}	$V_{SS} - 0.3$	—	$V_{SS} + 0.2$	Vdc
$\overline{RES}, P_0-P_7, \overline{IRQ}, Data$		—	—	$V_{SS} + 0.8$	Vdc
Input Leakage Current ($V_{in} = 0$ to $5.25V$, $V_{CC} = 5.25V$) Logic	I_{in}	—	—	2.5	μA
$\phi_1, \phi_2(in)$		—	—	100	μA
Three State (Off State) Input Current ($V_{in} = 0.4$ to $2.4V$, $V_{CC} = 5.25V$) Data Lines	$ITSI$	—	—	10	μA
Output High Voltage ($I_{OH} = -100\mu A$, $V_{CC} = 4.75V$) Data, A0-A15, R/W, P_0-P_7	V_{OH}	$V_{SS} + 2.4$	—	—	Vdc
Output Low Voltage ($I_{OL} = 1.6mA$, $V_{CC} = 4.75V$) Data, A0-A15, R/W, P_0-P_7	V_{OL}	—	—	$V_{SS} + 0.5$	Vdc
Power Supply Current	ICC	—	—	130	mA
Capacitance $V_{in} = 0$, $T_A = 25^\circ C$, $f = 1MHz$) Logic, P_0-P_7	C				pF
	C_{in}	—	—	10	
Data		—	—	15	
A0-A15, R/W	C_{out}	—	—	12	
ϕ_1	C_{ϕ_1}	—	30	50	
ϕ_2	C_{ϕ_2}	—	50	80	

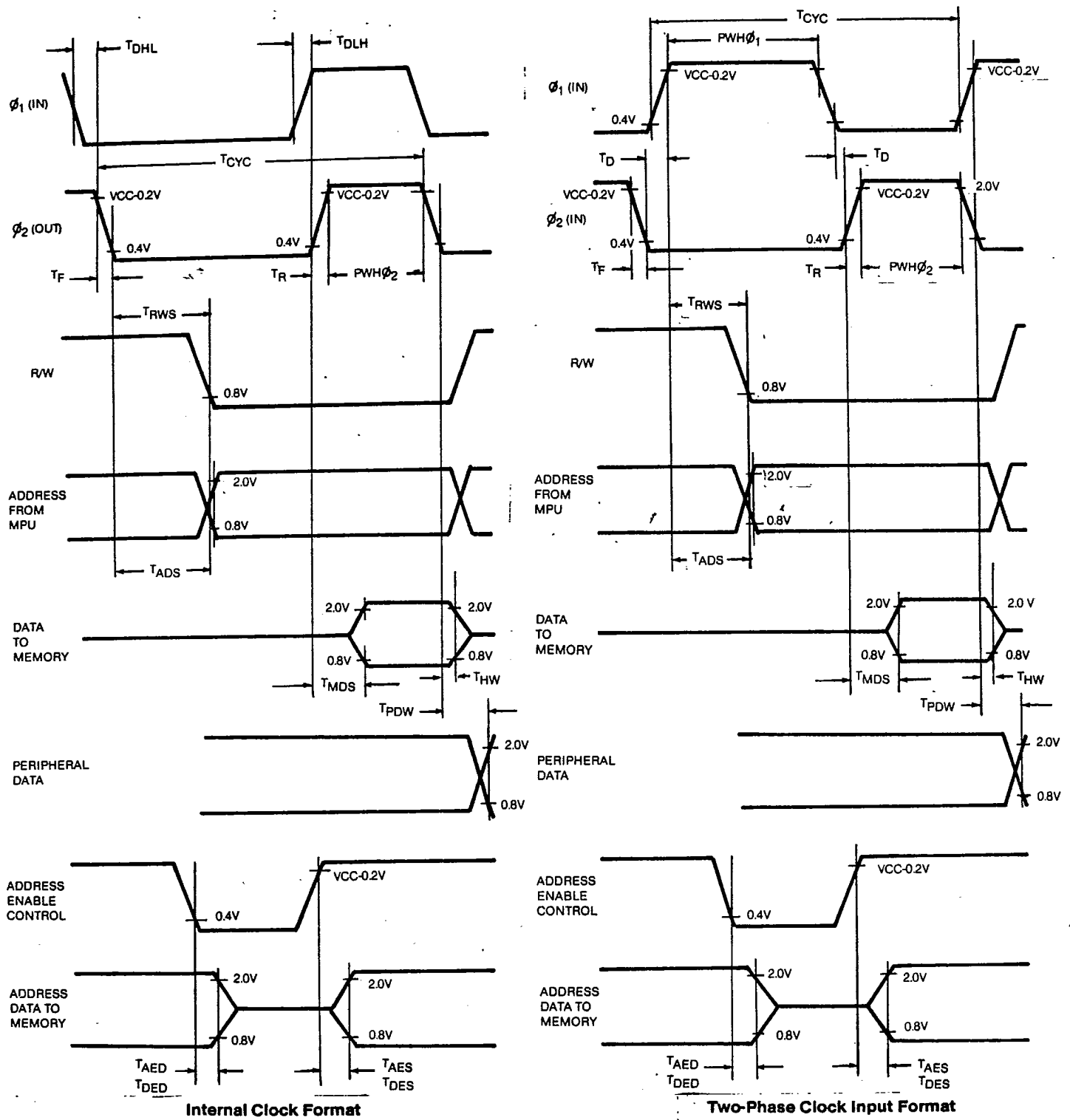


Internal Clock Format



Two Phase Clock Input Format

**TIMING FOR READING DATA FROM
MEMORY OR PERIPHERALS**



TIMING FOR WRITING DATA TO MEMORY OR PERIPHERALS

AC CHARACTERISTICS

1 MHz TIMING

2 MHz TIMING

3 MHz TIMING

ELECTRICAL CHARACTERISTICS ($V_{CC} = 5V \pm 5\%$, $V_{SS} = 0V$, $T_A = 0^\circ - 70^\circ C$)
Minimum Clock Frequency = 50 KHz

CLOCK TIMING

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS
Cycle Time	T_{CYC}	1000	—	—	500	—	—	333	—	—	ns
Clock Pulse Width ϕ_1 (Measured at $V_{CC}-0.2V$) ϕ_2	$PWH\phi_1$ $PWH\phi_2$	430 470	—	—	215 235	—	—	150 160	—	—	ns ns
Fall Time, Rise Time (Measured from 0.2V to $V_{CC}-0.2V$)	T_F, T_R	—	—	25	—	—	15	—	—	15	ns
Delay Time between Clocks (Measured at 0.2V)	T_D	0	—	—	0	—	—	0	—	—	ns

READING/WRITE TIMING (LOAD=1 TTL)

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS
Read/Write Setup Time from 6510	T_{RWS}	—	100	300	—	100	150	—	100	110	ns
Address Setup Time from 6510	T_{ADS}	—	100	300	—	100	150	—	100	125	ns
Memory Read Access Time	T_{ACC}	—	—	575	—	—	300	—	—	170	ns
Data Stability Time Period	T_{DSU}	100	—	—	60	—	—	40	—	—	ns
Data Hold Time-Read	T_{HR}	10	—	—	10	—	—	10	—	—	ns
Data Hold Time-Write	T_{HW}	10	30	—	10	30	—	10	30	—	ns
Data Setup Time from 6510	T_{MDS}	—	150	200	—	75	100	—	75	90	ns
Address Hold Time	T_{HA}	10	30	—	10	30	—	10	30	—	ns
R/W Hold Time	T_{HRW}	10	30	—	10	30	—	10	30	—	ns
Delay Time, ϕ_2 negative transition to Peripheral Data valid	T_{PDW}	—	—	1	—	—	150	—	—	125	ns
Peripheral Data Setup Time	T_{PDSU}	300	—	—	150	—	—	100	—	—	ns
Address Enable Setup Time	T_{AES}	—	—	75	—	—	75	—	—	75	ns
Data Enable Setup Time	T_{DES}	—	—	120	—	—	120	—	—	120	ns
Address Disable Hold Time*	T_{AED}	—	—	120	—	—	120	—	—	120	ns
Data Disable Hold Time*	T_{DED}	—	—	130	—	—	130	—	—	130	ns
Peripheral Data Hold Time	T_{PDH}	—	—	—	20	—	—	10	—	—	ns

*Note — 1 TTL Load, $C_L=30$ pF

SIGNAL DESCRIPTION

Clocks (ϕ_1, ϕ_2)

The 6510 requires either a two phase non-overlapping clock that runs at the Vcc voltage level, or an external control for the internal clock generator.

Address Bus (A_0-A_{15})

The three state outputs are TTL compatible, capable of driving one standard TTL load and 130 pf.

Data Bus (D_0-D_7)

Eight pins are used for the data bus. This is a Bi-Directional bus, transferring data to and from the device and peripherals. The outputs are tri-state buffers capable of driving one standard TTL load and 130 pf.

Reset

This input is used to reset or start the microprocessor from a power down condition. During the time that this line is held low, writing to or from the microprocessor is inhibited. When a positive edge is detected on the input, the microprocessor will immediately begin the reset sequence.

After a system initialization time of six clock cycles, the mask interrupt flag will be set and the microprocessor will load the program counter from the memory vector locations FFFC and FFFD. This is the start location for program control.

After Vcc reaches 4.75 volts in a power up routine, reset must be held low for at least two clock cycles. At this time the R/W signal will become valid.

When the reset signal goes high following these two clock cycles, the microprocessor will proceed with the normal reset procedure detailed above.

Interrupt Request (\overline{IRQ})

This TTL level input requests that an interrupt sequence begin within the microprocessor. The microprocessor will complete the current instruction being executed before recognizing the request. At that time, the interrupt mask bit in the Status Code Register will be examined. If the interrupt mask flag is not set, the microprocessor will begin an interrupt sequence. The Program Counter and Processor Status Register are stored in the stack. The microprocessor will then set the interrupt mask flag high so that no further interrupts may occur. At the end of this cycle, the program counter low will be loaded from address FFFE, and program counter high from location FFFF, therefore transferring program control to the memory vector located at these addresses.

Address Enable Control (AEC)

The Address Bus, R/W, and Data Bus are valid only when the Address Enable Control line is high. When low, the Address Bus, R/W and Data Bus are in a high-impedance state. This feature allows easy DMA and multiprocessor systems.

I/O Port (P_0-P_7)

Eight pins are used for the peripheral port, which can transfer data to or from peripheral devices. The Output Register is located in RAM at Address 0001, and the Data Direction Register is at Address 0000. The outputs are capable at driving one standard TTL load and 130 pf.

Read/Write (R/W)

This signal is generated by the microprocessor to control the direction of data transfers on the Data Bus. This line is high except when the microprocessor is writing to memory or a peripheral device.

ADDRESSING MODES

ACCUMULATOR ADDRESSING — This form of addressing is represented with a one byte instruction, implying an operation on the accumulator.

IMMEDIATE ADDRESSING — In immediate addressing, the operand is contained in the second byte of the instruction, with no further memory addressing required.

ABSOLUTE ADDRESSING — In absolute addressing, the second byte of the instruction specifies the eight low order bits of the effective address while the third byte specifies the eight high order bits. Thus, the absolute addressing mode allows access to the entire 65K bytes of addressable memory.

ZERO PAGE ADDRESSING — The zero page instructions allow for shorter code and execution times by only fetching the second byte of the instruction and assuming a zero high address byte. Careful use of the zero page can result in significant increase in code efficiency.

INDEXED ZERO PAGE ADDRESSING — (X, Y indexing) — This form of addressing is used in conjunction with the index register and is referred to as "Zero Page, X" or "Zero Page, Y." The effective address is calculated by adding the second byte to the contents of the index register. Since this is a form of "Zero Page" addressing, the content of the second byte references a location in page zero. Additionally, due to the "Zero Page" addressing nature of this mode, no carry is added to the high order 8 bits of memory and crossing of page boundaries does not occur.

INDEX ABSOLUTE ADDRESSING — (X, Y indexing) — This form of addressing is used in conjunction with X and Y index register and is referred to as "Absolute, X," and "Absolute, Y." The effective address is formed by adding the contents of X and Y to the address contained in the second and third bytes of the instruction. This mode allows the index register to contain the index or count value and the instruction to contain the base address. This type of indexing allows any location referencing and the index to modify multiple fields resulting in reduced coding and execution time.

IMPLIED ADDRESSING — In the implied addressing mode, the address containing the operand is implicitly stated in the operation code of the instruction.

RELATIVE ADDRESSING — Relative addressing is used only with branch instructions and establishes a destination for the conditional branch.

The second byte of the instruction becomes the operand which is an "Offset" added to the contents of the lower eight bits of the program counter when the counter is set at the next instruction. The range of the offset is — 128 to + 127 bytes from the next instruction.

INDEXED INDIRECT ADDRESSING — In indexed indirect addressing (referred to as [Indirect, X]), the second byte of the instruction is added to the contents of the X index register, discarding the carry. The result of this addition points to a memory location on page zero whose contents is the low order eight bits of the effective address. The next memory location in page zero contains the high order eight bits of the effective address. Both memory locations specifying the high and low order bytes of the effective address must be in page zero.

INDIRECT INDEXED ADDRESSING — In indirect indexed addressing (referred to as [Indirect, Y]), the second byte of the instruction points to a memory location in page zero. The contents of this memory location is added to the contents of the Y index register, the result being the low order eight bits of the effective address. The carry from this addition is added to the contents of the next page zero memory location, the result being the high order eight bits of the effective address.

ABSOLUTE INDIRECT — The second byte of the instruction contains the low order eight bits of a memory location. The high order eight bits of that memory location is contained in the third byte of the instruction. The contents of the fully specified memory location is the low order byte of the effective address. The next memory location contains the high order byte of the effective address which is loaded into the sixteen bits of the program counter.

INSTRUCTION SET — ALPHABETIC SEQUENCE

ADS Add Memory to Accumulator with Carry
AND "AND" Memory with Accumulator
ASL Shift left One Bit (Memory or Accumulator)

BCC Branch on Carry Clear
BCS Branch on Carry Set
BEQ Branch on Result Zero
BIT Test Bits in Memory with Accumulator
BMI Branch on Result Minus
BNE Branch on Result not Zero
BPL Branch on Result Plus
BRK Force Break
BVC Branch on Overflow Clear
BVS Branch on Overflow Set

CLC Clear Carry Flag
CLD Clear Decimal Mode
CLI Clear Interrupt Disable Bit
CLV Clear Overflow Flag
CMP Compare Memory and Accumulator
CPX Compare Memory and Index X
CPY Compare Memory and Index Y

DEC Decrement Memory by One
DEX Decrement Index X by One
DEY Decrement Index Y by One
EOR "Exclusive or" Memory with Accumulator

INC Increment Memory by One
INX Increment Index X by One
INY Increment Index Y by One

JMP Jump to New Location
JSR Jump to New Location Saving Return Address

LDA Load Accumulator with Memory
LDX Load Index X with Memory
LDY Load Index Y with Memory
LSR Shift One Bit Right (Memory or Accumulator)

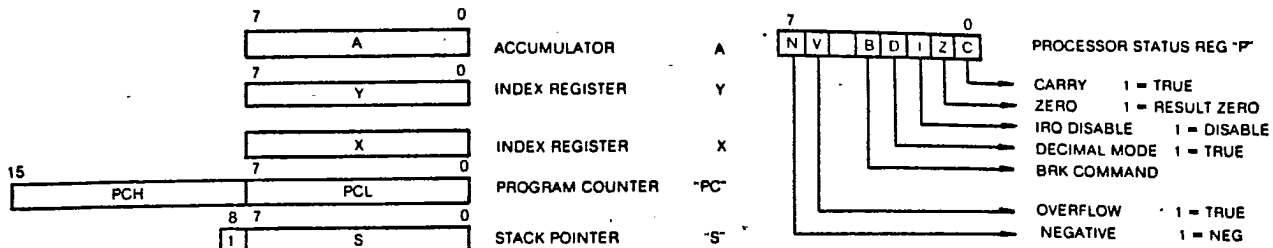
NOP No Operation
ORA "OR" Memory with Accumulator
PHA Push Accumulator on Stack
PHP Push Processor Status on Stack
PLA Pull Accumulator from Stack
PLP Pull Processor Status from Stack

ROL Rotate One Bit Left (Memory or Accumulator)
ROR Rotate One Bit Right (Memory or Accumulator)
RTI Return from Interrupt
RTS Return from Subroutine

SBC Subtract Memory from Accumulator with Borrow
SEC Set Carry Flag
SED Set Decimal Mode
SEI Set Interrupt Disable Status
STA Store Accumulator in Memory
STX Store Index X in Memory
STY Store Index Y in Memory

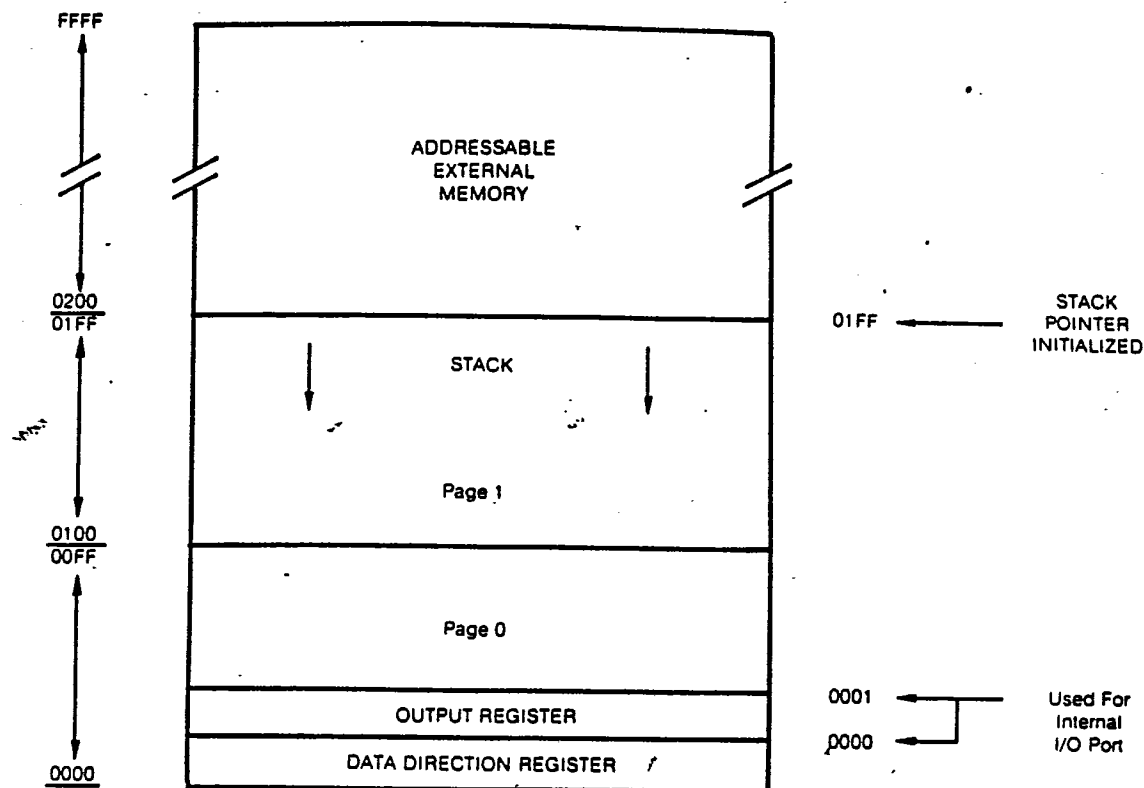
TAX Transfer Accumulator to Index X
TAY Transfer Accumulator to Index Y
TSX Transfer Stack Pointer to Index X
TXA Transfer Index X to Accumulator
TXS Transfer Index X to Stack Register
TYA Transfer Index Y to Accumulator

PROGRAMMING MODEL



INSTRUCTION SET-OP CODES, Execution Time, Memory Requirements

INSTRUCTIONS			IMMEDIATE		ABSOLUTE		ZERO PAGE		ACCUM		IMPLICIT		PAGE 0		PAGE 1		PAGE 2		PAGE 3		PAGE 4		PAGE 5		PAGE 6		PAGE 7		PAGE 8		PAGE 9		PAGE 10		PAGE 11		PAGE 12		PAGE 13		PAGE 14		PAGE 15		PAGE 16		PAGE 17		PAGE 18		PAGE 19		PAGE 20		PAGE 21		PAGE 22		PAGE 23		PAGE 24		PAGE 25		PAGE 26		PAGE 27		PAGE 28		PAGE 29		PAGE 30		PAGE 31		PAGE 32		PAGE 33		PAGE 34		PAGE 35		PAGE 36		PAGE 37		PAGE 38		PAGE 39		PAGE 40		PAGE 41		PAGE 42		PAGE 43		PAGE 44		PAGE 45		PAGE 46		PAGE 47		PAGE 48		PAGE 49		PAGE 50		PAGE 51		PAGE 52		PAGE 53		PAGE 54		PAGE 55		PAGE 56		PAGE 57		PAGE 58		PAGE 59		PAGE 60		PAGE 61		PAGE 62		PAGE 63		PAGE 64		PAGE 65		PAGE 66		PAGE 67		PAGE 68		PAGE 69		PAGE 70		PAGE 71		PAGE 72		PAGE 73		PAGE 74		PAGE 75		PAGE 76		PAGE 77		PAGE 78		PAGE 79		PAGE 80		PAGE 81		PAGE 82		PAGE 83		PAGE 84		PAGE 85		PAGE 86		PAGE 87		PAGE 88		PAGE 89		PAGE 90		PAGE 91		PAGE 92		PAGE 93		PAGE 94		PAGE 95		PAGE 96		PAGE 97		PAGE 98		PAGE 99		PAGE 100		PAGE 101		PAGE 102		PAGE 103		PAGE 104		PAGE 105		PAGE 106		PAGE 107		PAGE 108		PAGE 109		PAGE 110		PAGE 111		PAGE 112		PAGE 113		PAGE 114		PAGE 115		PAGE 116		PAGE 117		PAGE 118		PAGE 119		PAGE 120		PAGE 121		PAGE 122		PAGE 123		PAGE 124		PAGE 125		PAGE 126		PAGE 127		PAGE 128		PAGE 129		PAGE 130		PAGE 131		PAGE 132		PAGE 133		PAGE 134		PAGE 135		PAGE 136		PAGE 137		PAGE 138		PAGE 139		PAGE 140		PAGE 141		PAGE 142		PAGE 143		PAGE 144		PAGE 145		PAGE 146		PAGE 147		PAGE 148		PAGE 149		PAGE 150		PAGE 151		PAGE 152		PAGE 153		PAGE 154		PAGE 155		PAGE 156		PAGE 157		PAGE 158		PAGE 159		PAGE 160		PAGE 161		PAGE 162		PAGE 163		PAGE 164		PAGE 165		PAGE 166		PAGE 167		PAGE 168		PAGE 169		PAGE 170		PAGE 171		PAGE 172		PAGE 173		PAGE 174		PAGE 175		PAGE 176		PAGE 177		PAGE 178		PAGE 179		PAGE 180		PAGE 181		PAGE 182		PAGE 183		PAGE 184		PAGE 185		PAGE 186		PAGE 187		PAGE 188		PAGE 189		PAGE 190		PAGE 191		PAGE 192		PAGE 193		PAGE 194		PAGE 195		PAGE 196		PAGE 197		PAGE 198		PAGE 199		PAGE 200		PAGE 201		PAGE 202		PAGE 203		PAGE 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**6510 MEMORY MAP****APPLICATIONS NOTES**

Locating the Output Register at the internal I/O Port in Page Zero enhances the powerful Zero Page Addressing instructions of the 6510.

By assigning the I/O Pins as inputs (using the Data Direction Register) the user has the ability to change the contents of address 0001 (the Output Register) using peripheral devices. The ability to change these contents using peripheral inputs, together with Zero Page Indirect Addressing instructions, allows novel and versatile programming techniques not possible earlier.

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