67417

Serializing First-In First-Out
(FIFO) 64 x 8/9 Memory

Advanced
Micro
Devices

Features/Benefits

- **High-speed 28-MHz serial shift-in/shift-out rate**
- **10-MHz parallel shift-in/shift-out rate**
- **Three-state outputs with HI-current drive**
- **Cascadable at parallel port only**
- **Half-full flag (32 or more)**
- **Selectable 64x8 or 64x9 FIFO configuration thus providing "frame mark bit"**

Typical Applications

- **LAN equipment**
- **Data communication**
- **Office automation**
- **Microcomputers**
- **Minicomputers**
- **Disk/tape controllers**

Description

The 67417 is a serializing/deserializing FIFO. This FIFO, the first one of its type in the industry, is organized 64 words x 8/9 bits wide. Like traditional Monolithic Memories' FIFOs it is cascadable, but only at the parallel port.

Ordering Information

Part Number	Package	Temp	Description
67417	CD 024	Com	64x8/9

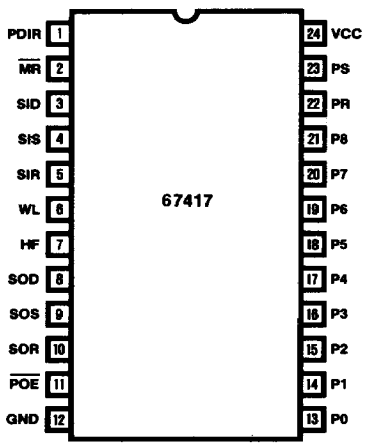
In addition, the device has the ability to connect directly to a system bus. These features make it a complete "sub-system on a chip."

The FIFO basically has three modes of operation;

1. Serial in to parallel out
2. Parallel in to serial out
3. Serial in to serial out (requires non-standard logic level on PDIR).

In the first mode, serial data can be accepted at up to 28 MHz and the FIFO outputs parallel data at up to 10 MHz. Similarly, in the alternate mode parallel data can be transformed into serial data. Please refer to appendix for detailed description.

Pin Configuration



Pin Names

P0-P8	Parallel Data
PS	Parallel Shift In/Out
PR	Parallel Input/Output Ready
$\overline{POE}$	Parallel Output Enable
SID	Serial Input Data
SIS	Serial Input Shift
SIR	Serial Input Ready
SOD	Serial Output Data
SOS	Serial Output Shift
SOR	Serial Output Ready
PDIR	Parallel Port Direction
WL	Word Length
$\overline{MR}$	Master Reset
HF	Half Full Flag
VCC	VCC
GND	Ground

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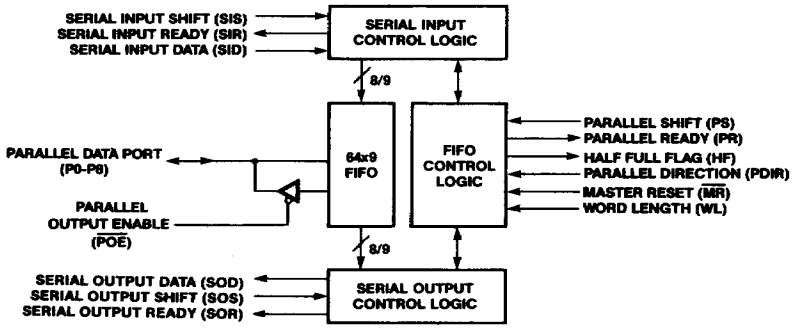
Issue Date: May 1988

Block Diagram



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Absolute Maximum Ratings

Supply voltage V_{CC} ..... -0.5 V to 7 V
Input voltage ..... -1.5 V to 7 V
Off-state output voltage ..... -0.5 V to 5.5 V
Storage temperature ..... -65° to +150°C

Operating Conditions

SYMBOL	PARAMETER	FIGURE	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{CC}	Voltage		4.75	5	5.25	V
T_A	Operating free-air temperature		0		75	°C
	SERIAL INPUT PARAMETERS					
f_{SIN}	Max. Serial Shift-In Rate	1			28	MHz
t_{SISH}	Serial Shift-In HIGH time	1	23			ns
t_{SISL}	Serial Shift-In LOW time	1	12			ns
t_{SIDS}	Serial Input Data Setup time	1	14			ns
t_{SIDH}	Serial Input Data Hold time	1	0			ns
t_{SIRHS}	Recovery Time Serial Input Ready ↑ to Serial Input Shift ↓	1	0			ns
	SERIAL OUTPUT PARAMETERS					
f_{SOUT}	Max. Serial Shift-Out Rate	1			28	MHz
t_{SOSH}	Serial Shift-Out HIGH time	3	15			ns
t_{SOSL}	Serial Shift-Out LOW time	3	15			ns
t_{ORHS}	Recovery time Serial Output Ready ↑ to Serial Output Shift ↑	3	5			ns
	WORD LENGTH PARAMETERS					
t_{SWL}	Setup SIS, SOS	1,3	18			ns
t_{HWL}	Hold SIS, SOS	1,3	3			ns
	PARALLEL PORT PARAMETERS					
f_P	Parallel shift-in/shift-out rate	8			10	MHz
t_{PSH}	Parallel Shift-In/Out HIGH time	5/8	30			ns
t_{PSL}	Parallel Shift-In/Out LOW time	5/8	30			ns
t_{PIDS}	Parallel Input Data Setup time	5	-5			ns
t_{PIDH}	Parallel Input Data hold time	5	35			ns
t_{PDIRSL}	Shift LOW to parallel direction transition	14	50			ns
t_{PDIRSH}	Parallel direction transition to Shift HIGH	14	50			ns
t_{PRHS}	Parallel Ready ↑ to Parallel Shift Low	10/11	30			ns
	MASTER RESET PARAMETER					
t_{MRW}	Master Reset LOW time	12/13	40			ns

Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER	FIGURE	COMMERCIAL MIN	TYP	MAX	UNIT
	SERIAL INPUT PARAMETERS					
t_{SIRL}	Serial Input Shift ↑ to Serial Input Ready LOW	2			23	ns
t_{SIHFH}	Serial Input Shift ↑ to Half-Full Flag HIGH	7			1.3	µs
	SERIAL OUTPUT PARAMETERS					
t_{SORL}	Serial Output Shift ↑ to Serial Output Ready LOW	4			23	ns
t_{SOD}	Serial Output Shift ↑ to Serial Output data	3			23	ns
t_{ODRH}	Serial Output Data valid to Serial Output Ready HIGH	3	0	25		ns
t_{SOHFL}	Serial Output Shift ↑ to Half-Full LOW	7			1.3	µs
	PARALLEL INPUT/OUTPUT PARAMETERS					
t_{PSPRL}	Parallel Shift ↑ to Parallel Ready LOW	5/8			65	ns
t_{PSPRH}	Parallel Shift ↓ to Parallel Ready HIGH	5/8/10			80	ns
t_{PSHFH}	Parallel Shift-In ↓ to Half-Full HIGH	6			1.3	µs
t_{PSHFL}	Parallel Shift-Out ↓ to Half-Full LOW	9			1.3	µs
	PARALLEL OUTPUT PARAMETERS					
t_{PODH}	Minimum Parallel Shift ↓ to Ouput data	8	20			ns
t_{POD}	Maximum Parallel Shift ↓ to Output data	8			60	ns
t_{PODV}	Minimum Output data valid to parallel ready HIGH	8	0	15		ns
	OTHER PARAMETERS					
t_{PT}	Fall-through time	10/11/16/17			2.6	µs
t_{IPH}	Parallel Input Ready pulse HIGH	11	30			ns
t_{OPH}	Parallel Output Ready pulse HIGH	10	30			ns
t_{MRO}	$\overline{\text{Master Reset}}$ ↓ to Data Out LOW	12			65	ns
t_{MRSIRL}	$\overline{\text{Master Reset}}$ ↓ to Serial Input Ready LOW	12			40	ns
t_{MRSIRH}	$\overline{\text{Master Reset}}$ ↑ to Serial Input Ready HIGH	12			40	ns
t_{MRPRL}	$\overline{\text{Master Reset}}$ ↓ to Parallel Ready LOW	12/13			40	ns
t_{MRPRH}	$\overline{\text{Master Reset}}$ ↑ to Parallel Ready HIGH	13			30	ns
t_{MRSORL}	$\overline{\text{Master Reset}}$ ↓ to Serial Output Ready LOW	13			40	ns
t_{MRHFL}	Master Reset ↓ to Half-Full LOW	12/13			60	ns
t_{PDIROR}	Parallel Direction change to new Output Ready	14			60	ns
t_{PDIROD}	Parallel Direction change to Output data valid	14			60	ns
t_{PDIRPZ}	Parallel Direction change to Parallel Output data Hi-Z	14			35	ns
t_{PDIRSZ}	Parallel Direction changes to Serial Output-data Hi-Z	14			80	ns
t_{PZX}	Output enable time $\overline{\text{POE}}$ to P0-8	15			30	ns
t_{PXZ}	Output disable time $\overline{\text{POE}}$ to P0-8	15			35	ns

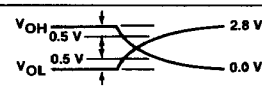
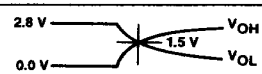
Electrical Characteristics Over Operating Conditions

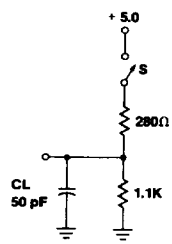
SYMBOL	PARAMETER	TEST CONDITIONS				COM MIN	COM TYP	COM MAX	UNIT
V_{IL}	Low-level input voltage							0.8†	V
V_{IH}	High-level input voltage					2†			V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = −18 mA					−1.5	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.4 V					−0.4	mA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = 2.4 V					0.1	mA
I_I	Maximum input current	V_{CC} = MAX	V_I = 5.5 V					0.4	mA
V_{OL}	Low-level output voltage	V_{CC} = MIN	Data Outputs P0-P8, SOD	I_{OL} = 24 mA	0°C-75°C			0.58	V
					25°C			0.55	
				I_{OL} = 16 mA	0°C-75°C			0.5	
			All other outputs	I_{OL} = 8 mA				0.5	
V_{OH}	High-level output voltage	V_{CC} = MIN	I_{OH} = −3 mA			2.4			V
I_{OS}	Output short-circuit current*	V_{CC} = MAX	V_O = 0 V			−20		−90	mA
I_{LZ}	Off-state output current* SOD P0 to P8	V_{CC} = MAX	V_O = 0.4 V					−100	μA
I_{HZ}			V_O = 2.4 V					100	mA
I_{CC}	Supply current	V_{CC} = MAX						350	mA
O_V	PDIR non-standard over voltage	Serial-In, Serial-Out				10		16	V

* Not more than one output should be shorted at a time and duration of the short circuit not exceed one second.

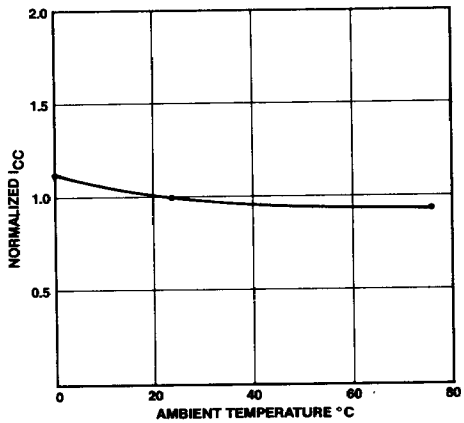
† This is an absolute voltage with respect to device GND (pin 12) and includes all overshoots due to test equipment.

Test Waveforms

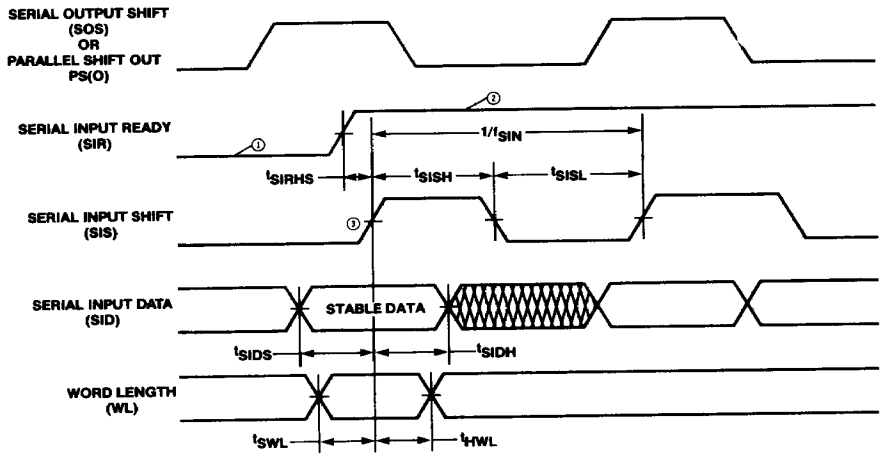
TEST	S = OPEN	S = CLOSED	OUTPUT WAVEFORM-MEAS-LEVEL
All t_{PD}		All t_{PD}	
t_{PXZ}	t_{PHZ}	t_{PLZ}	
t_{PZX}	t_{PZH}	t_{PZL}	



I_{CC} VS Temperature

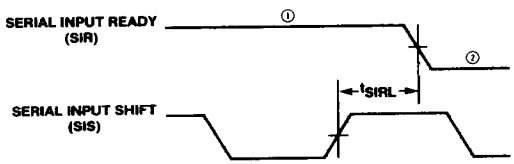


Definition of Waveforms



① FIFO is full.
② Shift-out (serial or parallel) is asserted, SIR goes High.
③ SIS can be asserted t_{SIRHS} after serial input ready changes from low-to-high.

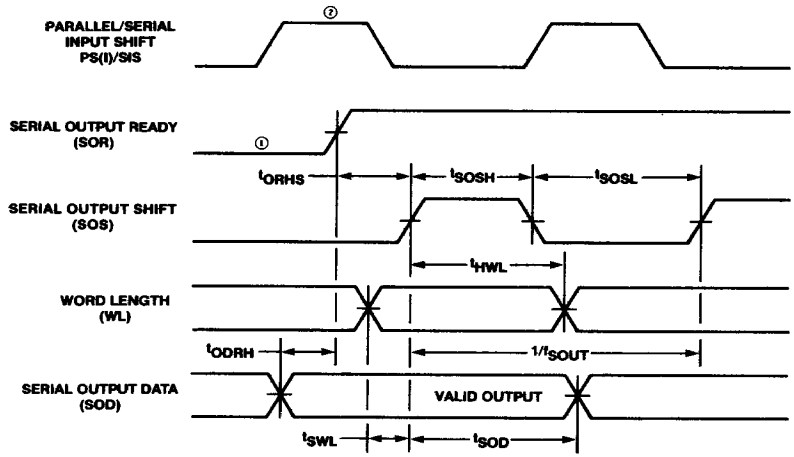
Figure 1. Serial Input Timing



① FIFO is not full.
② FIFO is full

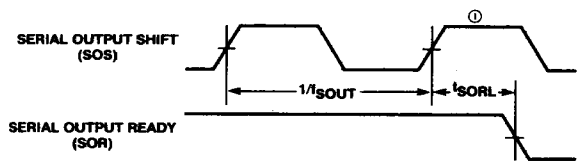
Figure 2. FIFO Full Specification (t_{SIRL})

Definition of Waveforms (cont'd)



① FIFO is empty, output ready remains Low and shift-out cannot be applied.
② After a word is shifted in, output ready goes High and shift-out can be applied.
③ The first serial bit is P0.

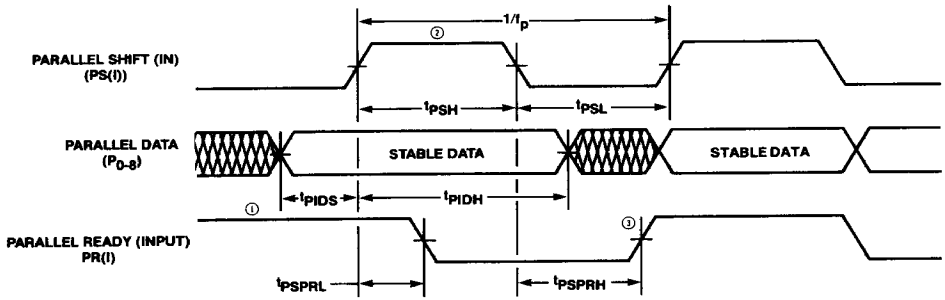
Figure 3. Serial Output Timing



① After the last shift-out, output ready goes Low indicating FIFO is empty.

Figure 4. FIFO Empty Specifications (t_{SORL})

Definition of Waveforms (cont'd)



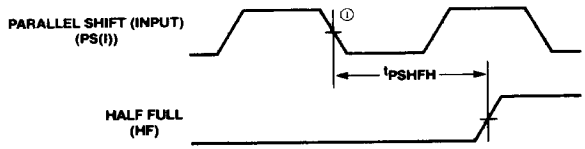
NOTE: P_{DIR} = High for the mode parallel-in to serial-out. Parallel ready is an output flag from the FIFO indicating that a word can be loaded into the FIFO.

① FIFO is not full and ready for input.

② PS (In) is asserted, shifting in parallel data P0-8.
PR (In) goes Low indicating parallel port is in use and no longer ready.
PR (In) will remain Low as long as PS (In) remains High.

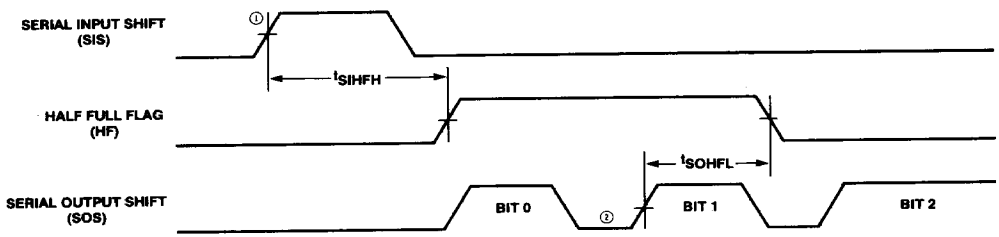
③ PS (In) has gone Low, allowing recent word to propagate through FIFO, PR (In) returns High when ready for more input.

Figure 5. Parallel Input Shift Timing



① for P_{DIR} = High, the direction is parallel-in to serial-out. After the 32nd shift-in, the half-full flag is set to High, and remains High, indicating the presence of 32 or more words.

Figure 6. Half-full Flag Specifications on Parallel (t_{PSHFH})

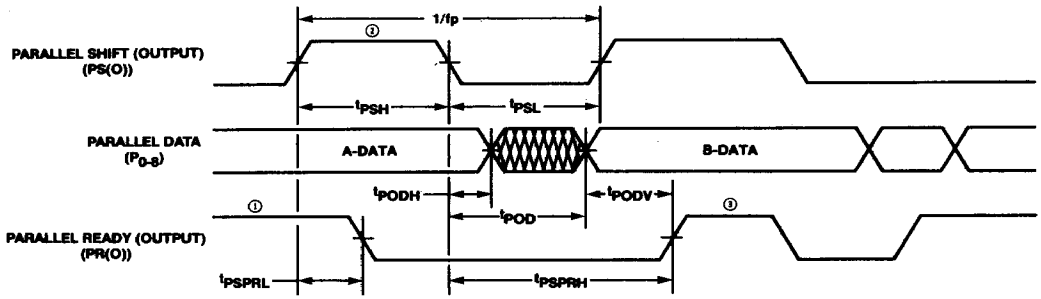


① When there are 31 words in the FIFO, the next shift-in on the 32nd word sets the half-full flag (HF) High indicating that there are 32 or more words.

② As soon as one word is partially shifted out, HF goes Low indicating there are less than 32 words.

Figure 7. Half-full Flag Specification on Serial Operation (t_{SIHFH}, t_{SOHFL})

Definition of Waveforms (cont'd)



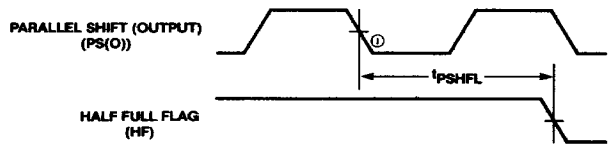
NOTE: For above conditions P_{DIR} = Low indicating that the direction is from serial-in to parallel-out. Thus parallel ready indicates the output status.

① FIFO is not empty and at least one word is valid and ready at P0-8 outputs.

② PS (Out) is asserted, shifting out parallel data. Data remains valid, but: PR (Out) goes Low to indicate parallel port is in use and no longer ready. PR (Out) will remain Low as long as PS (Out) remains High.

③ PS (Out) has gone Low, allowing data word to be shifted out. Next data word appears at output and PR (Out) is asserted to indicate valid data ready.

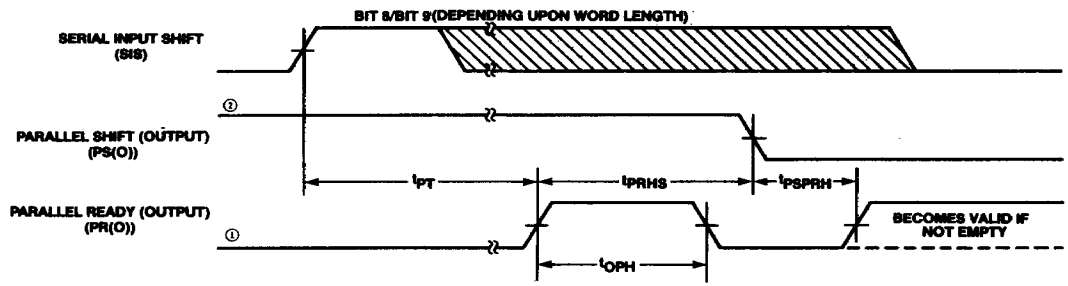
Figure 8. Serial-in to Parallel-out Specifications (t_{POD}, t_{PODH}, t_{ODV})



NOTE: For P_{DIR} = Low the direction is serial-in to parallel-out.

① When a word is shifted out and the half-full flag goes Low, 31 words or less are in the FIFO.

Figure 9. Half-full Flag Specification on Parallel Shift-out (t_{PSHFL})



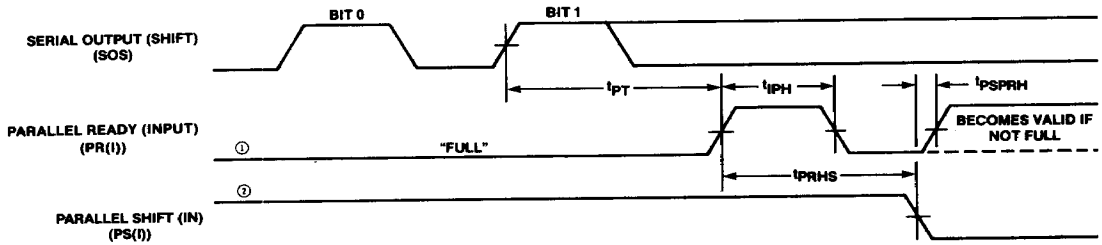
NOTE: P_{DIR} = Low indicating serial-in to parallel-out.

① FIFO initially empty.

② PS (Out) held High.

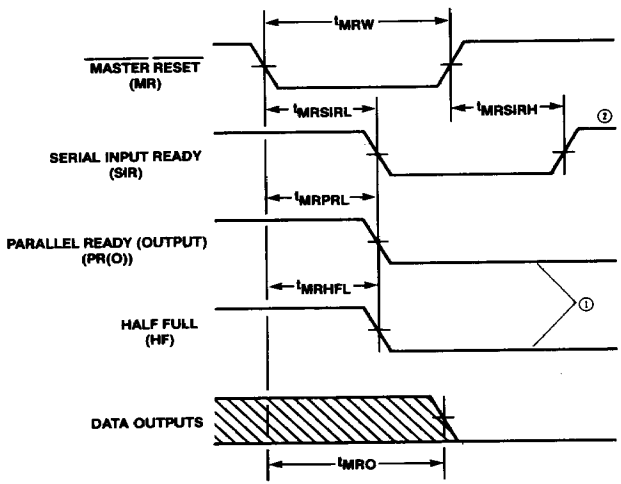
Figure 10. t_{PSPRH}, t_{PT}, t_{POH} Specifications (Serial Input Mode)

Definition of Waveforms (cont'd)



NOTE: P_{DIR} = High (parallel-in to serial-out).
① FIFO is full.
② PS (I) held High.

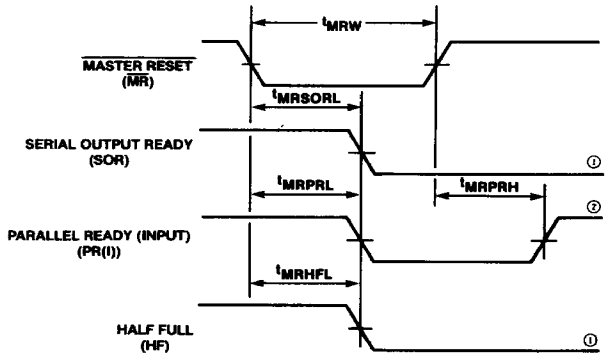
Figure 11. Fall-through Specifications



NOTE: P_{DIR} = Low.
① PR (O) and HF go Low.
② After $\overline{MR}$ goes High, SIR goes High.

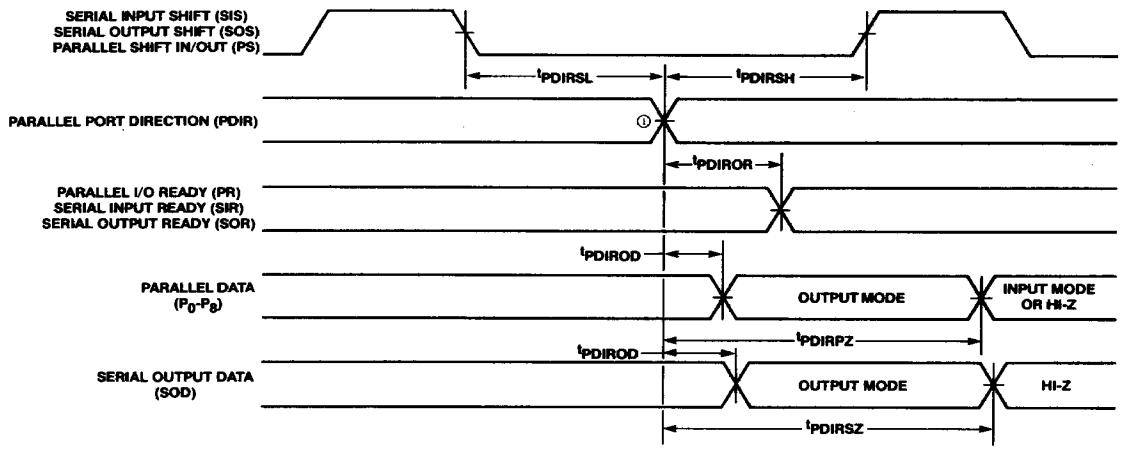
Figure 12. Master Reset Timing Serial-in to Parallel-out

Definition of Waveforms (cont'd)



NOTE: P_{DIR} = High.
① SOR and HF go Low.
② Affter $\overline{MR}$ goes High, PR(I) goes High.

Figure 13. Master Reset Timing (Parallel-in to Serial-out)



NOTE: When the FIFO is used as a stack, change the port direction before the FIFO is full; otherwise, data may be lost.

Figure 14. P_{DIR} Transition Parameters

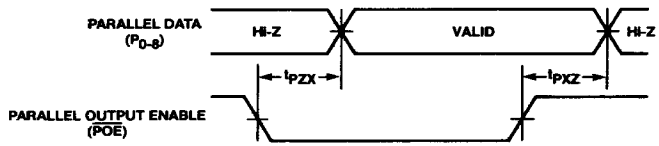


Figure 15. Parallel Port Enable and Disable Timing

Definition of Waveforms (cont'd)

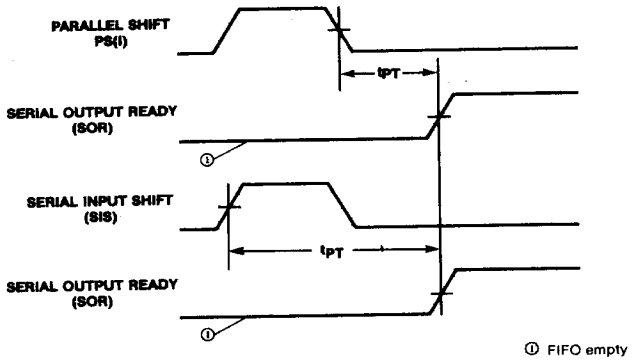


Figure 16. t_{PT} Specification (Shift-in to Serial Output Ready)

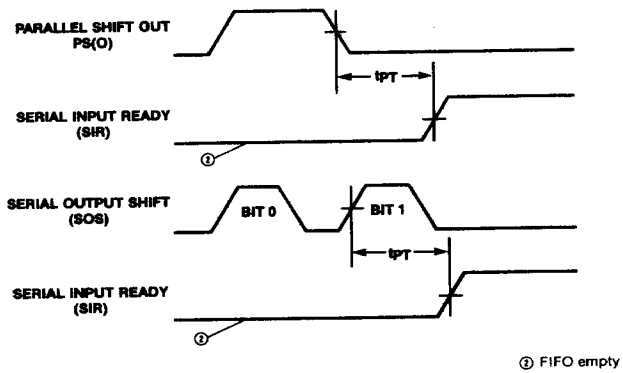


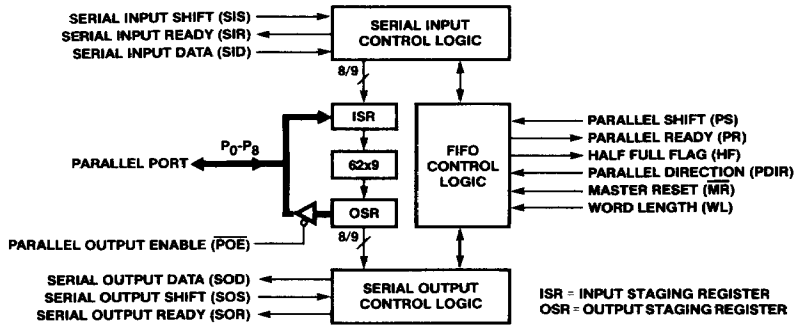
Figure 17. t_{PT} Specification (Shift-in to Serial Input Ready)

Appendix
Detailed Functional/Description for 67417

The 67417 is a serializing FIFO intended as a one-chip solution for data buffering and serializing/deserializing. It can be successfully used for interfacing parallel-format computing equipment to serial-format data communications and mass-memory equipment. The 67417 is a word-oriented device. It is meant to function with complete 8- or 9-bit words of data.

Parallel Port

This is a fully bidirectional port, and it operates at a more conservative data rate of 10 MHz. The input-staging register (ISR) internally controls the parallel input data port bus signals. Likewise the OSR internally controls the parallel output data port. The ISR data outputs drive the parallel data inputs to the cell array, and the OSR inputs are likewise driven by the final parallel data stage of the cell array



Basically the major internal subsystems of the 67417 are:

(i) The serial input port
(ii) The serial output port
(iii) The parallel port
(iv) The FIFO control logic and
(v) The cell array

Serial Port

The two serial ports (input and output) are entirely separate which allows a high-speed data rate of 28 MHz. These serial ports do not share data pins, control pins, or internal circuits. However, since the serial output data is a three-state output, the serial data ports could be connected together in the normal serial-parallel operation mode with separate SOR and SIR status signals.

The serial input port interface consists of the Serial Input Ready (SIR) output, Serial Input Data (SID) input, and the Serial Input Shift (SIS) clock input. Unlike the analogous SI and IR signals on the 67401/2, SIS and SIR do not accomplish a "handshake" with the rest of the logic of the system which incorporates the 67417; rather SIR is asserted whenever the 67417 is still capable of receiving at least one more bit. SIS is a positive edge-triggered input which sequences the serial input control logic. This logic in turn controls SIR and the 8/9-bit Input Staging Register (ISR).

The serial output port interface is the dual of the above, with a Serial Output Data (SOD) output, a Serial Output Shift (SOS) clock input, and a Serial Output Ready (SOR) status output. SOR is asserted whenever at least one more bit is available at the output. SOS is a positive edge-triggered input which sequences the 8/9-bit Output Staging Register (OSR). Serial Output Data is automatically three-stated whenever the serial output port is disabled (during Master Reset) and PDIR = Low. The parallel port is controlled by Parallel Shift (PS) input and Parallel Direction Input (PDIR). Parallel Ready (PR) is the handshake/status output. At the Parallel Port PS and PR *do* accomplish a handshake with the outside world as SI, IR, SO and OR on the 67401/2.

Modes of Operation

There are three modes in which the 67417 can operate

(i) Parallel-in to serial-out
(ii) Serial-in to parallel-out and
(iii) Serial-in to serial-out.

In the parallel-in to serial-out mode, PDIR = HIGH. Thus Parallel Shift (PS) acts as a Shift In (SI) and similarly, Parallel Ready (PR) as Input Ready (IR). The first bit shifted out of the serial port will be bit 0 of the parallel word input.

Similarly for serial-in to parallel-out mode, PDIR = LOW, and Parallel Shift (PS) acts as a Shift Out(SO) and Parallel Ready (PR) as Output Ready (OR). The first bit shifted into the serial port will be bit 0 of the parallel word output.

If the direction mode for a particular application of the 67417 is not intended to change during system operation, the PDIR input should be strapped to a logic LOW or HGH.

In the serial-in to serial-out mode, PDIR = 10 V minimum.

The parallel port does not function during this mode and is three-stated. The direction operating mode should not be changed if the FIFO is FULL otherwise stored data will be lost.

Cell Array

The 67417 cell array can function *either* as a 64x8 FIFO (with the 9th bit padded to a zero) or as a 64x9 FIFO, according to the setting of the word length (WL) control input. Like the PDIR

control input, WL can be switched at electronic speeds during system operations; but if the word length of a particular 67417 is *never* to change during system operation, WL for that part can be strapped to ground or V_{CC}.

It is a permissible 67417 mode of operation to almost fill the FIFO (there should be at least two empty locations) with WL set to 8-bit operation, then switch WL to 9-bit operation (WL = HIGH) to load one more word plus a frame marker in the last bit, and then switch PDIR and unload the 67417 in a 9-bit mode. This sequence of operations has the effect of providing a "frame marker bit" in the ninth bit of the last word loaded. The corresponding 9th bits will have been zeroed by the 67417 internal logic for all the other words in the frame since they were loaded while the 67417 was operating as an 8-bit device.

It is, however, the system designer's responsibility to avoid changing PDIR inputs when only part of an 8- or 9-bit word has been received or transmitted. In general, if such a change occurs, the part in general will try to add zero bits to pad out the impacted word to assume full length.

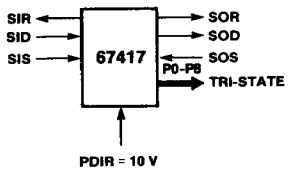
Half-Full Flag

This status output indicates when the 67417 statically contains 32 words or more. This provides an indication to send in more data if the device is operated in a mostly-empty mode or send out more data if the 67417 is operated in a mostly-full mode.

Cascading

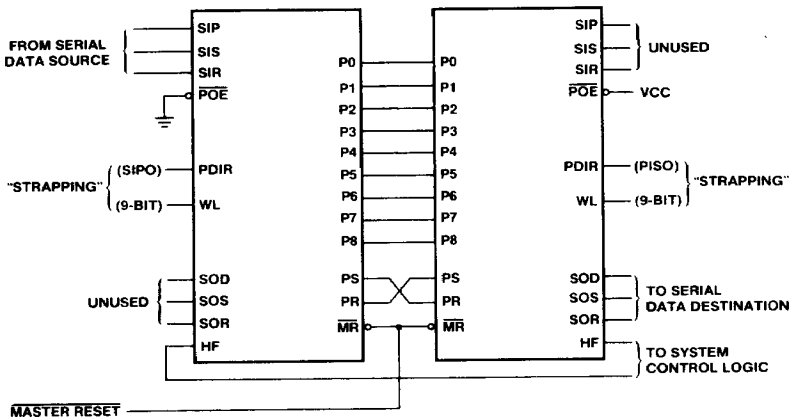
The 67417 is designed to be cascaded at the parallel port only, due to very high data transfer rates at the serial ports. Cascading two 67417's is accomplished by connecting Parallel Input/Output Ready (PR) of each part to control the Parallel Shift In/Out (PS) of the other part, with one FIFO in serial-in to parallel-out mode, and the other FIFO in parallel-in to serial-out mode. The combined effect of this is a reversible 128x8 or 128x9 serial-in serial-out FIFO. The 67417 can not be cascaded at the serial ports because SIR and SOR are not acknowledged signals but rather status signals only.

Applications



NOTE: It can shift in data serially in the multiples of 8- or 9-bit according to WL.

Figure 18. 512/576x1 Serial-in to Serial-out Mode



* SIPO = Serial-in to Parallel-out.
** PISO = Parallel-in to Serial-out.

Figure 19. Cascading of Two 'S417s for Serial-in to Serial-out Operation as a 128x9 (1152x1) FIFO

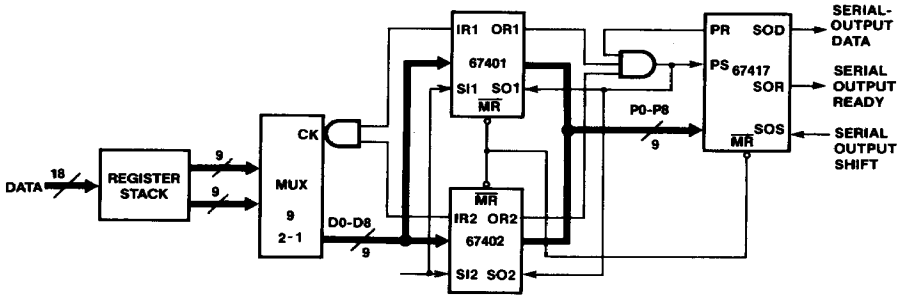


Figure 20. An Example of an Expansion Scheme for a 64x18 Parallel-to-Serial FIFO

An 18-bit data word is multiplexed into the two 67401/2 FIFOs. Since the 67417 FIFO is cascadable at the parallel port only, two 67401/2 FIFOs were used along with the 67417 to obtain the appropriate organization.

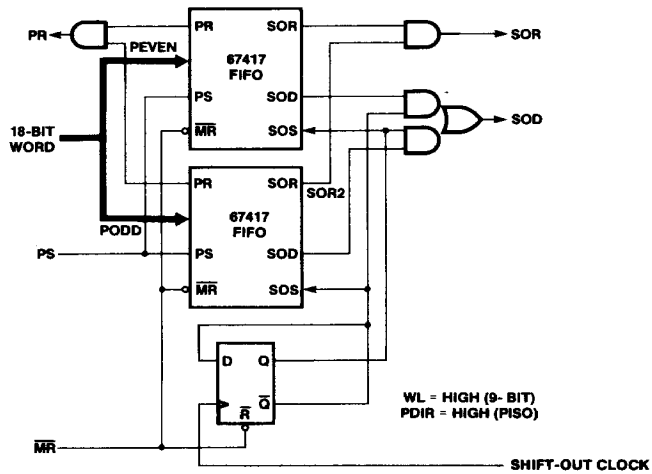


Figure 21. Another Example of an Expansion Scheme for a 64x18 Parallel-in to Serial-out FIFO Two 67417 FIFOs Are Used to Implement a 64x18 Parallel-in to Serial-out FIFO

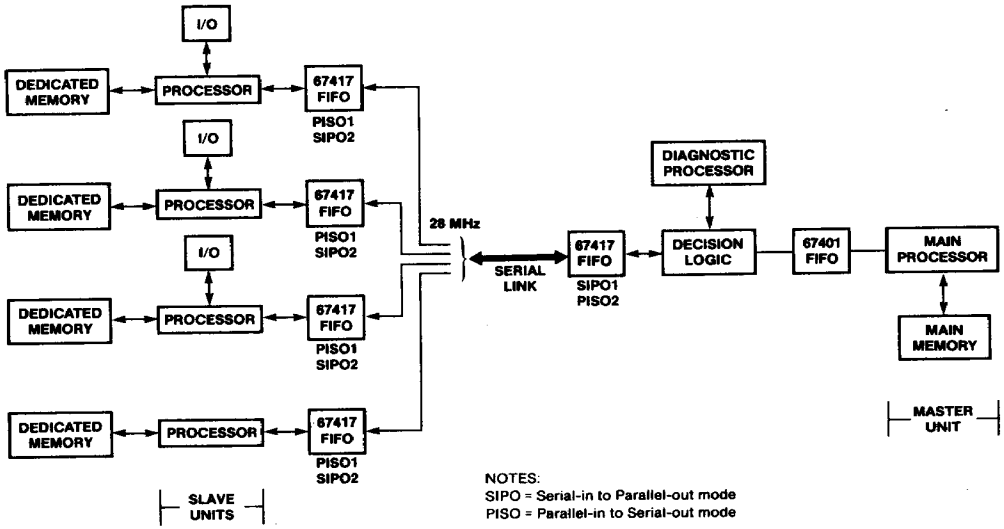


Figure 22. A Multiprocessing System

Each processor unit on the left has its own communication interface which consists of a serializing FIFO. The serial data link can operate in either direction 1 or direction 2 which is decided by the Decision logic. In direction 1 either of the slave units send the data to the master over the serial link, with its respective 67417 operating in parallel-in to serial-out mode (PISO1). While the 67417 for the master unit operates in serial-in to parallel-out mode (SIPO1). The direction 2 has the FIFOs (67417) operating in the reverse direction from the above case. Decision logic determines the priority of the slave processors to use the serial link.