FINAL

67C4033

Low Density First-In First-Out (FIFO) 64 x 5 CMOS Memory (Cascadable)

Advanced Micro Devices

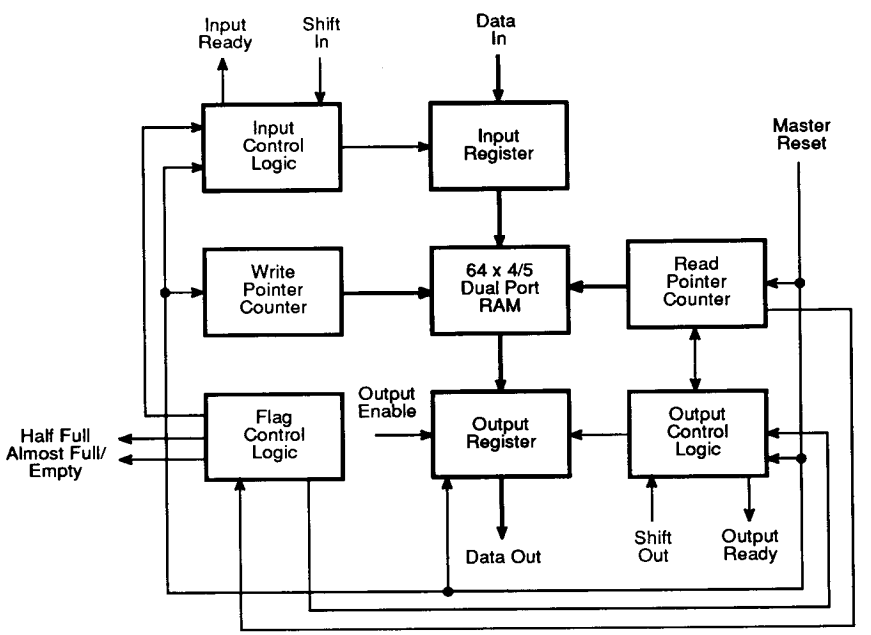
DISTINCTIVE CHARACTERISTICS

- Zero standby power
- High-speed 15 MHz shift-in/shift-out rates
- Very low active power consumption
- TTL-compatible inputs and outputs
- Readily expandable in word width and depth
- Half-Full and Almost-Full/Empty status flags
- RAM-based architecture for short fall-through delay
- Full CMOS 8-transistor cell for maximum noise immunity
- Asynchronous operation
- Output enable

GENERAL DESCRIPTION

The 67C4033 device is a high-performance CMOS RAM-based First-In First-Out (FIFO) buffer memory products organized as 64 words by 4 x 5 bits wide. This device uses Advanced Micro Devices latest CMOS process technology and meets the demands for high-speed, low-power operation. By utilizing an on-chip, dual-port RAM, a very short fall-through time is realized, thus improving overall system performance. By using both Read and Write pointers for addressing each memory location, the data can propagate to the outputs in much less time than in traditional register-based FIFOs. These FIFOs are easily integrated into many applications and perform particularly well for high-speed disk controllers, graphics, and communication network systems. The 550 µW standby power specification makes these devices ideal for ultra-low power and battery-powered systems.

BLOCK DIAGRAM



10684B-1

Publication# 10684 Rev. B Amendment/0
Issue Date: September 1992

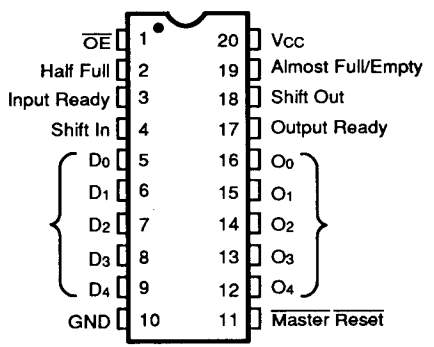
PRODUCT SELECTOR GUIDE

Part Number	67C4033-10	67C4033-15
Shift-In/Shift-Out Rate Operating Frequency	10 MHz	15 MHz
Maximum Power Supply Current	35 mA	45 mA
Operating Range	Com'l	Com'l

CONNECTION DIAGRAMS

Top View

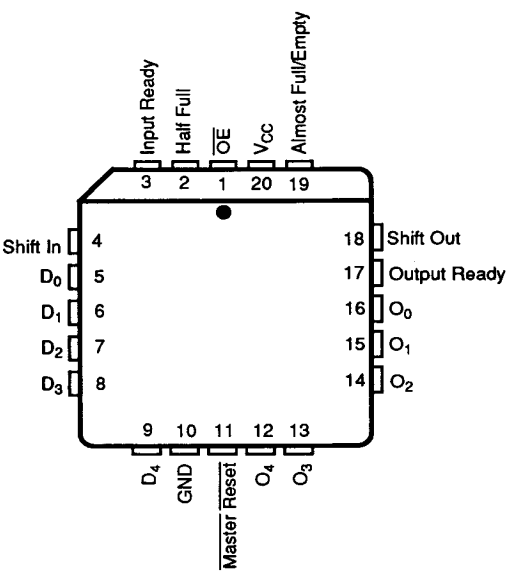
DIPs



10684B-2

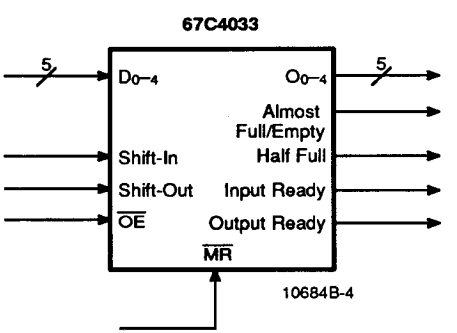
Note:
Pin 1 is marked for orientation for plastic packages.

PLCC



10684B-3

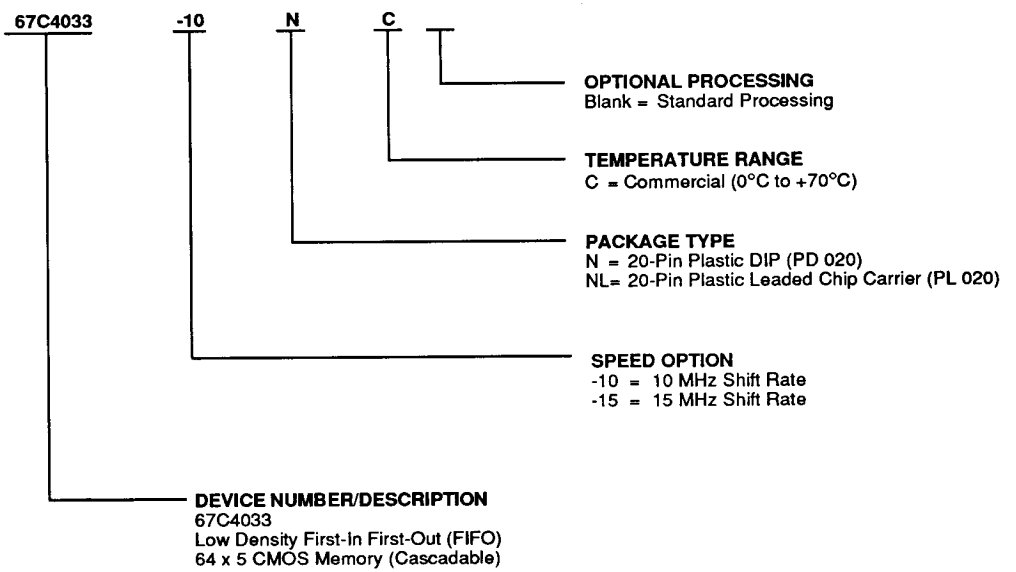
LOGIC SYMBOL



10684B-4

ORDERING INFORMATION
Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:



Valid Combinations	
67C4033-10	N, NL
67C4033-15	

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage V_{CC} . . . . . −0.5 V to +7.0 V
Input Voltage . . . . . −1.5 V to +7.0 V
Off-State Output Voltage . . . . . −0.5 to V_{CC} +0.5 V
Storage Temperature . . . . . −65°C to +150°C
Power Dissipation . . . . . 1.0 W
Latch-Up Trigger Current, All Outputs . . . . . 140 mA

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. This is a stress rating only; functional operation of the device at these limits or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure of the device to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices

Ambient Temperature (T_A)
Operating in Free Air . . . . . 0°C to +70°C

Supply Voltage (V_{CC})
With Respect to Ground . . . . . +4.5 V to +5.5 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

OPERATING CONDITIONS, Commercial

Parameter Symbol	Parameter Description	Figure	-10		-15		Unit
			Min.	Max.	Min.	Max.	
f_{IN}	Shift In Rate	1		10		15	MHz
t_{SIH}	Shift In High Time	1, B	16		16		ns
t_{SIL}	Shift In Low Time	1	30		30		ns
t_{IDS}	Input Data Setup to SI (Shift In)	1	0		0		ns
t_{IDH}	Input Data Hold Time from SI (Shift In)	1	40		40		ns
t_{RIDS}	Input Data Setup to IR (Input Ready)	3	0		0		ns
t_{RIDH}	Input Data Hold Time from IR (Input Ready)	3	30		30		ns
f_{OUT}	Shift Out Rate	4		10		15	MHz
t_{SOH}	Shift Out High Time	4, B	24		21		ns
t_{SOL}	Shift Out Low Time	4	30		30		ns
t_{MRW}*	Master Reset Pulse	8	35		35		ns
t_{MRS}	Master Reset to SI	8	65		65		ns

*See AC test and high-speed application note.

DC CHARACTERISTICS over COMMERCIAL operating range unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions		-10		-15		Unit
				Min.	Max.	Min.	Max.	
V_{IL}*	Low-Level Input Voltage				0.8		0.8	V
V_{IH}*	High-Level Input Voltage			2		2		V
I_{IN}	Input Current	V_{CC} = Max GND<V_{IN}<V_{CC}		–1	1	–1	1	µA
I_{OZ}	Off-State Output Current	V_{CC} = Max GND<V_{OUT}<V_{CC}		–5	5	–5	5	µA
V_{OL}	Low-Level Output Voltage	V_{CC} = Min	I_{OL} = 20 µA		0.1		0.1	V
			I_{OL} = 8 mA		0.4		0.4	V
V_{OH}	High-Level Output Voltage	V_{CC} = Min	I_{OH} = 20 µA	V_{CC} – 0.1		V_{CC} – 0.1		V
			I_{OH} = –4 mA	2.4		2.4		V
I_{OS}**	Output Short-Circuit Current	V_{CC} = Max	V_O = 0 V	–90	–20	–90	–20	mA
I_{CC}	Standby Supply Current	V_{CC} = Max I_{OUT} = 0	V_{IH} = V_{CC} V_{IL} = GND		100		100	µA
	Operating Supply Current		V_{IH} = Min, V_{IL} = Max f_{IN} = f_{OUT} = Max		35		45	mA

* V_{IL} and V_{IH} are input conditions of output tests and are not themselves directly tested. V_{IL} and V_{IH} are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

** Not more than one output should be shortened at a time, and duration of the short circuit should not exceed one second.

SWITCHING CHARACTERISTICS over COMMERCIAL operating range unless otherwise specified

Parameter Symbol	Parameter Description	Figure	-10		-15		Unit
			Min.	Max.	Min.	Max.	
t_{IRL}*	Shift in ↑ to Input Ready Low	1		60		55	ns
t_{IRH}*	Shift in ↓ to Input Ready HIGH			55		55	ns
t_{ORL}*	Shift Out ↑ to Output Ready LOW	4		55		47	ns
t_{ORH}*	Shift Out ↓ to Output Ready HIGH			50		47	ns
t_{ODH}	Output Data Hold (previous word)		5		5		ns
t_{ODS}	Output Data Shift (next word)			35		33	ns
t_{PT}	Data throughput	3, 6		100		90	ns
t_{MRORL}	Master Reset ↓ to Output Ready LOW	8		100		100	ns
t_{MRIRH}	Master Reset ↓ to Input Ready HIGH			100		100	ns
t_{MRO}	Master Reset ↓ to Outputs LOW			35		35	ns
t_{MRHFL}	Master Reset ↓ to Half-Full Flag LOW	9		100		100	ns
t_{MRAEH}	Master Reset ↓ to Almost Empty Flag HIGH			100		100	ns
t_{IPH}	Input Ready pulse HIGH	3, B	19		16		ns
t_{OPH}	Output Ready pulse HIGH	6, B	14		14		ns
t_{ORD}	Output Ready ↑ to Data Valid	4		–3		–3	ns
t_{AEH}	Shift Out ↑ to AF/E HIGH	10		110		110	ns
t_{AEL}	Shift Out ↑ to AF/E LOW			110		110	ns
t_{AFL}	Shift Out ↑ to AF/E LOW	11		110		110	ns
t_{AFH}	Shift Out ↑ to AF/E HIGH			110		110	ns
t_{HFH}	Shift In ↑ to HF HIGH	12		110		110	ns
t_{HFL}	Shift Out ↑ to HF LOW			110		110	ns
t_{PHZ}	Output Disable Delay	A		25		25	ns
t_{PLZ}**				25		25	ns
t_{PZL}**	Output Enable Delay	A		30		30	ns
t_{PZH}**				30		30	ns

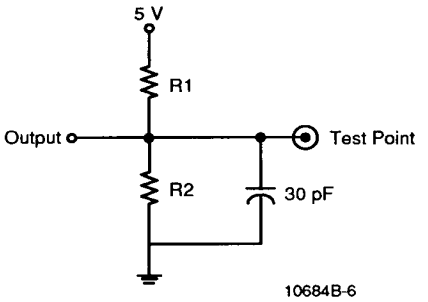
*See timing diagram for explanation of parameters.

CAPACITANCES*

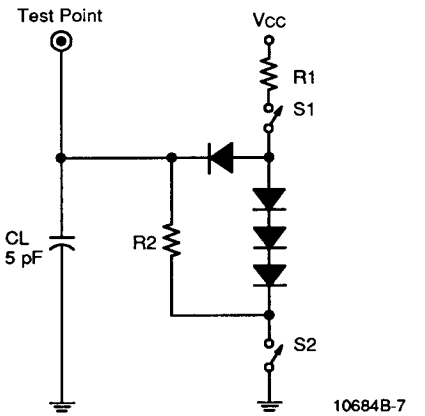
Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
C_{IN}	Input capacitance	T_A = 25°C, f = 1 MHz		10	pF
C_{OUT}	Output capacitance	V_{CC} = 4.5 V		7	

* These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

AC TEST LOADS AND CONDITIONS



Standard AC Test Load



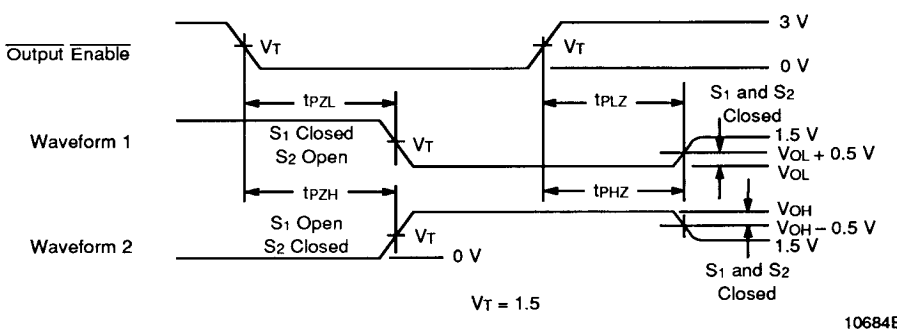
Three-State Test Load

Resistor Values

I_{OL}	R1	R2
8 mA	600 Ω	1200 Ω

Input Pulse Amplitude = 3 V
Input Rise and Fall Time (10% – 90%) = 2.5 ns
Measurements made at 1.5 V
All Diodes are 1N916 or 1N3064

ENABLE AND DISABLE



Waveform 1 is for a data output with internal conditions such that the output is low except when disabled by the output control.
Waveform 2 is for a data output with internal conditions such that the output is high except when disabled by the output control.

Figure A.

FUNCTIONAL DESCRIPTION

Data Input

The FIFO consists of a dual-port RAM and two ring counters for read and write. After power-up, the Master Reset should be pulsed LOW, which internally rests both the read and write counters. When the Ready (IR) is HIGH, the FIFO is ready to accept DATA from the Dx inputs. Data then present at the inputs is written into the first location of the RAM when Shift-In (SI) is brought HIGH. A SI HIGH signal causes the IR to go LOW. When the SI is brought LOW and the FIFO is not full, IR will go HIGH, indicating that more room is available. The write pointer now points to the next location in the RAM. If the memory is full, then the IR will remain LOW.

Data Output

Data is read from Ox outputs. Just after the first shift-in, the first data word is available at the outputs, which is indicated by the Output Ready (OR) going HIGH. When the OR is HIGH, data may be shifted out by bringing the Shift-Out (SO) HIGH. A HIGH signal at SO causes the read pointer to point to the next location in the RAM, and also the OR to go LOW. Valid data is maintained while the SO is HIGH. When the SO is brought LOW, the OR goes HIGH, indicating the presence of new valid data. If the FIFO is emptied, OR stays LOW, and Ox remains as before, (i.e., data does not change if the FIFO is empty). A dual-port RAM inside the chip provides the capability of simultaneous and asynchronous write (Shift-Ins) and reads (Shift-Outs).

AC TEST AND HIGH-SPEED APPLICATION NOTES

Since the FIFO is a very-high-speed device, care must be exercised in the design of the hardware and the timing utilized within the design. Device grounding and decoupling is crucial to correct operation as the FIFO will respond to very small glitches due to long reflective lines, high capacitances and/or poor supply decoupling and grounding. Advanced Micro Devices recommends a monolithic ceramic capacitor of 0.1 µF directly between Vcc and GND with very short lead length. In addition, care must be exercised in how the timing is set up and how the parameters are measured. For example, since an AND gate function is associated with both the Shift-In – Input Ready combination, as well as Shift-Out – Output Ready combination, timing measurements may be misleading; i.e., a rising edge of the Shift-In pulse is not recognized until Input Ready is HIGH. If Input Ready is not HIGH due to (a) too high a frequency, or (b) FIFO being full or affected by Master Reset, the Shift-In activity will be ignored. This will affect the device from a functional standpoint, and will also cause the "effective" timing of Input Data Hold time (t_{IDH}) and the next activity of Input Ready (t_{IRL}) to be extended relative to Shift-In going HIGH. The same type of problem also relates to t_{IRH}, t_{ORL} and the Status Flag timing as related to Shift-In and Shift-Out. For high speed applications, proper grounding technique is essential.

HF AND AFE STATUS FLAGS

The Half-Full (HF) will be high only when the net balance of word shifted into the FIFO exceeds the number of words shifted out by thirty-two or more (i.e., when the FIFO contains thirty-two or more words). The Almost-Full/Empty (AFE) flag will be HIGH when the FIFO contains fifty-six or more words or when the FIFO contains eight or fewer words (see Figures 9, 10, and 11).

Care should be exercised in using the status flags because they are capable of producing arbitrarily short pulses. For example, if the FIFO contains thirty-one words, and SI and SO pulses are applied simultaneously, the HF flag may produce an arbitrarily short pulse, depending on the precise phase of SI and SO.

The flags will always settle to the correct state after the appropriate delay (e.g., t_{HFL}, t_{HFH} in this example). This property of the status flags will clearly be a function of the dynamic relation between SI and SO. Generally, the use of level-sensitive, rather than edge-sensitive, status detection circuits will alleviate this hazard.

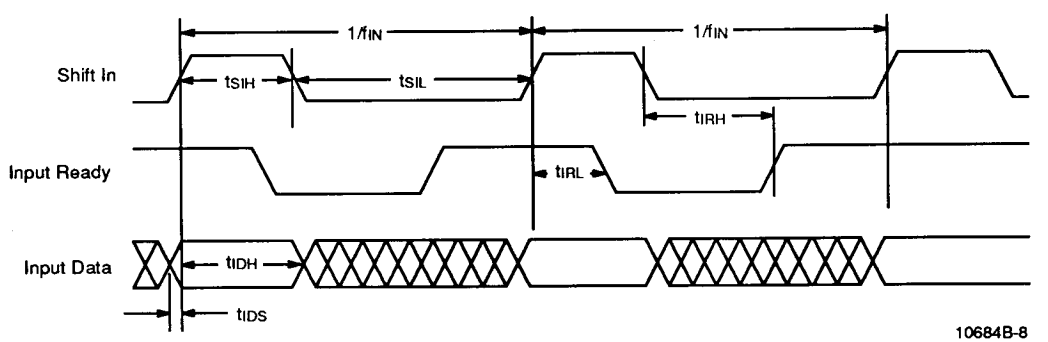
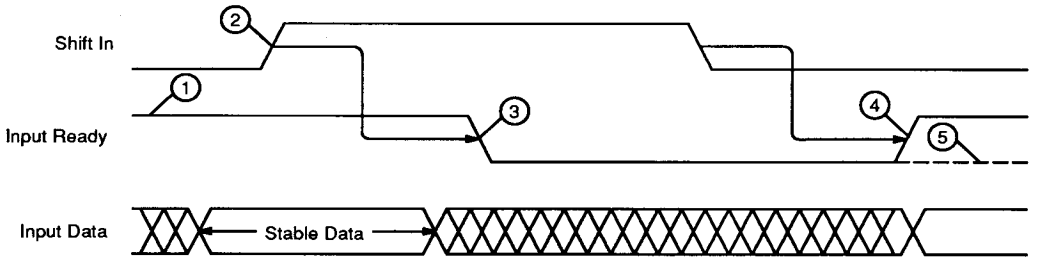
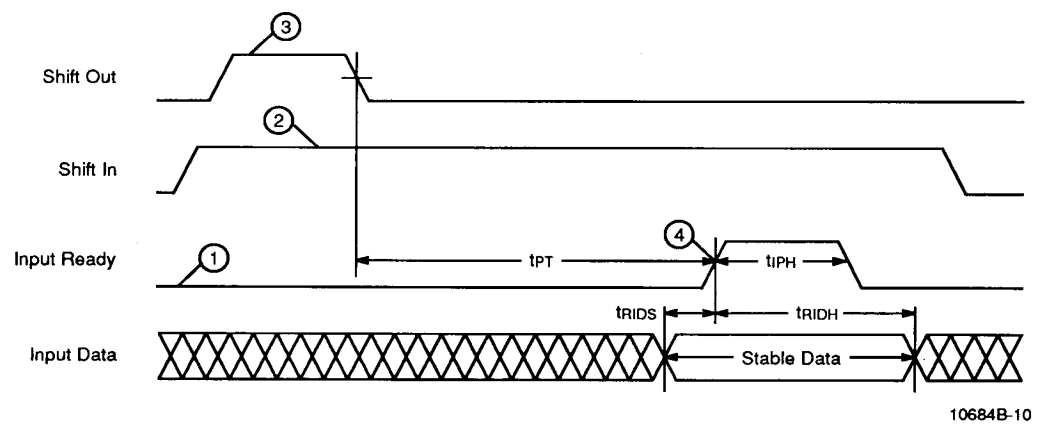


Figure 1. Input Timing



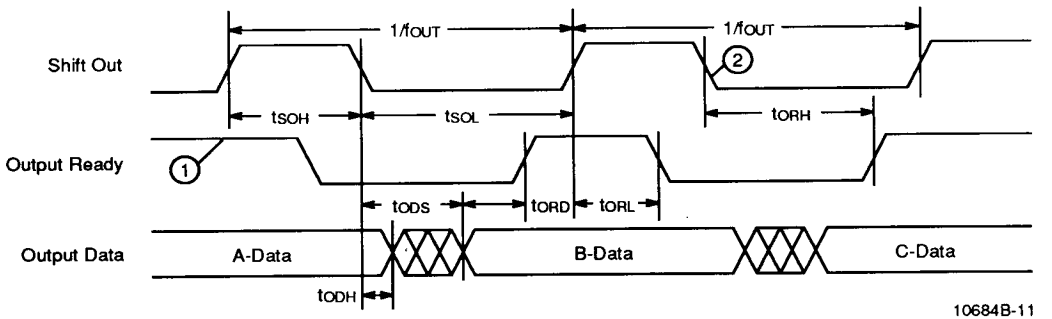
1. Input Ready HIGH indicates space is available and a Shift-in pulse may be applied.
2. Input Data is loaded into the first available memory location.
3. Input Ready goes LOW indicating this memory location is full.
4. Shift-In going LOW allows Input Ready to sense the status of the next memory location. The next memory location is empty as indicated by Input Ready HIGH.
5. If the FIFO is already full then the Input Ready remains LOW.
   Note: Shift-In pulses applied while Input Ready is LOW will be ignored.

Figure 2. The Mechanism of Shifting Data into the FIFO



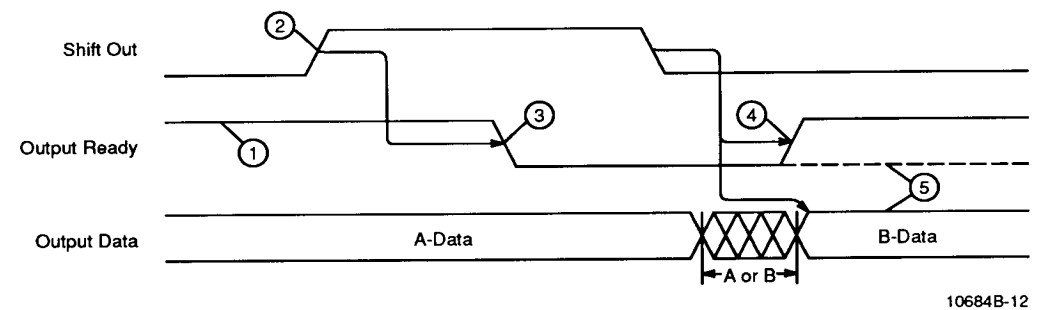
1. FIFO is initially full.
2. Shift-In is held HIGH.
3. Shift-Out pulse is applied. An empty location is detected by the internal pointers on the falling edge of SO.
4. As soon as Input Ready becomes HIGH, the Input Data is loaded into this location.

Figure 3. Data is shifted in whenever Shift-In and Input Ready are Both HIGH



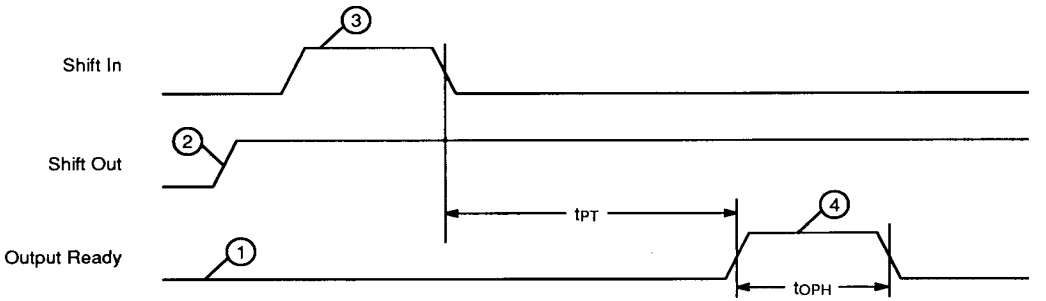
1. The diagram assumes that the FIFO contains at least three words: A-Data (first input word), B-Data (second input word), and C-Data (third input word).
2. Output data changes on the falling edge of SO after a valid Shift-Out Sequence, i.e., OR and SO are both high together.

Figure 4. Output Timing



1. Output Ready HIGH indicates that data is available and a Shift-Out pulse may be applied.
2. Shift-Out goes HIGH causing B-Data (second input word) to advance to the output register. Output data remains as valid A-Data while Shift-Out is HIGH.
3. Output Ready goes LOW.
4. Shift-Out goes LOW causing Output Ready to go HIGH and new data (B) to appear at the data outputs.
5. If the FIFO has only one word loaded (A-Data) then Output Ready stays LOW and the output data remains the same (A-Data).

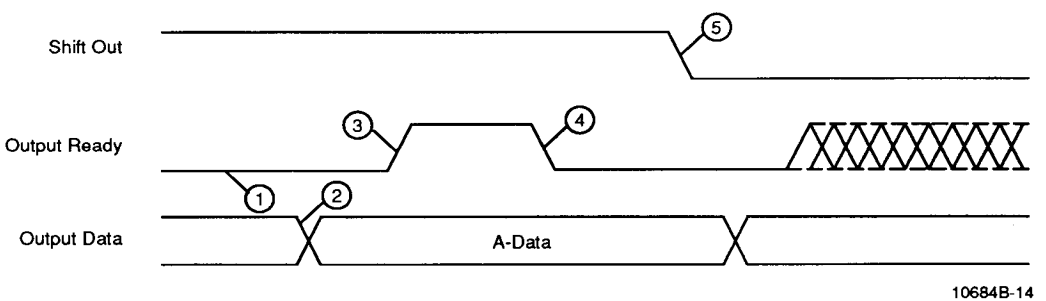
Figure 5. The Mechanism of Shifting Data Out of the FIFO



10684B-13

1. FIFO initially empty.
2. Shift-Out held HIGH.
3. Shift-In pulse applied. A full location is detected by the internal pointers on the falling edge of Shift-In.
4. As soon as Output Ready becomes HIGH, the word is shifted out.

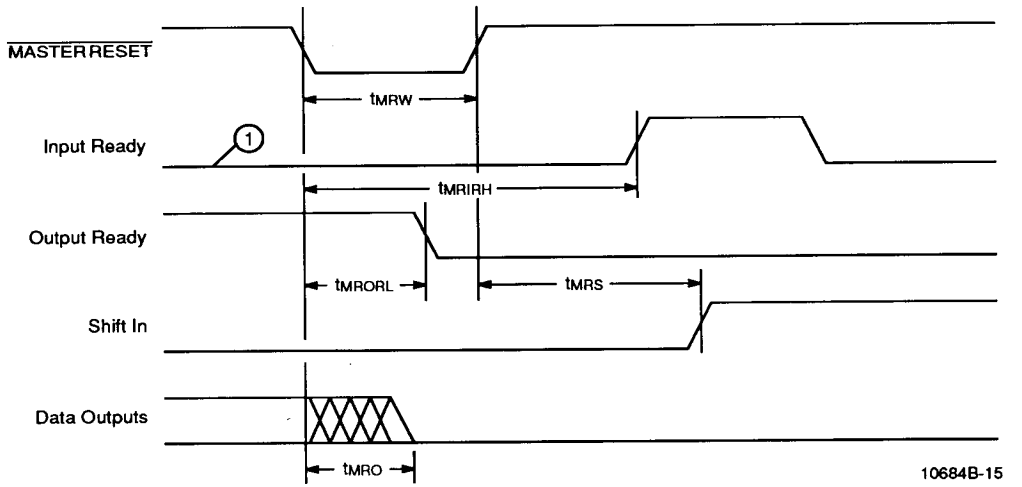
Figure 6. t_{PT} and t_{OPH} Specification



10684B-14

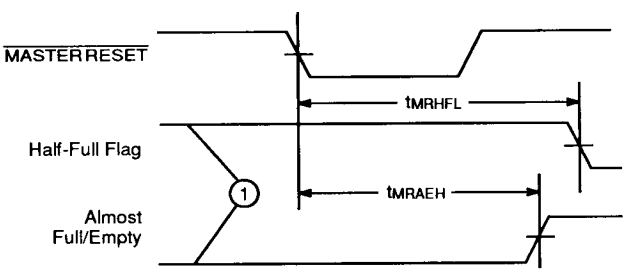
1. The internal logic does not detect the presence of any words in the FIFO.
2. New data (A) arrives at the outputs.
3. Output Ready goes HIGH indicating arrival of the new data.
4. Since Shift-Out is held HIGH, Output Ready goes immediately LOW.
5. As soon as Shift-Out goes LOW, the Output Data is subject to change. Output Ready will go HIGH or remain LOW depending on whether there are any additional upstream words in the FIFO.

Figure 7. Data is Shifted Out Whenever Shift Out and Output Ready are Both HIGH



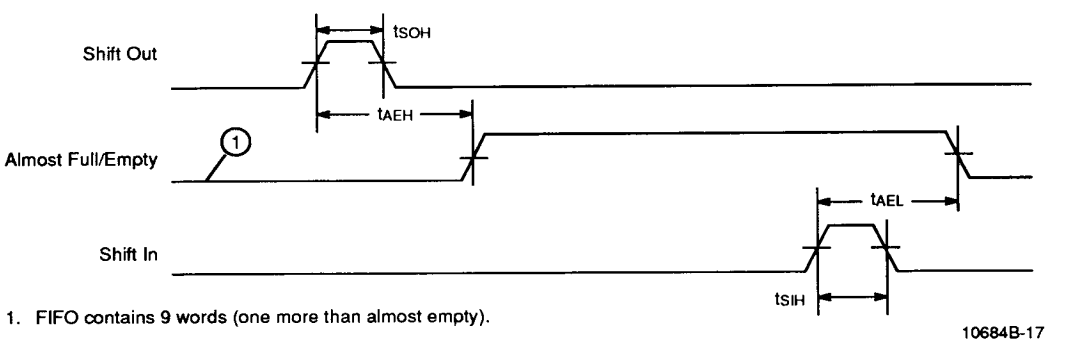
1. FIFO is initially full.

Figure 8. Master Reset Timing



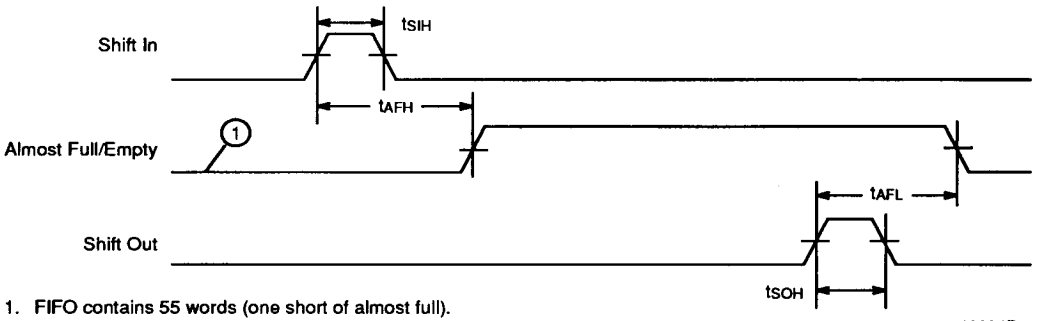
1. FIFO initially has between 32 and 56 words.

Figure 9. t_{MRHFL}, t_{MRAEH} Specifications



1. FIFO contains 9 words (one more than almost empty).

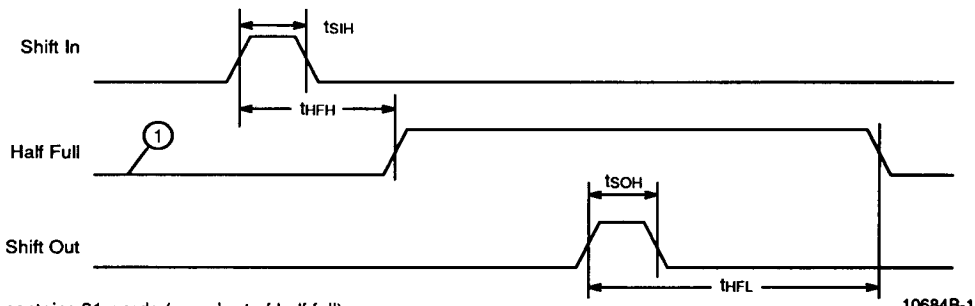
Figure 10. t_{AEH}, t_{AEL} Specifications



1. FIFO contains 55 words (one short of almost full).

10684B-18

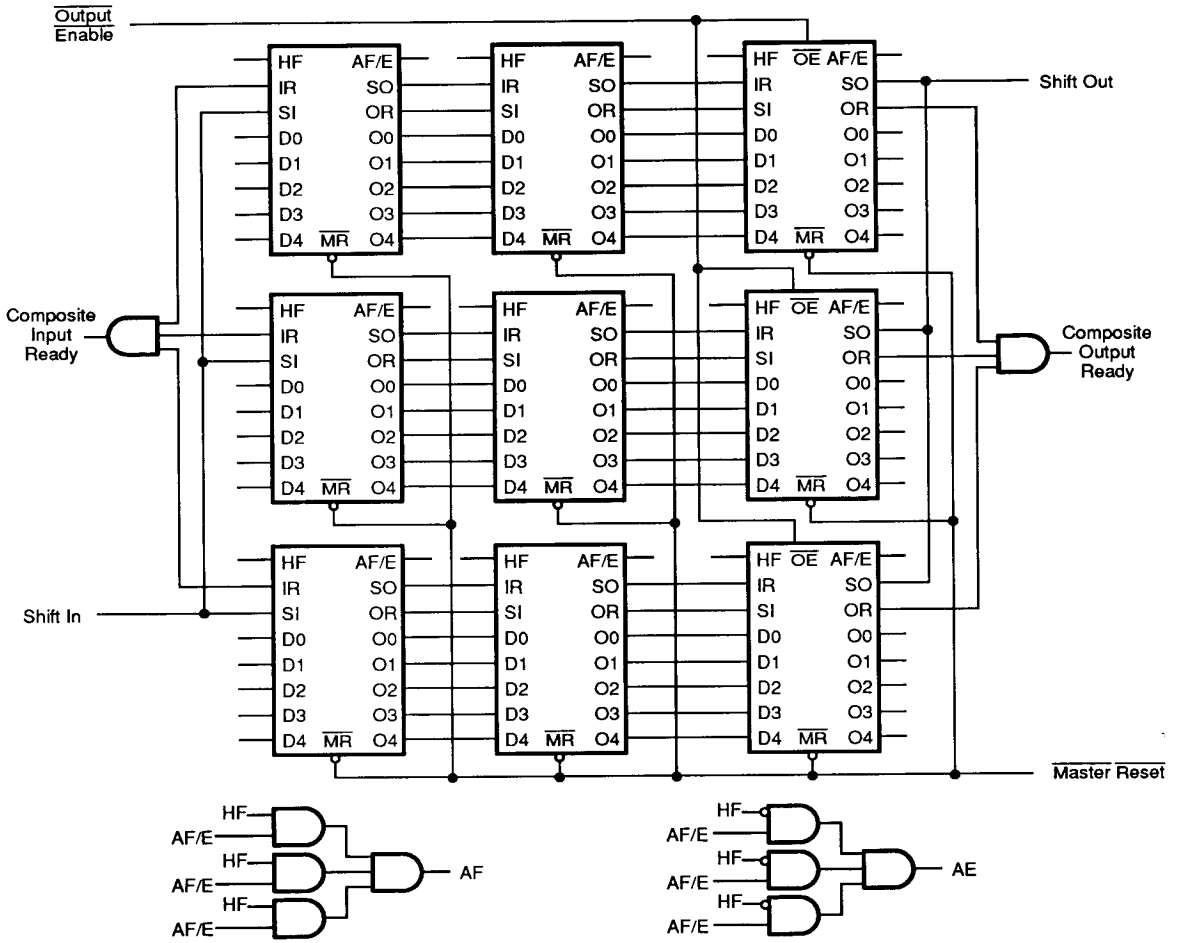
Figure 11. t_{AFH}, t_{AFL} Specifications



1. FIFO contains 31 words (one short of half full).

10684B-19

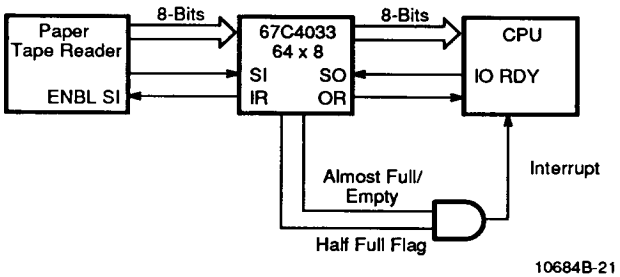
Figure 12. t_{HFL}, t_{HFH} Specifications



Almost Full (AF) is eight words or less to FIFO full.
Almost Empty (AE) is eight words or less to FIFO empty.

10684B-20

Figure 13. 192 x 15 FIFO



Note: Expanding the FIFOs in word width is done by ANDing the IR and OR as shown in Figure 13.

Figure 14. Application for 67C4033 "Slow and Steady Rate to Fast *Blocked Rate*"

I_{CC} vs. Frequency