67C4500-35/50/65/80

Deep First-in First-out (FIFO)
256x9 CMOS Memory

DISTINCTIVE CHARACTERISTICS

- RAM based FIFO
- 256x9 organization
- Cycle times of 45/65/80/100 nanoseconds
- Asynchronous and simultaneous writes and reads
- Low power consumption — 60 mA maximum
- Status flags - full, half-full, empty

- Retransmit capability
- Expandable in both width and depth
- Increased noise immunity for $\overline{XI}$ - CMOS threshold
- Functional and pin compatible with industry standard devices

GENERAL DESCRIPTION

The 67C4500 is a RAM-based CMOS FIFO that is 256 words deep with 9-bit wide words. It is expandable to any width and/or depth to create much larger FIFOs.

This FIFO can accept data and output data asynchronously and simultaneously at data rates from 0 to 22 MHz. Status flags are provided to signify empty, full, and half-full conditions. The capability also exists to retransmit data from the FIFO.

Deep FIFOs such as the 67C4500 are useful in a wide range of applications. The ability to buffer large transfers of data and the rate adaption capabilities make the 67C4500 useful in communication, image processing, mass storage, DSP, and printing systems.
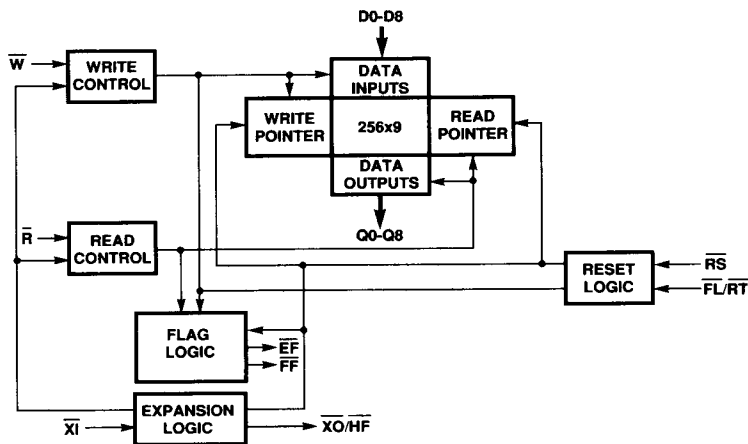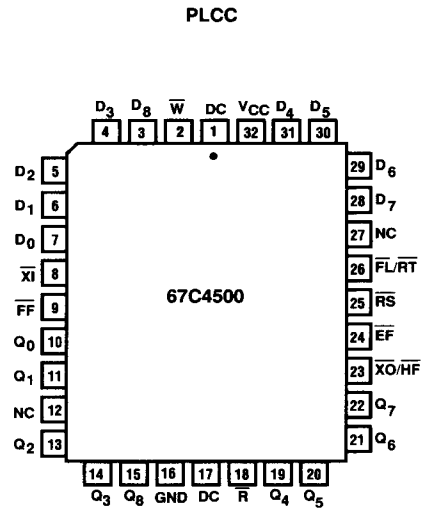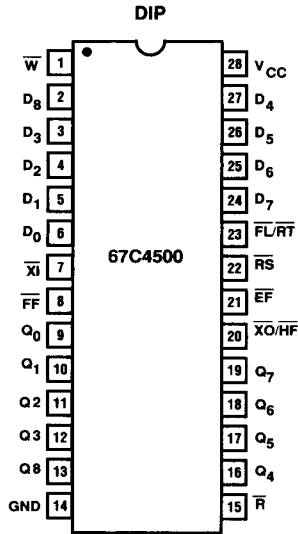
BLOCK DIAGRAM

Figure 1.

Advanced Micro Devices

CONNECTION DIAGRAMS

DIP


```
  W̄ [1]        [28] V_CC
 D_8 [2]       [27] D_4
 D_3 [3]       [26] D_5
 D_2 [4]       [25] D_6
 D_1 [5]       [24] D_7
 D_0 [6]       [23] FL/RT
  X̄Ī [7]  67C4500  [22] R̄S̄
  F̄F̄ [8]       [21] ĒF̄
 Q_0 [9]       [20] X̄Ō/H̄F̄
 Q_1 [10]      [19] Q_7
 Q_2 [11]      [18] Q_6
 Q_3 [12]      [17] Q_5
 Q_8 [13]      [16] Q_4
 GND [14]      [15] R̄
```

PLCC


```
        D_3 D_8 W̄ DC V_CC D_4 D_5
         [4][3][2][1][32][31][30]
 D_2 [5]                    [29] D_6
 D_1 [6]                    [28] D_7
 D_0 [7]                    [27] NC
  X̄Ī [8]      67C4500       [26] FL/RT
  F̄F̄ [9]                    [25] R̄S̄
 Q_0 [10]                   [24] ĒF̄
 Q_1 [11]                   [23] X̄Ō/H̄F̄
 NC [12]                    [22] Q_7
 Q_2 [13]                   [21] Q_6
         [14][15][16][17][18][19][20]
          Q_3 Q_8 GND DC R̄ Q_4 Q_5
```

Note: Pin 1 is marked for orientation.

Pin Designations:
W̄ = Write
R̄ = Read
R̄S̄ = Reset
F̄L̄/R̄T̄ = First Load/Retransmit
D_x = Data In
Q_x = Data Out
X̄Ī = Expansion In
X̄Ō/H̄F̄ = Expansion Out/Half-Full Flag
F̄F̄ = Full Flag
ĒF̄ = Empty Flag
V_{cc} = Supply Voltage
GND = Ground

ORDERING INFORMATION

Standard Products

AMD/MMI standard products are available in several packages. The order number (Valid Combination) is formed by a combination of:
a. Device Number
b. Speed Option
c. Operating Conditions
d. Package Type

67 C 4500 - 35 N

c. OPERATING CONDITIONS
67 = Commercial (0°C to 70°C)

CMOS TECHNOLOGY

a. PART NUMBER

b. PERFORMANCE
35 ns = 35 ns t_A
50 ns = 50 ns t_A
65 ns = 65 ns t_A
80 ns = 80 ns t_A

d. PACKAGE TYPE
N = Plastic DIP
J = Ceramic DIP
NL = Plastic Leaded Chip Carrier

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ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{CC} .... -0.5 V to + 7.0 V
Input voltage .... -0.5 V to V_{CC} + 0.5 V
Operating temperature .... 0°C to + 70°C
Storage temperature .... -55°C to + 150°C
Power dissipation .... 1.0 W
DC output current .... 50 mA

Stresses above those listed under ABSOLUTE MAXIMUM RAT-INGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

DC CHARACTERISTICS Commercial: V_{CC} = 5 V ± 10%, T_A = 0°C to + 70°C

Parameter Symbol	Parameter Description	67C4500-35 T_A = 35 ns Min.	Max.	67C4500-50 T_A = 50 ns Min.	Max.	67C4500-65 T_A = 65 ns Min.	Max.	67C4500-80 T_A = 80 ns Min.	Max.	Unit
I_{IL}	Input Leakage Current (any input) (Note 1)	-1	1	-1	1	-1	1	-1	1	µA
I_{IO}	Output Leakage Current (data outputs) (Note 2)	-10	10	-10	10	-10	10	-10	10	µA
V_{IH}	Input High Voltage (all inputs except $\overline{XI}$) (Note 3)	2.0	–	2.0	–	2.0	–	2.0	–	V
V_{IL}	Input Low Voltage (all inputs except $\overline{XI}$) (Note 3)	–	0.8	–	0.8	–	0.8	–	0.8	V
V_{IHXI}	Input High Voltage, $\overline{XI}$ (Note 3)	3.5	–	3.5	–	3.5	–	3.5	–	V
V_{ILXI}	Input Low Voltage, $\overline{XI}$ (Note 3)	–	1.5	–	1.5	–	1.5	–	1.5	V
V_{OH}	Output Logic "1" Voltage I_{OH} = -2 mA	2.4	–	2.4	–	2.4	–	2.4	–	V
V_{OL}	Output Logic "0" voltage I_{OL} = 8 mA	–	0.4	–	0.4	–	0.4	–	0.4	V
I_{CC1}	Average V_{CC} Power Supply Current (Note 4)	–	60	–	60	–	60	–	60	mA
I_{CC2}	Average Standby Current ($\overline{R} = \overline{W} = \overline{RS} = \overline{FL/RT}$ = V_{IH}) (Note 4)	–	20	–	20	–	20	–	20	mA
I_{CC3}	Power Down Current (all inputs = V_{CC} -0.2 V) (Note 4)	–	5	–	5	–	5	–	5	mA

Notes: 1. Measurements with GND ≤ V_{IN} ≤ V_{CC}.
2. $\overline{R}$ ≥ V_{IH}, GND ≤ V_{OUT} ≤ V_{CC}.
3. These are absolute voltage levels with respect to the ground pins on the device and include all overshoots due to system or tester noise. Do not attempt to test these values without suitable equipment.
4. I_{CC} measurements are made with outputs open.

AC CHARACTERISTICS VCC = 5 V ± 10%, TA = 0°C to + 70°C

Parameter Symbol	Parameter Description	Figures	67C4500-35 Min. Max.		67C4500-50 Min. Max.		67C4500-65 Min. Max.		67C4500-80 Min. Max.		Unit
Write and Flag Timing											
t_{WC}	Write Cycle Time	3	45		65		80		100		ns
t_{WPW}	Write Pulse Width	3	35		50		65		80		ns
t_{WR}	Write Recovery Time	3	10		15		15		20		ns
t_{DS}	Data Setup Time	3,9	25		30		30		40		ns
t_{DH}	Data Hold Time	3,9	0		5		10		10		ns
t_{WFF}	Write LOW to Full Flag LOW	6,9		30		45		60		60	ns
t_{WHF}	Write LOW to Half-Full Flag LOW	5		45		65		80		100	ns
t_{WEF}	Write HIGH to Empty Flag HIGH	4,8		30		45		60		60	ns
t_{WLZ}	Write pulse HIGH to data bus at LOW Z (Note 1)	8	10		15		15		20		ns
Read and Flag Timing											
t_{RC}	Read Cycle Time	3	45		65		80		100		ns
t_{A}	Access Time	3,4,8,9		35		50		65		80	ns
t_{RR}	Read Recovery Time	3	10		15		15		20		ns
t_{RPW}	Read Pulse Width	3	35		50		65		80		ns
t_{RLZ}	Read pulse LOW to data bus at LOW Z (Note 1)	3	5		10		10		10		ns
t_{DV}	Data Valid from read pulse HIGH	3	5		5		5		5		ns
t_{RHZ}	Read pulse HIGH to data bus at HIGH Z (Note 1)	3		20		30		30		30	ns
t_{RFF}	Read HIGH to Full Flag HIGH	6,9		30		45		60		60	ns
t_{RHF}	Read HIGH to Half Full-Flag HIGH	5		45		65		80		100	ns
t_{REF}	Read LOW to Empty Flag LOW	4,8		30		45		60		60	ns
Reset Timing											
t_{RSC}	Reset Cycle Time	2	45		65		80		100		ns
t_{RS}	Reset Pulse Width	2	35		50		65		80		ns
t_{RSS}	Reset Setup Time	2	35		50		65		80		ns
t_{RSR}	Reset Recovery Time	2	10		15		15		20		ns
t_{EFL}	Reset to Empty Flag LOW	2		45		65		80		100	ns
t_{HFH}	Reset to Half-Full Flag High	2		45		65		80		100	ns
t_{FFH}	Reset to Full Flag HIGH	2		45		65		80		100	ns
Retransmit Timing											
t_{RTC}	Retransmit Cycle Time	7	45		65		80		100		ns
t_{RT}	Retransmit Pulse Width	7	35		50		65		80		ns
t_{RTR}	Retransmit Recovery Time	7	10		15		15		20		ns

Note: 1. Characterized parameters.

FUNCTIONAL DESCRIPTION

The 67C4500 CMOS FIFO is designed around a 256x9 dual-port static RAM array. (See Figure 1.) RAM-based FIFOs store the data written into them in a sequential pattern.

The dual-port RAM array has dedicated write and read address pointers. The flag logic prevents illogical writes and reads from occurring. The Empty Flag prevents reading while empty, which is a data underflow condition, while the Full Flag prevents writing while full, which is a data overflow condition. Once data that has been stored at a given address is read, it can be overwritten.

Address pointers automatically overflow to address zero after reaching address 255. Thus the flag status of the FIFO is a function of the difference between the pointers, not their absolute value.

Resetting the FIFO simply initializes both address pointers to address zero. Pulsing Retransmit initializes the read address pointer to zero without affecting the write address pointer.

Expansion Logic is used when implementing a FIFO of a depth greater than that of the 67C4500. The write, read, data-in and data-out lines of the 67C4500 are connected in parallel, and the Expansion-Out ($\overline{XO}$) and the Expansion-In ($\overline{XI}$) lines are daisy-chained together. The write and read control circuits of the individual FIFOs are automatically enabled and disabled through the handshake between $\overline{XO}$ and $\overline{XI}$.

OPERATIONAL DESCRIPTION

Resetting The FIFO

Upon power up, the FIFO must be initialized with a Reset cycle. (See Figure 2.) The states of $\overline{XI}$ and $\overline{FL}$ are used during the reset cycle to determine the FIFO's mode of operation, as shown in Tables 1 and 2. For a valid reset cycle to occur, both the Read ($\overline{R}$) and Write ($\overline{W}$) signals must be HIGH t_{RSS} prior to and t_{RSR} after the rising edge of Reset ($\overline{RS}$). The reset cycle initializes the FIFO to an empty condition, signified by the Empty Flag ($\overline{EF}$) being LOW, active, and both the Half-Full (HF) and Full Flag ($\overline{FF}$) being HIGH, inactive.
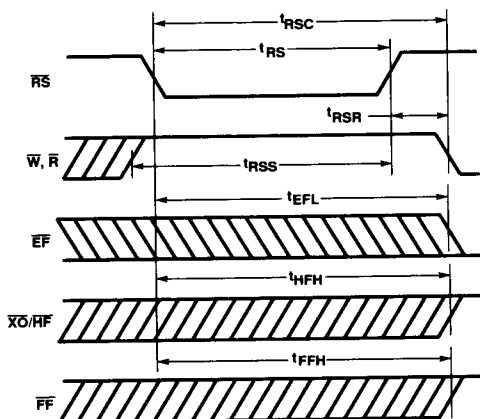

Figure 2. Reset Timing

Writing Data To The FIFO

The HIGH state of the Full Flag ($\overline{FF}$) indicates that the FIFO is capable of accepting data. The falling edge of Write ($\overline{W}$) initiates a write cycle. (See Figure 3.) Data appearing at inputs D0-D8 t_{DS} prior to and t_{DH} after the rising edge of $\overline{W}$ will be stored sequentially in the FIFO.

The LOW- to-HIGH transition of the Empty Flag ($\overline{EF}$) occurs t_{WEF} after the rising edge of $\overline{W}$ during the first write cycle on an empty FIFO. (See Figure 4.) The Half-Full Flag /HF) will go LOW t_{WHF} after the falling edge of $\overline{W}$ during the write operation which creates the half-full condition. (See Figure 5.) HF will remain LOW, while the number of writes to the FIFO exceeds the number of reads by 128 or more. The Half-Full Flag is not available in Depth-Expansion Mode. The Full Flag ($\overline{FF}$) goes LOW t_{WFF} after the falling edge of $\overline{W}$ during the write cycle which creates a full condition. (See Figure 6.) A full condition exists when there have been 256 more write cycles than read cycles. The Full Flag being active prohibits any further write operations, thus preventing data overflow situations.

Reading Data From The FIFO

The HIGH state of the Empty Flag ($\overline{EF}$) indicates that the FIFO is ready to output data. The falling edge of Read ($\overline{R}$) initiates a read cycle. (See Figure 3.) Valid data appears on the outputs Q0-Q8 t_A after the falling edge of $\overline{R}$, and remains until t_{DV} after the rising edge of $\overline{R}$. Q0-Q8 return to a high-impedance state when a valid read is not in progress.

The Full Flag ($\overline{FF}$) will go HIGH t_{RFF} after the rising edge of $\overline{R}$ during the first read cycle following a full condition. (See Figure 6.) The Half-Full Flag ($\overline{HF}$) will go HIGH t_{RHF} after the rising edge of $\overline{R}$ during the read operation, which eliminates the half-full condition. (See Figure 5). HF will remain HIGH, while the number of writes to the FIFO exceeds the number of reads by 127 or less. The Half-Full Flag is not available in Depth-Expansion Mode. The HIGH-to-LOW transition of $\overline{EF}$ occurs t_{REF} after the falling edge of $\overline{R}$ during the read cycle, which creates an empty condition. (See Figure 4.) An empty condition exists when there has been an equal number of write cycles and read cycles. The Empty Flag being active prohibits any further read operations, thus preventing a data underflow situation.

Half-Full Flag

The Half-Full ($\overline{HF}$) Flag will be active LOW only when the net balance of the words written into the FIFO exceeds the number of words read out by 128 or more. (See Figure 5.)

Care should be exercised in using the Half-Full Flag, because it is capable of producing arbitrarily short pulses. For example, if the FIFO contains 128 words, and Read and Write pulses are applied simultaneously, the $\overline{HF}$ flag may produce an arbitrarily short pulse, depending on the precise phase of Read and Write.

$\overline{HF}$ will always settle to the correct state after the appropriate delay, t_{WHF} or t_{RHF}. This property of the Half-Full Flag is clearly a function of the dynamic relation between $\overline{W}$ and $\overline{R}$. Generally, the use of level-sensitive, rather than edge-sensitive, status detection circuits will alleviate this hazard.

RESET AND RETRANSMIT TRUTH TABLE Single-Device Configuration/Width-Expansion Mode

Mode	Input			Internal Status		Outputs		
	$\overline{RS}$	$\overline{FL/RT}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$	$\overline{HF}$
Reset	0	X	0	Location zero	Location zero	0	1	1
Retransmit	1	0	0	Location zero	Unchanged	X (Note 1)	X (Note 1)	X (Note 1)
Read/Write	1	1	0	Increment (Note 2)	Increment (Note 2)	X	X	X

Notes: 1. Flags will change to show correct state according to write pointer.
2. Pointers will increment only if corresponding flag is HIGH at the beginning of the cycle.

Table 1.

RESET AND FIRST LOAD TRUTH TABLE Depth-Expansion/Compound-Expansion Mode

Mode	Input			Internal Status		Outputs	
	$\overline{RS}$	$\overline{FL/RT}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$
Reset–first device	0	0	$\overline{XO}$ (Note 1)	Location zero	Location zero	0	1
Reset all other devices	0	1	$\overline{XO}$ (Note 1)	Location zero	Location zero	0	1
Read/Write	1	X (Note 2)	$\overline{XO}$ (Note 1)	Increment (Note 3)	Increment (Note 3)	X	X

Notes: 1. $\overline{XI}$ is connected to $\overline{XO}$ of previous device. See Figure 12.
2. Same as during Reset Cycle.
3. Pointers will increment only if corresponding flag is HIGH at the beginning of the cycle.
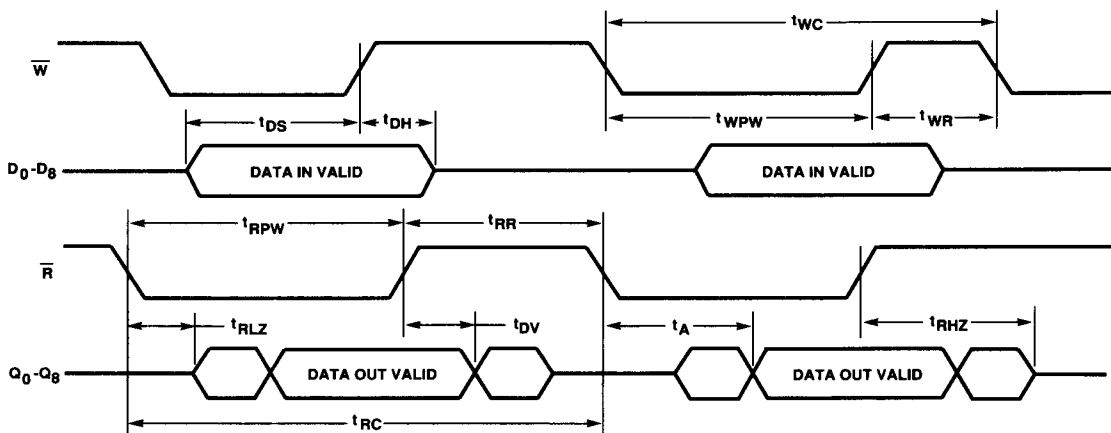
Table 2.

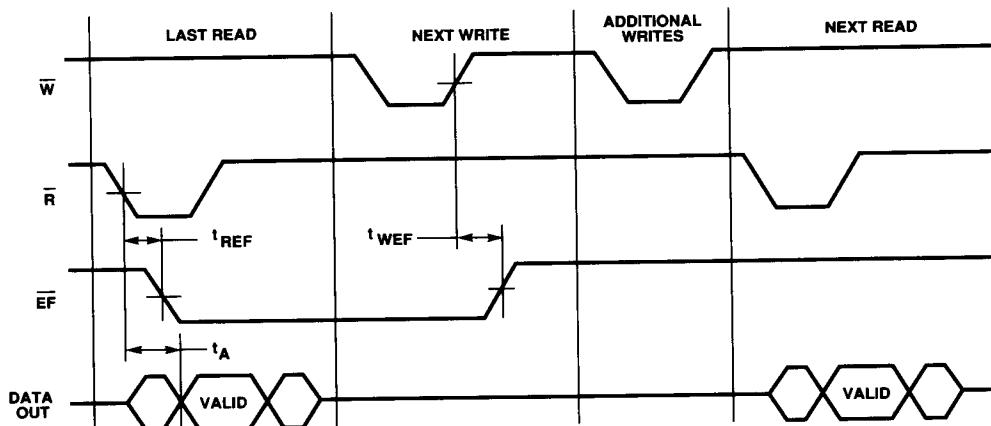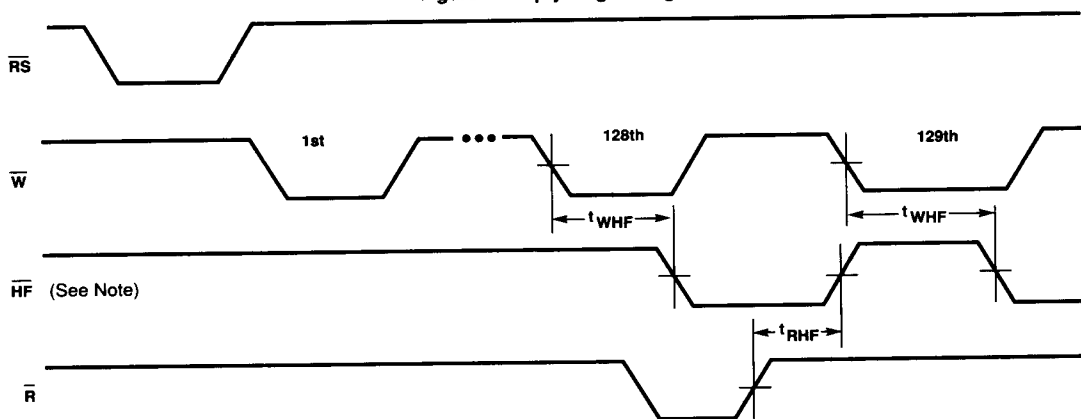**Figure 3. Asynchronous Write and Read Timing**

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Figure 4. Empty Flag Timing

Note: Depending on the precise phase of $\overline{W}$ and $\overline{R}$, the Half-Full Flag may appear as a pulse of arbitrarily short duration of either polarity when $\overline{W}$ and $\overline{R}$ are operating asynchronously near half full.
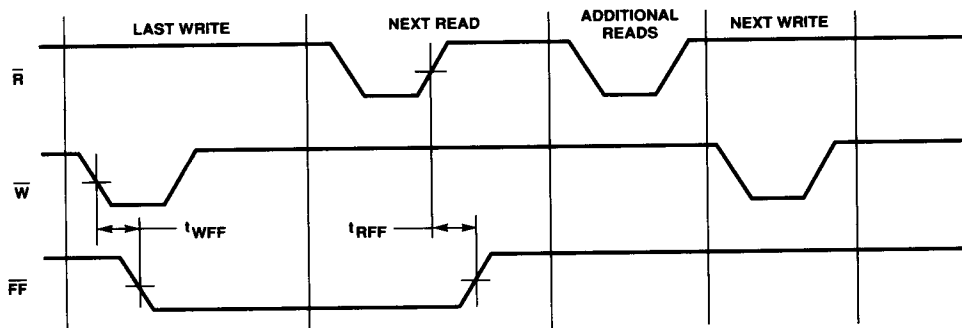
Figure 5. Half-Full Flag Timing

Figure 6. Full Flag Timing

Retransmit

The retransmit function resets the read address pointer allowing the data that was previously read to be read again. This capability is useful when the block of data being transferred through the FIFO doesn't exceed the FIFO's depth and is intended for use when there are 256 or less writes between reset cycles.

The $\overline{FL/RT}$ is used as the Retransmit ($\overline{RT}$) input in Single-Device Mode. $\overline{RT}$, an active LOW-going pulse of at least t_{RT} in duration, returns the internal read pointer to address zero and leaves the write pointer unaffected. $\overline{W}$ and $\overline{R}$ must both be HIGH during the retransmit cycle. The first write or read cycle should not start until t_{RTR} after the rising edge of $\overline{RT}$. The flags may change state during this cycle, but they will accurately reflect the new state of the FIFO t_{RTC} after the falling edge of $\overline{RT}$. (See Figure 7 and Table 1.)

Single-Device/Width-Expansion Modes

Single-Device and Width-Expansion Modes are configured by grounding the Expansion-In ($\overline{XI}$) input. (See Figures 10 and 11, and Table 1.) During these modes of operation, the Half-Full Flag and Retransmit features are available. The 67C4500 can be expanded in width to create FIFOs of word widths greater than nine bits. In Width-Expansion Mode all of the control line inputs are common to all devices. (See Figure 11.) Creating composite status flags can pose two hazards. 1.) OR-ing the flag outputs is fine for the HIGH-to-LOW transition, because the skew between devices is masked out. However, when the flags make a LOW-to-HIGH transition, a false composite flag is generated. 2.) The converse is true when the flags are AND-ed: the LOW-to-HIGH transition is fine, and the HIGH-to-LOW generates a false flag. These two hazards can be avoided if one device's flags are used as the flags for the expanded FIFO, and the write control circuitry and read control circuitry is designed to hold off sampling the flags until the worst case settling time (t_{WEF}, t_{WHF}, t_{WFF}, t_{REF}, t_{RHF}, and t_{WFF}) for each flag has elapsed.

Depth-Expansion Mode

Depth-Expansion Mode is configured during the Reset cycle. (See Figure 12 and Table 2.) Expansion Out ($\overline{XO}$) of one device must be connected to Expansion In ($\overline{XI}$) of the next device, with $\overline{XO}$ of the last device being connected to $\overline{XI}$ of the first device. The device that is to receive data first has its First Load ($\overline{FL}$) input tied LOW, while all other devices must have this input HIGH. Write and read control is passed between devices using $\overline{XO}$ and $\overline{XI}$. A LOW-going pulse on $\overline{XO}$ occurs when the last physical location of an active device, address 255, is written to, and another LOW-going pulse occurs when the last physical location of an active device is read. Only one device is enabled for writes, and only one device is enabled for reads at any given time.

When expanding in depth, a composite Full Flag must be created by OR-ing all the $\overline{FF}$ outputs together. Likewise, a composite Empty Flag is created by OR-ing all the $\overline{EF}$ outputs together. The Half-Full Flag and Retransmit functions are not available in Depth-Expansion Mode.

Compound Expansion

FIFOs of greater width and depth than the 67C4500 can be created by using both Width-Expansion Mode and Depth-Expansion Mode simultaneously. (See Figure 13.)
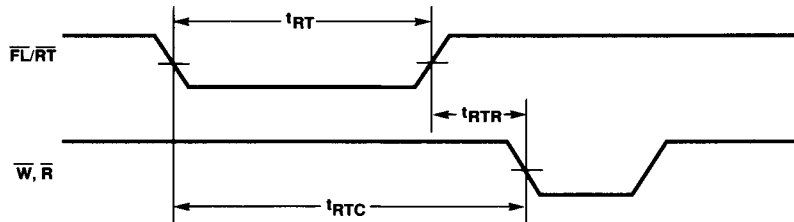
Note: $\overline{EF}$, $\overline{HF}$ and $\overline{FF}$ may change state during Retransmit as a result of the offset of the read and write pointers, but the flags will be valid at t_{RTC}.
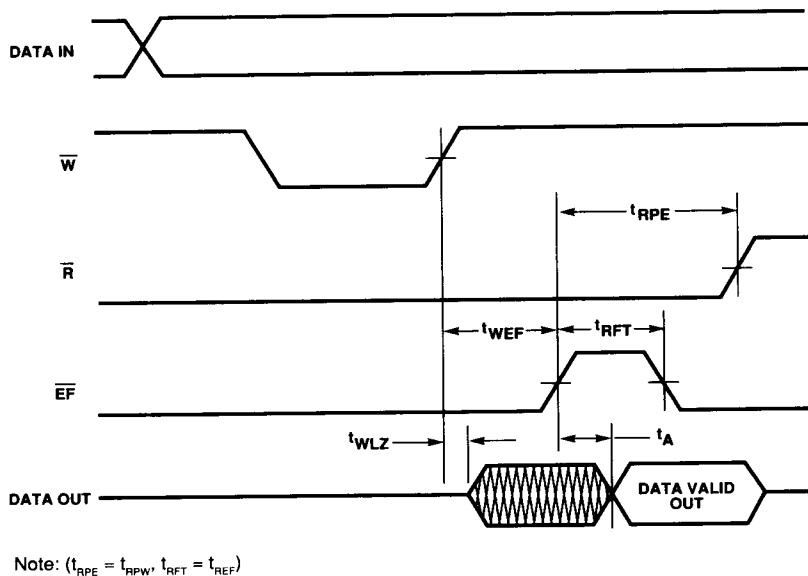
Figure 7. Retransmit Timing

DATA IN

$\overline{W}$

t_{RPE}

$\overline{R}$

t_{WEF} t_{RFT}

$\overline{EF}$

t_{WLZ} t_A

DATA OUT

DATA VALID
OUT

Note: $(t_{RPE} = t_{RPW}, t_{RFT} = t_{REF})$

Figure 8. Read Data Flow Through Mode

$\overline{R}$

$\overline{W}$

t_{RFF} t_{WPF}

$\overline{FF}$

t_{WFT} t_{DH}

DATA IN

DATA IN
VALID

t_A t_{DS}
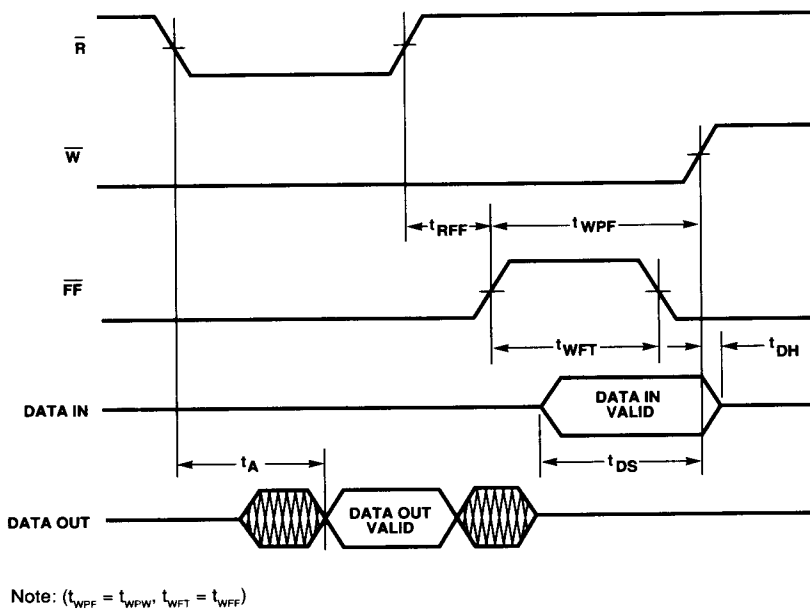
DATA OUT

DATA OUT
VALID

Note: $(t_{WPF} = t_{WPW}, t_{WFT} = t_{WFF})$

Figure 9. Write Data Flow Through Mode

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