Deep First-In First-Out (FIFO) 512x9 CMOS Memory 67C4501-25/35/50/65/80

Features

- **Ram-based FIFO**
- **512x9 organization**
- **Cycle times of 35/45/65/80/100 nanoseconds**
- **Asynchronous and simultaneous writes and reads**
- **Low power consumption**
  - **— 60 mA max, -35/55/65/80**
  - **— 70 mA max, -25**
- **Status flags - Full, Half-Full, Empty**
- **Retransmit capability**
- **Expandable in both width and depth**
- **Increased noise immunity for $\overline{XI}$ - CMOS threshold**
- **Functional and pin-compatible with industry standard devices**

General Description

The 67C4501 is a RAM-based CMOS FIFO that is 512 words deep with 9-bit wide words. It is expandable to any width and/or depth to create much larger FIFOs.

This FIFO can accept data and output data asynchronously and simultaneously at data rates from 0 to 28.5 MHz. Status flags are provided to signify empty, full, and half-full conditions. The capability also exists to retransmit data from the FIFO.

Deep FIFOs such as the 67C4501 are useful in a wide range of applications. The ability to buffer large transfers of data and the rate adaption capabilities make the 67C4501 useful in communication, image processing, mass storage, DSP, and printing systems.

Pin Names

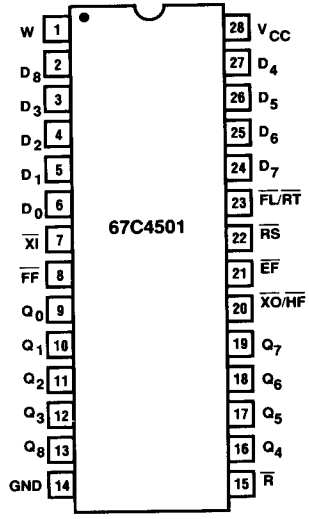
PIN NAME	DESIGNATION
$\overline{W}$	Write
$\overline{R}$	Read
$\overline{RS}$	Reset
$\overline{FL}/\overline{RT}$	First Load/Retransmit
D_X	Data In
Q_X	Data Out
$\overline{XI}$	Expansion In
$\overline{XO}/\overline{HF}$	Expansion Out/Half-Full Flag
$\overline{FF}$	Full Flag
$\overline{EF}$	Empty Flag
VCC	Supply Voltage
GND	Ground

Ordering Information

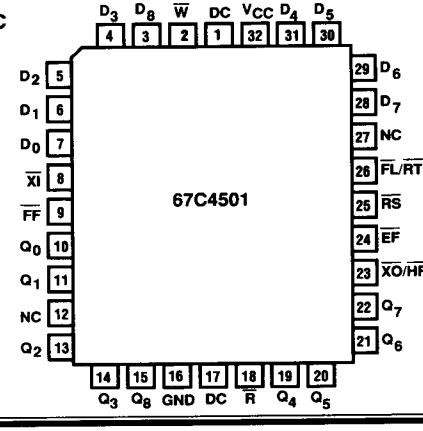
PART NUMBER	DESCRIPTION	PACK	TEMP
67C4501-25	512-word by 9-bit FIFO	N,J,NL	Com
67C4501-35	512-word by 9-bit FIFO	N,J,NL	Com
67C4501-50	512-word by 9-bit FIFO	N,J,NL	Com
67C4501-65	512-word by 9-bit FIFO	N,J,NL	Com
67C4501-80	512-word by 9-bit FIFO	N,J,NL	Com

Pin Configurations

DIP



PLCC



Publication #	Rev.	Amendment
10175	C	/0

Issue Date: August 1988

Absolute Maximum Ratings*

Supply voltage, V_{CC} ..... -0.5 V to +7.0 V
Input voltage ..... -0.5 V to V_{CC} +0.5 V
Operating temperature ..... 0°C to +70°C
Storage temperature ..... -55°C to +150°C
Power dissipation ..... 1.0 W
D.C. output current ..... 50 mA

*Note:
Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

DC Electrical Characteristics Commercial: V_{CC} = 5 V ±10%, T_A = 0°C to + 70°C

SYMBOL	PARAMETER	67C4501-25 T_A = 25 ns MIN	MAX	67C4501-35 T_A = 35 ns MIN	MAX	67C4501-50 T_A = 50 ns MIN	MAX	67C4501-65 T_A = 65 ns MIN	MAX	67C4501-80 T_A = 80 ns MIN	MAX	UNITS
I_{LI}[1]	Input leakage current (any input)	-1	1	-1	1	-1	1	-1	1	-1	1	μA
I_{LO}[2]	Output leakage current	-10	10	-10	10	-10	10	-10	10	-10	10	μA
V_{IH}[3]	Input high voltage (all inputs except $\overline{XI}$)	2.0	—	2.0	—	2.0	—	2.0	—	2.0	—	V
V_{IL}[3]	Input low voltage (all inputs except $\overline{XI}$)	—	0.8	—	0.8	—	0.8	—	0.8	—	0.8	V
V_{IHXI}[3]	Input high voltage, $\overline{XI}$	3.5	—	3.5	—	3.5	—	3.5	—	3.5	—	V
V_{ILXI}[3]	Input low voltage, $\overline{XI}$	—	1.5	—	1.5	—	1.5	—	1.5	—	1.5	V
V_{OH}	Output logic "1" voltage I_{OH} = -2 mA	2.4	—	2.4	—	2.4	—	2.4	—	2.4	—	V
V_{OL}	Output logic "0" voltage I_{OL} = 8 mA	—	0.4	—	0.4	—	0.4	—	0.4	—	0.4	V
I_{CC1}[4]	Average V_{CC} power supply current	—	70	—	60	—	60	—	60	—	60	mA
I_{CC2}[4]	Average standby current (R = W = RS = FL/RT = V_{IH})	—	20	—	20	—	20	—	20	—	20	mA
I_{CC3}[4]	Power down current (all inputs = V_{CC} -0.2 V)	—	5	—	5	—	5	—	5	—	5	mA

Notes:
1. Measurements with GND ≤ V_{IN} ≤ V_{CC}.
2. $\overline{R}$ ≥ V_{IH}, GND ≤ V_{OUT} ≤ V_{CC}.
3. These are absolute voltage levels with respect to the ground pins on the device and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
4. I_{CC} measurements are made with outputs open.

AC Electrical Characteristics V_{CC} = 5 V ±10%, T_A = 0° C to + 70° C

SYMBOL	DESCRIPTION	FIG	67C4501-25 MIN	67C4501-25 MAX	67C4501-35 MIN	67C4501-35 MAX	67C4501-50 MIN	67C4501-50 MAX	67C4501-65 MIN	67C4501-65 MAX	67C4501-80 MIN	67C4501-80 MAX	UNITS
Write and Flag Timing													
t_{WC}	Write cycle time	3	35		45		65		80		100		ns
t_{WPW}	Write pulse width	3	25		35		50		65		80		ns
t_{WR}	Write recovery time	3	10		10		15		15		20		ns
t_{DS}	Data set-up time	3, 9	15		18		30		30		40		ns
t_{DH}	Data hold time	3, 9	0		0		5		10		10		ns
t_{WFF}	Write LOW to full flag LOW	6, 9		25		30		45		60		60	ns
t_{WHF}	Write LOW to half-full flag LOW	5		35		45		65		80		100	ns
t_{WEF}	Write HIGH to empty flag HIGH	4, 8		25		30		45		60		60	ns
t_{WLZ}[1]	Write pulse HIGH to data bus at LOW Z	8	5		10		15		15		20		ns
Read and Flag Timing													
t_{RC}	Read cycle time	3	35		45		65		80		100		ns
t_A	Access time	3,4,8,9		25		35		50		65		80	ns
t_{RR}	Read recovery time	3	10		10		15		15		20		ns
t_{RPW}	Read pulse width	3	25		35		50		65		80		ns
t_{RLZ}[1]	Read pulse LOW to data bus at LOW Z	3	5		5		10		10		10		ns
t_{DV}	Data valid from read pulse HIGH	3	5		5		5		5		5		ns
t_{RHZ}[1]	Read pulse HIGH to data bus at HIGH Z	3		18		20		30		30		30	ns
t_{RFF}	Read HIGH to full flag HIGH	6, 9		25		30		45		60		60	ns
t_{RHF}	Read HIGH to half-full flag HIGH	5		35		45		65		80		100	ns
t_{REF}	Read LOW to empty flag LOW	4, 8		25		30		45		60		60	ns
Reset Timing													
t_{RSC}	Reset cycle time	2	35		45		65		80		100		ns
t_{RS}	Reset pulse width	2	25		35		50		65		80		ns
t_{RSS}	Reset set-up time	2	25		35		50		65		80		ns
t_{RSR}	Reset recovery time	2	10		10		15		15		20		ns
t_{EFL}	Reset to empty flag LOW	2		35		45		65		80		100	ns
t_{HFH}	Reset to half-full flag HIGH	2		35		45		65		80		100	ns
t_{FFH}	Reset to full flag HIGH	2		35		45		65		80		100	ns
Retransmit Timing													
t_{RTC}	Retransmit cycle time	7	35		45		65		80		100		ns
t_{RT}	Retransmit pulse width	7	25		35		50		65		80		ns
t_{RTR}	Retransmit recovery time	7	10		10		15		15		20		ns

Note:

1. Characterized parameters.

Block Diagram

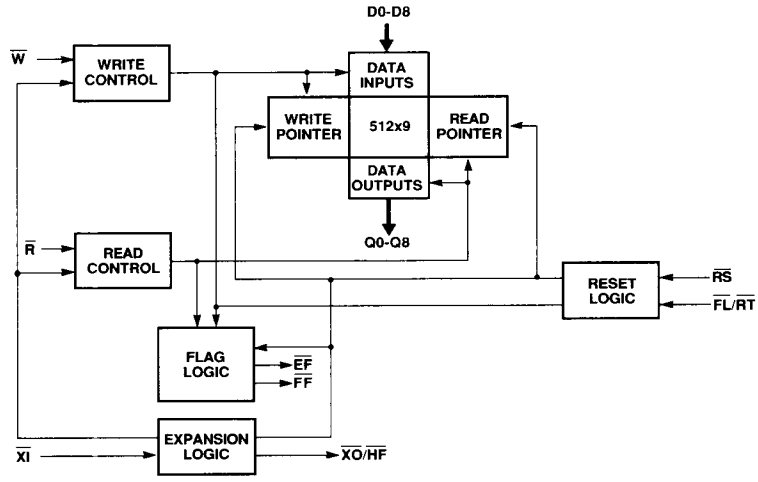


Figure 1.

Functional Description

The 67C4501 CMOS FIFO is designed around a 512x9 dual-port static RAM array. (See Figure 1.) RAM-based FIFOs store the data written into them in a sequential pattern.

The dual-port RAM array has dedicated write and read address pointers. The flag logic prevents illogical writes and reads from occurring. The Empty Flag prevents reading while empty, a data underflow condition. While the Full Flag prevents writing while full, a data overflow condition. Once data that has been stored at a given address is read, it can be overwritten.

Address pointers automatically overflow to address zero after reaching address 511. Thus the flag status of the FIFO is a function of the difference between the pointers, not their absolute value.

Resetting the FIFO simply initializes both address pointers to address zero. Pulsing Retransmit initializes the read address pointer to zero without affecting the write address pointer.

Expansion Logic is used when implementing a FIFO of a depth greater than that of the 67C4501. The write, read, data-in and data-out lines of the 67C4501 are connected in parallel, and the Expansion-Out ($\overline{XO}$) and the Expansion-In ($\overline{XI}$) lines are daisy-chained together. The write and read control circuits of the individual FIFOs are automatically enabled and disabled through the handshake between $\overline{XO}$ and $\overline{XI}$.

Operational Description

Resetting the FIFO

Upon power up, the FIFO must be initialized with a Reset cycle. (See Figure 2.) The states of $\overline{XI}$ and $\overline{FL}$ are used during the reset cycle to determine the FIFO's mode of operation, as shown in Tables 1 and 2. For a valid reset cycle to occur, both the Read ($\overline{R}$) and Write ($\overline{W}$) signals must be HIGH tRSS prior to, and tRSR after, the rising edge of Reset ($\overline{RS}$). The reset cycle initializes the FIFO to an empty condition, signified by the Empty Flag ($\overline{EF}$) being LOW (active), and both the Half-Full ($\overline{HF}$) and Full Flag ($\overline{FF}$) being HIGH (inactive).

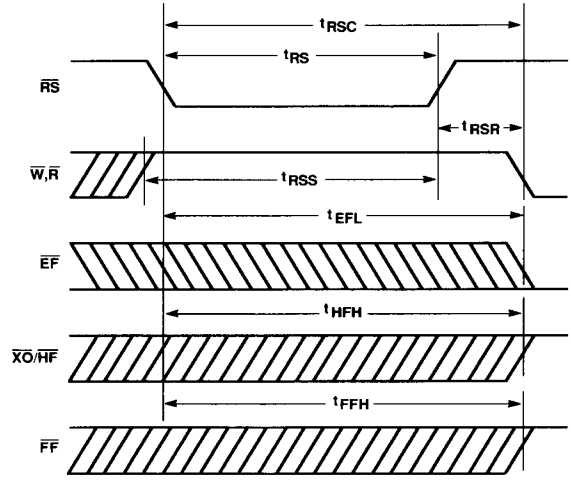


Figure 2. Reset Timing

Reset and Retransmit Truth Table — Single-Device Configuration/Width-Expansion Mode

MODE	INPUT			INTERNAL STATUS		OUTPUTS		
	$\overline{RS}$	$\overline{FL}/\overline{RT}$	$\overline{XI}$	READ POINTER	WRITE POINTER	$\overline{EF}$	$\overline{FF}$	$\overline{HF}$
Reset	0	X	0	Location zero	Location zero	0	1	1
Retransmit	1	0	0	Location zero	Unchanged	X[1]	X[1]	X[1]
Read/Write	1	1	0	Increment[2]	Increment[2]	X	X	X

1. Flags will change to show correct state according to write pointer.
2. Pointers will increment only if corresponding flag is HIGH at the beginning of the cycle.

Table 1.

Reset and First Load Truth Table — Depth-Expansion/Compound-Expansion Mode

MODE	INPUT			INTERNAL STATUS		OUTPUTS	
	$\overline{RS}$	$\overline{FL}/\overline{RT}$	$\overline{XI}$	READ POINTER	WRITE POINTER	$\overline{EF}$	$\overline{FF}$
Reset — first device	0	0	$\overline{XO}$[1]	Location zero	Location zero	0	1
Reset all other devices	0	1	$\overline{XO}$[1]	Location zero	Location zero	0	1
Read/Write	1	X[2]	$\overline{XO}$[1]	Increment[3]	Increment[3]	X	X

1. $\overline{XI}$ is connected to $\overline{XO}$ of previous device. See Figure 12.
2. Same as during Reset Cycle.
3. Pointers will increment only if corresponding flag is HIGH at the beginning of the cycle.

Table 2.

Writing Data to the FIFO

The HIGH state of the Full Flag ($\overline{FF}$) indicates that the FIFO is capable of accepting data. The falling edge of Write ($\overline{W}$) initiates a write cycle. (See Figure 3.) Data appearing at inputs D0-D8 tDS prior to, and tDH after, the rising edge of $\overline{W}$ will be stored sequentially in the FIFO.

The LOW-to-HIGH transition of the Empty Flag ($\overline{EF}$) occurs tWEF after the rising edge of $\overline{W}$ during the first write cycle on an empty FIFO. (See Figure 4.) The Half-Full Flag ($\overline{HF}$) will go LOW tWHF after the falling edge of $\overline{W}$ during the write operation which creates the half-full condition. (See Figure 5.) $\overline{HF}$ will remain LOW, while the number of writes to the FIFO exceed the number of reads by 256 or more. The Half-Full Flag is not available in Depth-Expansion Mode. The Full Flag ($\overline{FF}$) goes LOW tWFF after the falling edge of $\overline{W}$ during the write cycle which creates a full condition. (See Figure 6.) A full condition exists when there have been 512 more write cycles than read cycles. The Full Flag being active prohibits any further write operations, thus preventing data overflow situations.

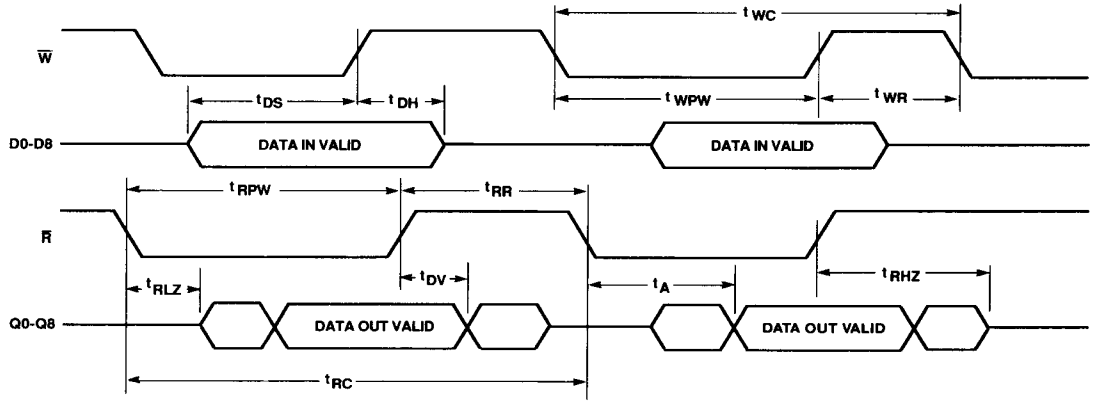


Figure 3. Asynchronous Write and Read Timing

Reading Data from the FIFO

The HIGH state of the Empty Flag ($\overline{EF}$) indicates that the FIFO is ready to output data. The falling edge of Read ($\overline{R}$) initiates a read cycle. (See Figure 3.) Valid data appears on the outputs Q0-Q8 tA after the falling edge of $\overline{R}$, and remains until tDV after the rising edge of $\overline{R}$. Q0-Q8 return to a high impedance state when $\overline{R}$ is inactive, when the FIFO is empty, or when the FIFO is in Depth Expansion Mode but is not active.

The Full Flag ($\overline{FF}$) will go HIGH tRFF after the rising edge of $\overline{R}$ during the first read cycle following a full condition. (See Figure 6.) The Half-Full Flag ($\overline{HF}$) will go HIGH tRHF after the rising edge of $\overline{R}$ during the read operation, which eliminates the half-full condition. (See Figure 5.) $\overline{HF}$ will remain HIGH, while the number of writes to the FIFO exceed the number of reads by 255 or less. The Half-Full Flag is not available in Depth-Expansion Mode. The HIGH-to-LOW transition of $\overline{EF}$ occurs tREF after the falling edge of $\overline{R}$ during the read cycle, which creates an empty condition. An empty condition exists when there have been an equal number of write cycles and read cycles. The Empty Flag being active prohibits any further read operations, thus preventing a data underflow situation.

Half-Full Flag

The Half-Full ($\overline{HF}$) Flag will be active LOW only when the net balance of the words written into the FIFO exceeds the number of words read out by 256 or more. (See Figure 5.)

Care should be exercised in using the Half-Full Flag, because it is capable of producing arbitrarily short pulses. For example, if the FIFO contains 256 words, and Read and Write pulses are applied simultaneously, the $\overline{HF}$ flag may produce an arbitrarily short pulse, depending on the precise phase of Read and Write.

$\overline{HF}$ will always settle to the correct state after the appropriate delay, tWHF or tRHF. This property of the Half-Full Flag is clearly a function of the dynamic relation between $\overline{W}$ and $\overline{R}$. Generally, the use of level-sensitive, rather than edge-sensitive, status detection circuits will alleviate this hazard.

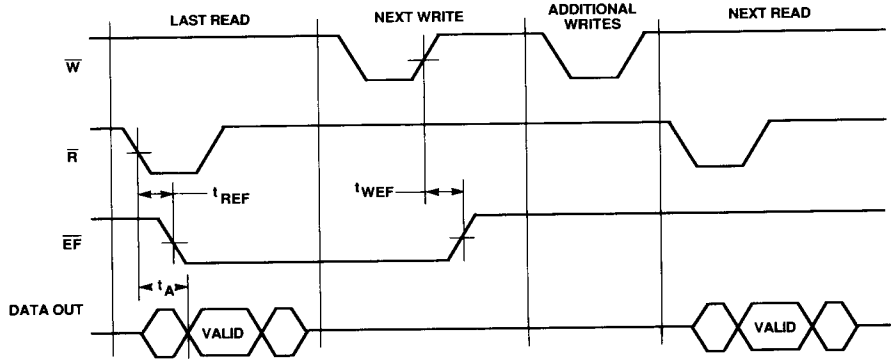
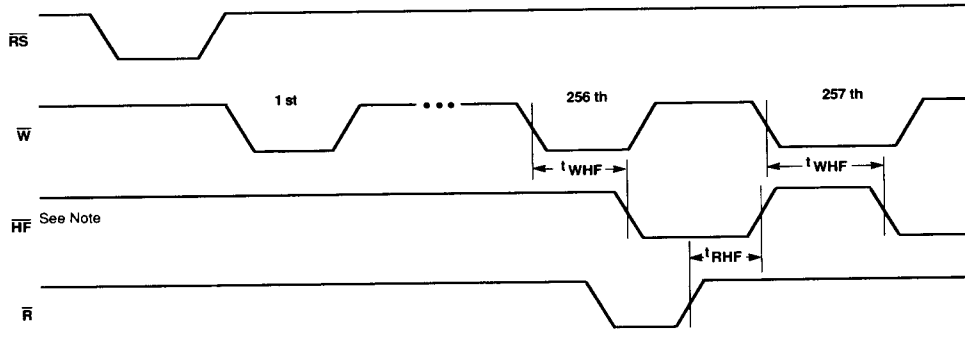


Figure 4. Empty Flag Timing



Note: Depending on the precise phase of $\overline{W}$ and $\overline{R}$, the Half-Full Flag may appear as a pulse of arbitrarily short duration of either polarity when $\overline{W}$ and $\overline{R}$ are operating asynchronously near half-full.

Figure 5. Half-Full Flag Timing

Retransmit

The $\overline{FL}/\overline{RT}$ is used as the Retransmit ($\overline{RT}$) input in Single Device Mode. The retransmit capability is intended for use when there are 512 or less writes between reset cycles. $\overline{RT}$, an active LOW going pulse of at least tRT in duration, initializes the internal read pointer to address zero and leaves the write pointer unaffected. $\overline{W}$ and $\overline{R}$ must both be HIGH during the retransmit cycle. The first write or read cycle should not start until tRTR after the rising edge of $\overline{RT}$. The flags may change state during this cycle, but they will accurately reflect the new state of the FIFO tRTC after the falling edge of $\overline{RT}$. (See Figure 7 and Table 1.)

Single-Device/Width-Expansion Modes

Single-Device and Width-Expansion Modes are configured by grounding the Expansion-In ($\overline{XI}$) input. (See Figures 10 & 11 and Table 1.) During these modes of operation, the Half-Full Flag and Retransmit features are available. The 67C4501 can be expanded in width to create FIFOs of word widths greater than 9 bits . In Width-Expansion Mode all of the control line inputs are common to all devices. (See Figure 11.) Creating composite status flags can pose two hazards. 1) OR-ing the flag outputs is fine for the HIGH-to-LOW transition, because the skew between devices is masked out. However, when the flags make a LOW-to-HIGH transition, a false composite flag is generated due to the skew between devices. 2) The converse is true when the flags are AND-ed: the LOW-to-HIGH transition is fine, and the HIGH-to-LOW generates a false flag. These two hazards can be avoided if one devices' flags are used as the flags for the expanded FIFO, and the write and read control circuitry is designed to hold off sampling the flags until the worst case settling time (tWEF, tWHF, tWFF, tREF, tRHF, and tWFF) for each flag has elapsed.

Depth-Expansion Mode

Depth-Expansion Mode is configured during the Reset cycle. (See Figure 12 and Table 2.) Expansion Out ($\overline{XO}$) of one device must be connected to Expansion In ($\overline{XI}$) of the next device, with $\overline{XO}$ of the last device being connected to $\overline{XI}$ of the first device. The device that is to receive data first has its First Load ($\overline{FL}$) input tied LOW, while all other devices must have this input HIGH. Write and read control is passed between devices using $\overline{XO}$ and $\overline{XI}$. A LOW-going pulse on $\overline{XO}$ occurs when the last physical location, address 511, of an active device is written to, and another LOW-going pulse occurs when the last physical location of an active device is read. Only one device is enabled for writes, and only one device is enabled for reads at any given time.

When expanding in depth, a composite Full Flag must be created by OR-ing all the $\overline{FF}$ outputs together. Likewise, a composite Empty Flag is created by OR-ing all the $\overline{EF}$ outputs together. The Half-Full Flag and Retransmit functions are not available in Depth-Expansion Mode.

Compound Expansion

FIFOs of greater width and depth than the 67C4501 can be created by using both Width-Expansion Mode and Depth-Expansion Mode simultaneously. (See Figure 13.)

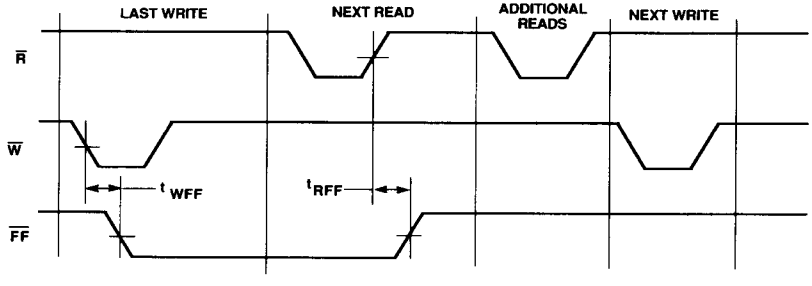
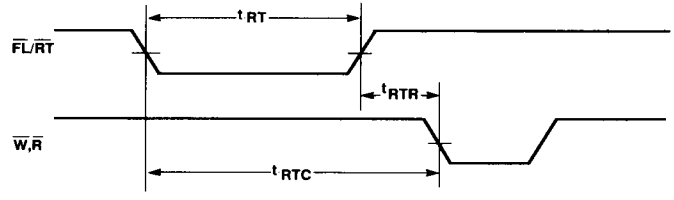
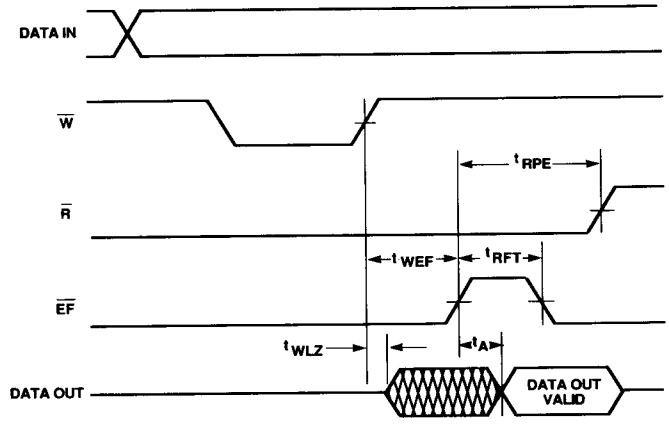


Figure 6. Full Flag Timing



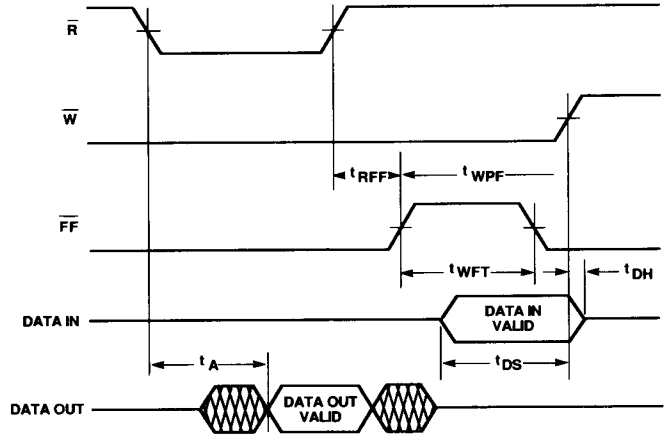
Note: $\overline{EF}$, $\overline{HF}$ and $\overline{FF}$ may change state during Retransmit as a result of the offset of the read and write pointers, but the flags will be valid at tRTC.

Figure 7. Retransmit Timing



Note: ($t_{RPE} = t_{RPW}$, $t_{RFT} = t_{REF}$)

Figure 8. Read Data Flow Through Mode



Note : ($t_{WPF} = t_{WPW}$, $t_{WFT} = t_{WFF}$)

Figure 9. Write Data Flow Through Mode