Dual universal serial communications controller (DUSCC)

68562

DESCRIPTION

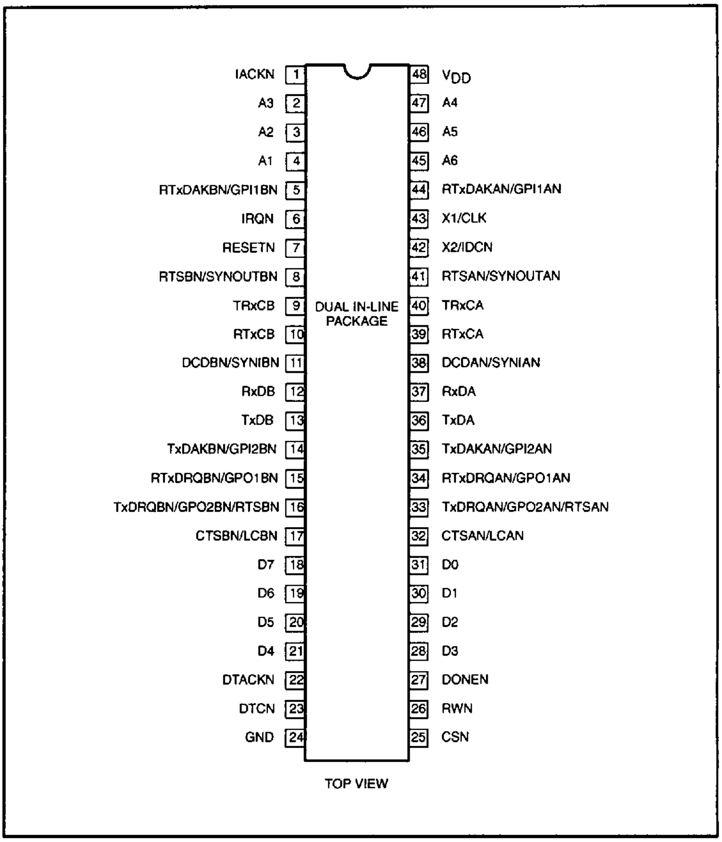
The Philips Semiconductors Dual Universal Serial Communications Controller (DUSCC) is a single-chip MOS-LSI communications device that provides two independent, multiprotocol, full-duplex receiver/transmitter channels in a single package. It supports bit-oriented (byte count and byte control) synchronous protocols. The 68562 interfaces to the 68000 MPU via asynchronous bus control signals and is capable of program-polled, interrupt-driven, block-move or DMA data transfers.

The operating mode and data format of each channel can be programmed independently. Each channel consists of a receiver, a transmitter, a 16-bit multifunction counter/timer, a Digital Phase-Locked Loop (DPLL), a parity/CRC generator and checker, and associated control circuits. The two channels share a common Bit Rate Generator (BRG), operating directly from a crystal or an external clock, which provides sixteen common bit rates simultaneously. The operating rate for the receiver and transmitter of each channel can be independently selected from the BRG, the DPLL, the counter/timer, or from an external 1X or 16X clock, making the DUSCC well suited for dual-speed channel applications. Data rates up to 4Mbits are supported.

The transmitter and receiver each contain a four-deep FIFO with appended transmitter command and receiver status bits and a shift register. This permits reading and writing of up to four characters at a time, minimizing the potential of receiver overrun or transmitter underrun, and reducing interrupt or DMA overhead. In addition, a flow control capability is provided to disable a remote transmitter when the FIFO of the local receiving device is full.

Two modem control inputs (DCD and CTS) and three modem control outputs (RTS and two general purpose) are provided. Because the modem control inputs and outputs are general purpose in nature, they can be optionally programmed for other functions.

PIN CONFIGURATION



ORDERING INFORMATION

DESCRIPTION	ORDER CODE	PACKAGE DESIGNATOR*
48-Pin Ceramic DIP	68562/BXA	GDIP1-T48

* MIL-STD 1835 or Appendix A of 1995 Military Data Handbook

7110826 0085061 T82

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FEATURES

General Features

- Dual full-duplex synchronous/ asynchronous receiver and transmitter
- Multiprotocol operation
  - BOP: HDLC/ADCCP, SDLC, SDLC loop, X.25 or X.75 link level, etc.
  - COP: BISYNC, DDCMP
  - ASYNC: 5 - 8 bits plus optional parity
- Four character receiver and transmitter FIFOs
- 0 to 4MHz data rate
- Programmable bit rate for each receiver and transmitter selectable from:
  - 16 fixed rates: 50 to 38.4k baud
  - One user-defined rate derived from programmable counter/timer
  - External 1X or 16X clock
  - Digital phase-locked loop
- Parity and FCS (Frame Check Sequence LRC or CRC) generation and checking
- Programmable data encoding/decoding: NRZ, NRZI, FM, FM1, Manchester
- Programmable channel mode: full-half-duplex, auto-echo, or local loopback
- Programmable data transfer mode: polled, interrupt, DMA, wait
- DMA interface
  - Half- or full-duplex operation
  - Single or dual address data transfers
  - Automatic frame termination on counter/ timer terminal count or DMA DONE
- Interrupt capabilities
  - Daisy chain option
  - Vector output (fixed or modified by status)
  - Programmable internal priorities
  - Maskable interrupt conditions
  - 68000 compatible
- Multifunction programmable 16-bit counter/timer
  - Bit rate generator
  - Event counter
  - Count received or transmitted characters
  - Delay generator
  - Automatic bit length measurement
- Modem controls
  - RTS, CTS, DCD, and up to four general purpose I/O pins per channel
  - CTS and DCD programmable autoenables for Tx and Rx
  - Programmable interrupt on change of CTS or DCD
- On-chip oscillator for crystal
- TTL compatible
- Single +5V power supply

Asynchronous Mode Features

- Character length: 5 to 8 bits
- Odd or even parity, no parity, or force parity
- Up to two stop bits programmable in 1/16-bit increments
- 1X or 16X Rx and Tx clock factors
- Parity, overrun, and framing error detection
- False start bit detection
- Start bit search 1/2 bit time after framing error detection
- Break generation with handshake for counting break characters
- Detection of start and end of received break
- Character compare with optional interrupt on match
- Transmit up to 4Mbps and receive up to 2Mbps data rates

Character-Oriented Protocol Features

- Character length: 5 to 8 bits
- Odd or even parity, no parity, or force parity
- LRC or CRC generation and checking
- Optional opening PAD transmission
- One or two SYN characters
- External sync capability
- SYN detection and optional stripping
- SYN or MARK linefill on underrun
- Idle in MARK or SYNs
- Parity, FCS, overrun, and underrun error detection
- BISYNC Features
  - EBCDIC or ASCII header, test and control messages
  - SYN, DLE stripping
  - EOM (End Of Message) detection and transmission
  - Auto transparency mode switching
  - Auto hunt after receipt of EOM sequence (with closing PAD check after EOT or NAK)
  - Control character sequence detection for both transparent and normal text

Bit-Oriented Protocol Features

- Character length: 5 to 8 bits
- Detection and transmission of residual character: 0 - 7 bits
- Automatic switch to programmed character length for 1 field
- Zero insertion and deletion
- Optional opening PAD transmission
- Detection and generation of FLAG, ABORT, and IDLE bit patterns
- Detection and generation of shared (single) FLAG between frames
- Detection of overlapping (shared zero) FLAGs
- ABORT, ABORT-FLAGs, or FCS-FLAGs line fill on underrun
- Idle in MARK or FLAGs
- Secondary address recognition including group and global address
- Single- or dual-octet secondary address
- Extended address and control fields
- Short frame rejection for receiver
- Detection and notification of received end of message
- CRC generation and checking
- SDLC loop mode capability

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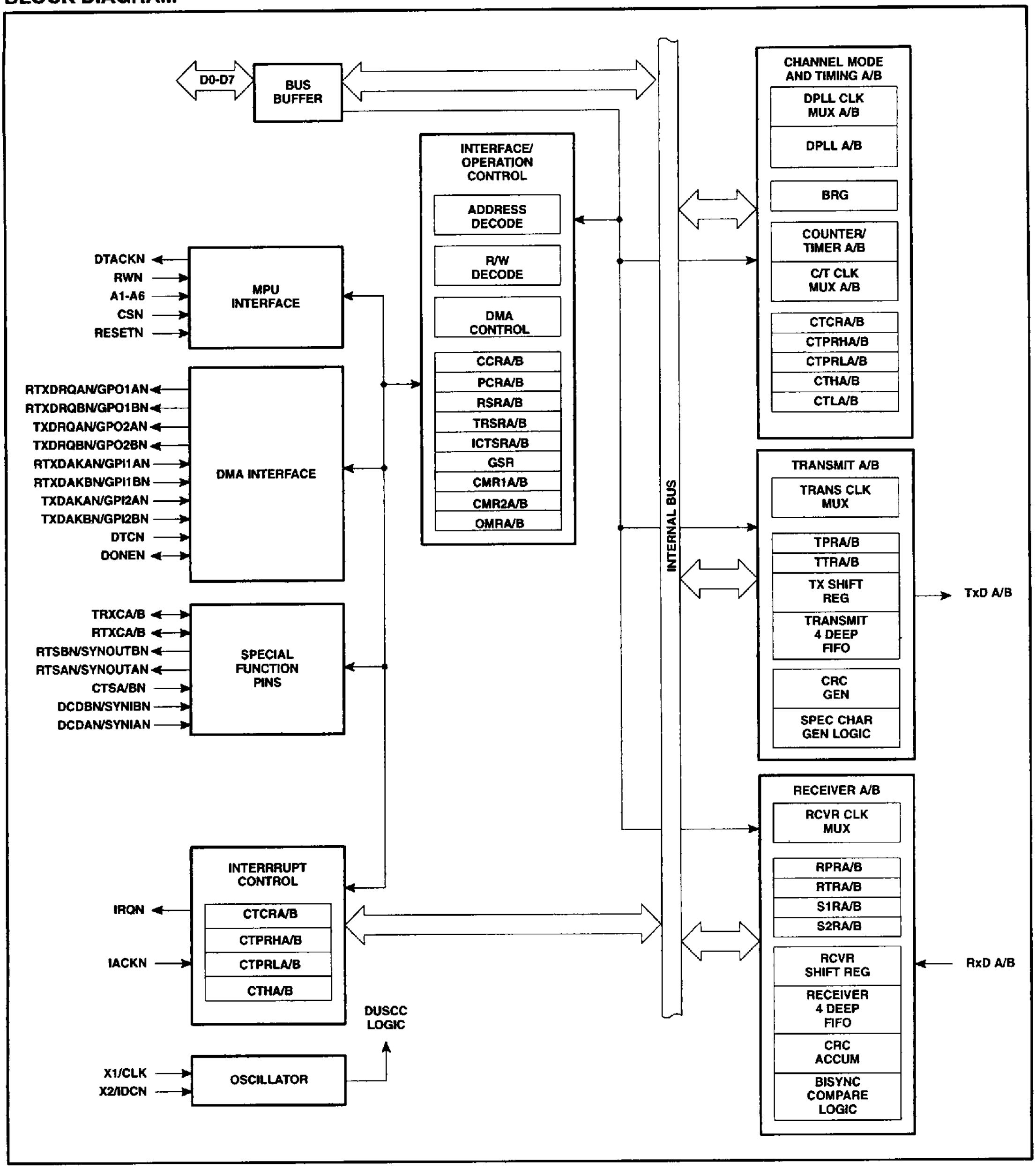
BLOCK DIAGRAM



7110826 0085063 855

PIN DESCRIPTION

In this data sheet, signals are discussed using the terms 'active' and 'inactive' or 'asserted' and 'negated' independent of whether the signal is active in the High (logic 1) or Low (logic 0) state. N at the end of a pin name signifies the signal associated with the pin is active-Low (see individual pin description for the definition of the active level of each signal.) Pins which are provided for both channels are designated by A/B after the name of the pin and the active-Low state indicator, N, if applicable. A similar method is used for registers provided for both channels: these are designated by either an underline or by A/B after the name.

MNEMONIC	DIP PIN NO.	TYPE	NAME AND FUNCTION
A1 - A6	4-2, 45-47	I	**Address Lines:** Active-High. Address inputs which specify which of the internal registers is accessed for read/write operation.
D0 - D7	31-28, 21-18	I/O	**Bidirectional Data Bus:** Active High, 3-State. Bit 0 is the LSB and bit 7 is the MSB. All data, command, and status transfers between the CPU and the DUSCC take place over this bus. The data bus is enabled when CSN is Low, during interrupt acknowledge cycles and single-address DMA acknowledge cycles.
R/WN	26	I	**Read/Write:** A High input indicates a read cycle and a Low input indicates a write cycle when a cycle is initiated by assertion of the CSN input.
CSN	25	I	**Chip Select:** Active-Low input. When Low, data transfers between the CPU and the DUSCC are enabled on D0 - D7 as controlled by the R/WN and A1 - A6 inputs. When CSN is High, the DUSCC is isolated from the data bus (except during interrupt acknowledge cycles and single-address DMA transfers) and D0 - D7 are placed in the 3-State condition.
DTACKN	22	O	**Data Transfer Acknowledge:** Active-Low, 3-State. DTACKN is asserted on a write cycle to indicate that the data on the bus has been latched, and on a read cycle or interrupt acknowledge cycle to indicate valid data is on the bus. The signal is negated when completion of the cycle is indicated by negation of the CSN or IACKN input, and returns to the inactive state (3-State) a short period after it is negated. In a single address DMA mode, data is latched with the falling edge of DTCN. DTACKN is negated when completion of the cycle is indicated by the assertion of DTCN or negation of DMA acknowledge inputs (whichever occurs first), and returns to the inactive state (3-State) a short period after it is negated. When negated, DTACKN becomes an open-drain output and requires an external pull-up resistor.
IRQN	6	O	**Interrupt Request:** Active-Low, open-drain. This output is asserted upon occurrence of any enabled interrupting condition. The CPU can read the general status register to determine the interrupting condition(s), or can respond with an interrupt acknowledge cycle to cause the DUSCC to output an interrupt vector on the data bus.
IACKN	1	I	**Interrupt Acknowledge:** Active-Low. When IACKN is asserted, the DUSCC responds by placing the contents of the interrupt vector register (modified or unmodified by status) on the data bus and asserting DTACKN. If no active interrupt is pending, DTACKN is not asserted.
X1/CLK	43	I	**Crystal or External Clock:** When using the crystal oscillator, the crystal is connected between pins X1 and X2. If a crystal is not used, and external clock is supplied at this input. This clock is used to drive the internal bit rate generator, as an optional input to the counter/timer or DPLL, and to provide other required clocking signals.
X2/IDCN	42	I/O	**Crystal or Interrupt Daisy Chain:** When a crystal is used as the timing source, the crystal is connected between pins X1 and X2. This pin can be programmed to provide and interrupt daisy chain active-Low output which propagates the IACKN signal to lower priority devices, if no active interrupt is pending. This pin should be grounded when an external clock is used on X1 and X2, is not used as an interrupt daisy chain output.
RESETN	7	I	**Master Reset:** Active-Low. A low on this pin resets the transmitters and receivers and resets the registers shown in Table 1. Reset in asynchronous, i.e., no clock is required.
RxDA, RxDB	37, 12	I	**Channel A (B) Receiver Serial Data Input:** The least significant bit is received first. If external receiver clock is specified for the channel, the input is sampled on the rising edge of the clock.
TxDA, TxDB	36, 13	O	**Channel A (B) Transmitter Serial Data Output:** The least significant bit is transmitted first. This output is held in the marking (High) condition when the transmitter is disabled or when the channel is operating in local loopback mode. If external transmitter clock is specified for the channel, the data is shifted on the falling edge of the clock.
RTxCA, RTxCB	39, 10	I/O	**Channel A (B) Receiver/Transmitter Clock:** As an input, it can be programmed to supply the receiver, transmitter, counter/timer, or DPLL clock. As an output, can supply the counter/timer output, the transmitter shift clock (1X), or the receiver sampling clock (1X). The maximum external receiver/transmitter clock frequency is 4MHz.

PIN DESCRIPTION (Continued)

MNEMONIC	DIP PIN NO.	TYPE	NAME AND FUNCTION
TRxCA, TRxCB	40, 9	I/O	**Channel A (B) Transmitter/Receiver Clock:** As an input, it can supply the receiver, transmitter, counter/timer, or DPLL clock. As an output, it can supply the counter/timer output, the DPLL output, the transmitter shift clock (1X), the receiver sampling clock (1X), the transmitter BRG clock (16X), The receiver BRG clock (16X), or the internal system clock (X1/2). The maximum external receiver/transmitter clock frequency is 4MHz.
CTSA/BN, LCA/BN	32, 17	I/O	**Channel A (B) Clear-To-Send Input or Loop Control Output:** Active-Low. The signal can be programmed to act as an enable for the transmitter when not in loop mode. The DUSCC detects logic level transitions on this input and can be programmed to generate an interrupt when a transition occurs. When operating in the COP loop mode, this pin becomes a loop control output which is asserted and negated by DUSCC commands. This output provides the means of controlling external loop interface hardware to go on-line and off-line without disturbing operation of the loop.
DCDA/BN, SYNIA/BN	38, 11	I	**Channel A (B) Data Carrier Detected or External Sync Input:** The function of this pin is programmable. As a DCD active-Low input, it acts as an enable for the receiver or can be used as a general purpose input for the DCD function, the DUSCC detects logic level transitions on this input and can be programmed to generate an interrupt when a transition occurs. As an active-Low external sync input, it is used in COP modes to obtain character synchronization without receipt of a SYN character. This mode can be used in disc or tape controller applications or for the optional byte timing lead in X.21.
RTxDRQA/BN, GPO1A/BN	34, 15	O	**Channel A (B) Receiver/Transmitter DMA Service Request or General Purpose Output:** Active-Low. For half-duplex DMA operation, this output indicates to the DMA controller that one or more characters are available in the receiver FIFO (when the receiver is enabled) or that the transmit FIFO is not full (when the transmitter is enabled). For full-duplex DMA operation, this output indicates to the DMA controller that data is available in the receiver FIFO. In non-DMA mode, this pin is a general purpose output that can be asserted and negated under program control.
TxDRQA/BN, GPO2A/BN, RTSA/BN	33, 16	O	**Channel A (B) Transmitter DMA Service Request, General Purpose Output, or Request-to-Send:** Active-Low. For full-duplex DMA operation, this output indicates to the DMA controller that the transmit FIFO is not full and can accept more data. When not in full-duplex DMA mode, this pin can be programmed as a general purpose or a Request-to -Send output, which can be asserted and negated under program control (see Detailed Operation).
RTxDAKA/BN, GPI1A/BN	44, 5	I	**Channel A (B) Receiver/Transmitter DMA Acknowledge or General Purpose Input:** Active-Low. For half-duplex single address DMA operation, this input indicates to the DUSCC that the DMA controller has acquired the bus and that the requested bus cycle (read receiver FIFO or load transmitter FIFO) is beginning. For full-duplex single address DMA operation, this input indicates to the DUSCC that the DMA controller has acquired the bus and that the requested read receiver FIFO bus cycle is beginning. Because the state of this input can be read under program control, it can be used as a general purpose input when not in single address DMA mode.
TxDAKA/BN, GP12A/BN	35, 14	I	**Channel A (B) Transmitter DMA Acknowledge or General Purpose Input:** Active-Low. When the channel is programmed for full-duplex single address DMA operation, this input is asserted to indicate to the DUSCC that the DMA controller has acquired the bus and that the requested load transmitter FIFO bus cycle is beginning. Because the state of this input can be read under program control, it can be used as a general purpose input when not in full-duplex single address DMA mode.
DTCN	23	I	**Device Transfer Complete:** Active-Low. DTCN is asserted by the DMA controller to indicate that the requested data transfer is complete.
DONEN	27	I/O	**Done:** Active-Low, open-drain. See Detailed Operation for a description of the function of this pin.
RTSA/BN, SYNOUTA/BN	41, 8	O	**Channel A (B) Sync Detect or Request-to-Send:** Active-Low. If programmed as a sync output, it is asserted one bit time after the specified sync character (COP or BISYNC modes) or a FLAG (BOP modes) is detected by the receiver. As a Request-to-Send modem control signal, it functions as described previously for the TxDRQN/RTSN pin.
V_{DD}	48	I	+5V ± 10% power input.
GND	24	I	Signal and power ground input.

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
P_W	Max Power Dissipation	1.8	W
T_{STG}	Storage Temperature range	-65 to +150	°C
	All voltages with respect to ground[3]	-0.5 to 7.0	V

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS Min	LIMITS Max	UNITS
V_{CC}	Supply voltage	4.5	5.5	V
V_{IH}	High level input voltage All except X1 and CLK X1 and CLK	 2.0 2.4		 V V
V_{IL}	Low level input voltage All except X1 and CLK X1 and CLK		 0.8 0.4	 V V
I_{IH}	Input current High		-400	µA
T_A	Operating free-air temperature range	-55	+110	°C

DC CHARACTERISTICS

T_A = -55 TO +110°C, V_{CC} = 5.0V ± 10%

SYMBOL	PARAMETER	TEST CONDITIONS[4, 5, 6]	LIMITS Min	LIMITS Max	UNIT
I_{CC}	Power supply current	V_{CC} = 5.5V		325	mA
V_{OL}	Output Low voltage All except DONEN & IRQN	V_{CC} = 4.5V I_{OL} = 5.3mA		0.5	V
V_{OL}	Output Low voltage DONEN & IRQN	V_{CC} = 4.5V I_{OL} = 8.8mA		0.5	V
V_{OH}	Output High voltage All except DONEN & IRQN	V_{CC} = 4.5V I_{OH} = -400µA	2.4		V
I_{OD}	Open-drain output leakage current (DONEN & IRQN)	V_{CC} = 5.5V V_O = 0V to V_{CC}		10	µA
I_{OZ}	3-State output leakage current	V_O = 0V to V_{CC} V_{CC} = 5.5V	-10	10	µA
I_{X1L}	X1/CLK Low input current	V_{CC} = 5.5V[11] V_{IN} = 0V, X2 floated V_{IN} = 0V, X2 grounded	 -5.0 -2.0		 mA mA
I_{X1H}	X1/CLK High input current	V_{CC} = 5.5V[11] V_{IN} = V_{CC}, X2 floated V_{IN} = V_{CC}, X2 grounded		 36.0 1.0	 mA mA
I_{X2L}	X2 Low input current	V_{CC} = 5.5V[11] V_{IN} = 0V, X1/CLK floated	-100		µA
I_{X2H}	X2 High input current	V_{CC} = 5.5V[11] V_{IN} = V_{CC}, X1/CLK floated		100	µA
I_{IH}	Input leakage current	V_{CC} = 5.5V V_{IN} = 5.5V		10	µA
I_{IL}	Input Low current All except DTCN, RTxDAKA/B, TxDAKA/B	V_{CC} = 5.5V V_{IN} = 0V	-100		µA
I_{IL}	Input Low current remaining input pins	V_{CC} = 5.5V V_{IN} = 0V	-10		µA

AC ELECTRICAL CHARACTERISTICS

T_A = -55 TO +110°C, V_{CC} = 5V ± 10%[4, 5, 6, 7]

NO.	FIGURE	PARAMETER	LIMITS Min	Typ	Max	UNIT
1	12	RESETN pulse width	1.2			µS
2	13, 15	A1 - A6 set-up time to CSN Low	10			nS
3	13, 15	A1 - A6 hold time from CSN High	0			nS
4	13, 15	RWN set-up time to CSN Low	0			nS
5	13, 15	RWN hold time to CSN High	0			nS
6	13, 15	CSN High pulse width[7]	160			nS
7	13, 16	CSN or IACKN High from DTACKN Low	30			nS
7A	16	IACKN High to DTACKN High			200	nS
8	13, 16	Data valid from CSN or IACKN Low			300	nS
9	13	Data bus floating from CSN High[10]			100	nS
10	15	Data hold time from DTACKN Low[8]	0			nS
11	13, 16	DTACKN Low from read data ready	0			nS
12	13, 15	DTACKN Low from CSN Low			560	nS
12A	15	CSN Low to write data valid			50	nS
13	13, 15	DTACKN High from CSN High			150	nS
14	13, 15	DTACKN high impedance from CSN High			185	nS
15	16	DTACKN Low from IACKN Low			550	nS
16	16	GPI input set-up time to CSN Low	20			nS
17	16	GPI input hold time from CSN Low	100			nS
18	16	GPO output valid from DTACKN Low			300	nS
19	18	IRQN High from:				
		Read RxFIFO (RxRDY interrupt)			450	nS
		Write TxFIFO (TxRDY interrupt)[12]			450	nS
		Write RSR (Rx condition interrupt)[12]			400	nS
		Write TRSR (Rx/Tx interrupt)[12]			400	nS
		Write ICTSR (port change and CT int.)[12]			400	nS
20	19	X1/CLK High or Low time	25			nS
		X1/CLK frequency	2.0	14.745 6	16	MHz
		CTCLK High or Low time	100			nS
		CTCLK frequency	0		4	MHz
		RxC High or Low time	110			nS
		RxC frequency (16X or 1X)[13]	0		4	MHz
		TxC High or Low time	110			nS
		TxC frequency (16X or 1X)	0		4	MHz
21	20	TxD output from TxC input Low (1X)			240	nS
		(16X)			435	nS
22	20	TxD output from TxC output Low			50	nS
23	21	RxD data set-up time to RxC High	50			nS
24	21	RxD data hold time from RxC High	50			nS
25	22	IACKN Low to daisy chain Low			200	nS
26	24	Data valid from receive DMA ACKN			300	nS
27	23,24	DTCN width	100			nS
28	23,24	RDYN Low to DTCN Low	80			nS
29	24	Data bus float from DTCN Low[10]			200	nS
30	23,24	DMA ACKN Low to RDYN (DTACKN) Low			360	nS
31	23,24	RDYN High from DTCN Low			230	nS
32	23,24	RDYN High impedance from DTCN Low			250	nS
33	24	Receive DMA REQN High from DMA ACKN Low			325	nS
34	24	Receive DMA ACKN width	150			nS
35	23,24	Receive DMA ACKN Low to DONEN Low			250	nS
36	23	Data set-up to DTCN Low	50			nS
37	23	Data hold from DTCN Low[9]	50			nS
38	23	Transmit DMA REQN High from ACKN Low			340	nS
39	23	Transmit DMA ACKN width	150			nS
40	23	Transmit DMA ACKN Low to DONEN Low output			250	nS
40A	23	DTCN Low DONEN output High			260	nS
41	25	CSN Low to transmit DONEN Low output			300	nS
42	25	CSN Low to transmit DMA REQ negated			400	nS
43	25	CSN Low to receive DONEN Low			300	nS
44	25	CSN Low to receive DMA REQ negated			400	nS

NOTES: On following page

NOTES:

1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other conditions above those indicated in the operation section of this specification is not implied.
2. For operating at elevated temperatures, the device must be derated based on +150°C maximum junction temperature and thermal resistance of 35°C/W junction to ambient.
3. This product includes circuitry specifically designed for the protection of its internal devices from damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying any voltages larger than the rated maxima.
4. Parameters are valid over specified temperature range.
5. All voltage measurements are referenced to ground (GND). For D.C. and functional testing, all inputs except X1/CLK swing between 0.4V and 2.4V with a transition time of 20ns maximum. For X1/CLK, this swing is between 0.4V and 4.4V All time measurements are referenced at input voltages of 0.2V and 2.4V for all inputs. Output levels are referenced at 1.5V.
6. Test conditions for outputs: C_L = 150pF, except open-drain outputs. Test condition for open-drain outputs: C_L = 50pF to GND, R_L = 2.7kΩ to V_{CC} except DTACKN whose RL - 820Ω to V_{CC} and C_L = 150pF to GND and DONEN which requires C_L = 50pF to GND and RL = 1kΩ to V_{CC}.
7. This specification will impose maximum 68000 CPU CLK to 6MHz. Higher CPU CLK can be used if repeating bus cycles are not performed.
8. Execution of the valid command (after it is latched) requires three falling edges of X1 (see Figure 14).
9. In single address DMA mode write operation, data is latched by the falling edge of DTCN.
10. These values were not explicitly tested, they are guaranteed by design and characterization data.
11. X1/CLK and X2 are not tested with a crystal installed.
12. These timings are from the falling edge of DTACKN (not CSN rising).
13. X1/CLK frequency must be at least four times the receiver serial data rate.

REGISTERS

The addressable registers of the DUSCC are shown in Table 1. The following rules apply to all registers:

7. A read from a reserved location in the map results in a read from the 'null register'. The null register returns all ones for data and results in a normal bus cycle. A write to one of these locations results in a normal bus cycle without a write being performed.
8. Unused bits of a defined register are read as zeros, unless ones have been loaded after master reset.
9. Bits that are unused in the chosen mode but are used in others are readable and writeable but their contents are ignored in the chosen mode.
10. All registers are addressable as 8-bit quantities. To facilitate operation with the 68000 MOVEP instruction, addresses are ordered such that certain sets of registers may also be accessed as words or long words.

The operation of the DUSCC is programmed by writing control words into the appropriate registers. Operational feedback is provided via status registers which can be read by the CPU. The contents of certain control registers are initialized on RESET. Care should be exercised if the contents of a register are changed during operation, since certain changes may cause operational problems, e.g., changing the channel mode at an inappropriate time may cause the reception or transmission of an incorrect character. In general, the contents of registers which control transmitter or receiver operation, or the counter/timer, should be changed only when they are not enabled.

The DUSCC registers can be separated into five groups to facilitate their usage:

1. Channel mode configuration and pin description registers.
2. Transmitter and receiver parameter and timing registers.
3. Counter/timer control and value registers.
4. Interrupt control and status registers.
5. Command register.

This arrangement is used in the following description of the DUSCC registers.

Channel Mode Configuration and Pin Description Registers

There are five registers in this group for each channel. The bit format for each of these registers is contained in Table 2. The primary function of these registers is to define configuration of the channels and the function of the programmable pins. A channel cannot be dynamically reconfigured. Do not write to CMR1 or CMR2 if the receiver or transmitter is enabled.

Channel Mode Register 1 (CMR1A, CMR1B)

[7:6] Data Encoding—These bits select the data encoding for the received and transmitted data:

00	If the DPLL is set to NRZI mode (see DPLL commands), it selects positive logic (1 = High, 0 = Low). If the DPLL is set to FM mode (see DPLL commands), Manchester (bi-phase level) encoding is selected.
01	NRZI. Non-return-to-zero inverted.
10	FM0. Bi-phase space.
11	FM1. Bi-phase mark.

[5] Extended Control (BOP)—

0	No. A one-octet control field follows the address field.
1	Yes. A two-octet control field follows the address field.

[5] Parity (COP/ASYNC), Code Select (BISYNC)—

0	Even parity if with parity is selected by [4:3] or a 0 in the parity bit position if force parity is selected by [4:3]. In BISYNC protocol mode, internal character comparisons are made using EBCDIC coding.
1	Odd parity if with parity is selected by [4:3] or a 1 in the parity bit position if force parity is selected by [4:3]. In BISYNC protocol mode, internal character comparisons are made using 7-bit plus odd parity ASCII coding. (Note: The receiver should be programmed for 7-bit characters, RPR[1:0] = 11, with no parity, CMR1[4:3] = 00.)

[4:3] Address Mode (BOP)—This field controls whether a single octet or multiple octets follow the opening FLAG(s) for both the receiver and the transmitter. This field is activated by selection of BOP secondary mode through the channel protocol mode bits CMR1[2:0] (see Detailed Operation).

00 Single-octet address.

01 Extended address.

10 Dual-octet address.

11 Dual-octet address with group.

[4:3] Parity Mode (COP/ASYNC)—This field selects the parity mode for both the receiver and the transmitter. A parity bit is added to the programmed character length if with parity or force parity is selected:

00 No parity. Required when BISYNC protocol mode is programmed.

01 Reserved.

10 With parity. Odd or even parity is selected by [5].

11 Force parity. The parity bit is forced to the state selected by [5].

[2:0] Channel Protocol Mode—This field selects the operational protocol and submode for both the receiver and transmitter:

000 BOP Primary. No address comparison is performed. For receive, all characters received after the opening FLAG(s) are transferred to the FIFO.

001 BOP Secondary. This mode activates the address modes selected by [4:3]. Except in the case of extended address ([4:3] = 01), and address comparison is performed to determine if a frame should be received. Refer to Detailed Operation for details of the various addressing modes. If a valid comparison occurs, the receiver is activated and the address octets and all subsequent received characters of the frame are transferred to the receive FIFO.

010 BOP Loop. The DUSCC acts as a secondary station in a loop. The GO-ON-LOOP and GO-OFF-LOOP commands are used to cause the DUSCC to go on and off the loop. Normally, the TxD output echoes the RxD input with a two-bit time delay. If the transmitter is enabled and the 'go active on poll' command has been asserted, the transmitter will begin sending when an EOP sequence consisting of a zero followed by seven ones is detected. The DUSCC changes the last one of the EOP to zero, making it another FLAG, and then operates as described in the Detailed Operation section. The loop sending status bit (TRSR[6]_ is asserted concurrent with the beginning of transmission. The frame should normally be terminated with an EOM followed by an echo of the marking RxD line so that secondary stations further down the loop can append their messages to the messages from up-loop stations by the same process. If the 'go active on poll' command is not asserted, the transmitter remains inactive (other than echoing the received data) even when the EOP sequence is received.

011 BOP Loop without address comparison. Same as normal loop mode except that address field comparisons are disabled. All received frames are transmitted to the CPU.

Table 1. DUSCC Register Address Map

ADDRESS BITS[1] 654321	ACRONYM	REGISTER NAME	MODE	AFFECTED BY RESET
c00000	CMR1	Channel Mode Register 1	R/W	Yes—00
c00001	CMR2	Channel Mode Register 2	R/W	Yes—00
c00010	S1R	SYN 1/Secondary Address 1 Register	R/W	No
c00011	S2R	SYN 2/Secondary Address 2 Register	R/W	No
c00100	TPR	Transmitter Parameter Register	R/W	Yes—00
c00101	TTR	Transmitter Timing Register	R/W	No
c00110	RPR	Receiver Parameter Register	R/W	Yes—00
c00111	RTR	Receiver Timing Register	R/W	No
c01000	CTPRH	Counter/Timer Preset Register High	R/W	No
c01001	CTPRL	Counter/Timer Preset Register Low	R/W	No
c01010	CTCR	Counter/Timer Control Register	R/W	Yes—00
c01011	OMR	Output and Miscellaneous Register	R/W	Yes—00
c01100	CTH	Counter/Timer High	R	No
c01101	CTL	Counter/Timer Low	R	No
c01110	PCR	Pin Configuration Register	R/W	Yes—00
c01111	CCR	Channel Command Register	R/W	No
c100XX	TxFIFO	Transmitter FIFO	W	No
c101XX	RxFIFO	Receiver FIFO	R	No
c11000	RSR	Receiver Status Register	R/W[2]	Yes—00
c11001	TRSR	Transmitter and Receiver Status Register	R/W[2]	Yes—00
c11010	ICTSR	Input and Counter/Timer Status Register	R/W[2]	Yes
d11011	GSR	General Status Register	R/W[2]	Yes—00
c11100	IER	Interrupt Enable Register	R/W	Yes—00
c11101		Not used		
011110	IVR	Interrupt Vector Register—Unmodified	R/W	Yes—0F
111110	IVRM	Interrupt Vector Register—Modified	R	Yes—0F
011111	ICR	Interrupt Control Register	R/W	Yes—00
111111		Not used		

NOTES:
1. c = 0 for Channel A, c = 1 for Channel B.
   d = don't care—register may be accessed as either channel.
   x = don't care—FIFOs are addressable at any of four adjacent addresses to allow them to be addressed as byte/word/long word with the 68000 MOVEP instruction.
2. A write to this register may perform a status resetting operation.

100 COP Dual SYN. Character sync is achieved upon receipt of a bit sequence matching the contents of the appropriate bits of S1R and S2R (SYN1-SYN2), including parity bits if any.

101 COP Dual SYN (BISYNC). Character sync is achieved upon receipt of a bit sequence matching the contents of the appropriate bits of S1R and S2R (SYN1-SYN2). In this mode, special transmitter and receive logic is activated. Transmitter and receiver character length must be programmed to 8 bits and no parity (see Detailed Operation).

110 COP Single SYN. Character sync is achieved upon receipt of a bit sequence matching the contents of the appropriate bits of S1R (SYN1), including parity bit if any. This mode is required when the external sync mode is selected (see description of RPR[4], BOP/COP).

111 Asynchronous. Start/stop format.

Channel Mode Register 2 (CMR2A, CMR2B)

[7:6] Channel Connection—This field selects the mode of operation of the channel. The user must exercise care when switching into and out of the various modes. The selected mode will be activated immediately upon mode selection, even if this occurs in the middle of a received or transmitted character.

00 Normal mode. The transmitter and receiver operate independently in either half- or full-duplex, controlled by the respective enable commands.

01 Automatic echo mode. Automatically retransmits the received data with a half-bit time delay (ASYNC, 16X clock mode) or a two-bit time delay (all other modes). The following conditions are true while in automatic echo mode:

1. Received data is reclocked and retransmitted on the TxD output.
2. The receiver clock is used for the transmitter for ASYNC 16X clock mode. For other modes the transmitter clock must be supplied.
3. The receiver must be enabled, but the transmitter need not be enabled.
4. The TxRDY and underrun status bits are inactive.
5. The received parity and/or FCS are checked if required, but are not regenerated for transmission, i.e., transmitted parity and/or FCS are as received.
6. In ASYNC mode, character framing is checked, but the stop bits are retransmitted as received. A received break is echoed as received.
7. CPU to receiver communication continues normally, but the CPU to transmitter link is disabled.

10 Local loopback mode. In this mode:

1. The transmitter data output and clock are internally connected to the receiver.
2. The transmit clock is used for the receiver if NRZI or NRZ encoding is used. For FM or Manchester encoding because the receiver clock is derived from the DPLL, the DPLL source clock must be maintained.
3. The TxD output is held High.
4. The RxD input is ignored.
5. The receiver and transmitter must be enabled.
6. CPU to transmitter and receiver communications continue normally.

11 Reserved.

[5:3] Data Transfer Interface—This field specifies the type of data transfer between the DUSCC's Rx and TxFIFOs and the CPU. All interrupt and status functions operate normally regardless of the data transfer interface programmed. Refer to Detailed Operation for details of the various DMA transfer interfaces.

000 Half-duplex single address DMA.

001 Half-duplex dual address DMA.

010 Full-duplex single address DMA.

011 Full-duplex dual address DMA.

100 Wait on receive only. In this mode a read of a non-empty receive FIFO results in a normal bus cycle. However, if the receive FIFO of the channel is empty when a read Rx FIFO cycle is initiated, the DTACKN output remains negated until a character is received and loaded into the FIFO. DTACKN is then asserted and the cycle is completed normally.

101 Wait on transmit only. In this mode a write to a non-full transmit FIFO results in a normal bus cycle. However, if the transmit FIFO of the channel is full when a write TxFIFO cycle is initiated, the DTACKN output remains negated until a FIFO position becomes available for the new character. DTACKN is then asserted and the cycle is completed normally.

110 Wait on transmit and receive. As above for both wait on receive and transmit operations.

111 Polled or interrupt. DMA and wait function of the channel are not activated. Data transfers to the Rx and TxFIFOs are via normal bus read and write cycles in response to polling of the status registers and/or interrupts.

[2:0] Frame Check Sequence Select—This field selects the optional frame check sequence (FCS) to be appended at the end of a transmitted frame. When CRC is selected in COP, then no parity and 8-bit character length must be used. The selected FCS is transmitted as follows:

1. Following transmission of a FIFOed character tagged with the 'send EOM' command.
2. If underrun control (TPR[7:6]) is programmed for TEOM, upon occurrence of an underrun.
3. If TEOM on zero count or done (TPR[4]) is asserted and the counter/timer is counting transmitted characters, after transmission of the character which causes the counter to reach zero count.
4. In DMA mode with TEOM on zero count or done (TPR[4]) set, after transmission of a character if DONEN is asserted when that character was loaded into the TxFIFO by the DMA controller.

000 No frame check sequence.

001 Reserved

010 LRC8: Divisor = $x^8 + 1$, dividend preset to zeros. The Tx sends the calculated LRC non-inverted. The Rx indicates and error if the computed LRC is not equal to 0. Valid for COP modes only.

011 LRC8: Divisor = $x^8 + 1$, dividend preset to ones. The Tx sends the calculated LRC non-inverted. The Rx indicates an error if the computed LRC is not equal to 0. Valid for COP modes only.

100 CRC16: Divisor - $x^{16} + x^{15} + x^2 + 1$, dividend preset to zeros. The Tx sends the calculated CRC non-inverted. The Rx indicates an error if the commuted CRC is not equal to 0. Not valid for ASYNC mode.

101 CRC16: Divisor = $x^{16} + x^{15} + x^2 + 1$, dividend preset to ones. The Tx sends the calculated CRC non-inverted. The Rx indicates an error if the computed CRC is not equal to 0. Not valid for ASYNC mode.

110 CRC-CCITT: Divisor = $x^{16} + x^{12} + x^5 + 1$, dividend preset to zeros. The Tx sends the calculated CRC non-inverted. The Rx indicates an error if the computed CRC is not equal to 0. Not valid for ASYNC mode.

111 CRC-CCITT: Divisor = $x^{16} + x^{12} + x^5 + 1$, dividend preset to ones. The Tx sends the calculated CRC inverted. The Rx indicates an error if the computed CRC is not equal to H'F0B8'. Not valid for ASYNC mode.

SYN1/Secondary Address 1 Register (S1RA, S1RB)

[7:0] Character Compare—In ASYNC mode this register holds a 5- to 8-bit long bit pattern which is compared with received characters. if a match occurs, the character compare status bit (RSR[7]) is set. This field is ignored if the receiver is in a break condition.

In COP modes, this register contains the 5- to 8-bit SYN1 bit pattern, right justified. Parity bit need not be included in the value placed in the register even is parity is specified in CMR1[4:3]. However, a character received with parity error, when parity is specified, will not match. In ASYNC, or COP modes, if parity is specified, then any unused bits in this register must be programmed to zeros. In BOP secondary mode it contains the address used to compare the first received address octet. The register is not used in BOP primary mode or secondary modes where address comparisons are not made, such as when extended addressing is specified.

SYN2/Secondary Address 2 Register (S2RA, S2RB)

[7:0]—This register is not used in ASYNC, COP single SYN, BOP primary modes, BOP secondary modes with single address field, and BOP secondary modes where address comparisons are not made, such as when extended addressing is specified.

In COP dual SYN modes, it contains the 5- to 8-bit SYN2 bit pattern, right justified, Parity bit need not be included in the value placed in the register even if parity is specified in CMR1[4:3]. However, a character received with parity error, when parity is specified, will not match. If parity is specified, then any unused bits in this register must be programmed to zeros. In BOP secondary mode using two address octets, it contains the partial address used to compare the second received address octet.

Pin Configuration Register (PCRA, PCRB)

This register selects the functions for multipurpose I/O pins.

[7] X2/IDC—This bit is defined only for PCRA. It is not used in PCRB

0 The X2/IDCN pin is used as a crystal connection.

1 The X2/IDCN pin is the interrupt daisy chain output.

[6] GPO2/RTS—The function of this pin is programmable only when not operating in full-duplex DMA mode.

0 The TxDRQN/GPO2N/RTSN pin is a general purpose output. It is Low when OMR[2] is a 1 and High when OMR[2] is a 0.

1 The pin is a request-to-send output (see Detailed Operation). The logical state of the pin is controlled by OMR[0]. When OMR[0] is set, the output is Low.

[5] SYNOUT/RTS—

0 The SYNOUTN/RTSN pin is an active-Low output which is asserted one bit time after a SYN pattern (COP modes) in HSRH/HSRL or FLAG (BOP modes) is detected in CCSR. The output remains asserted for one receiver clock period. See Figure 1 for receiver data path.

1 The pin is a request-to-send output (see Detailed Operation). The logical state of the pin is controlled by OMR[0] when OMR[0] is set, the output is Low.

[4:3] RTxC—

00 The pin is an input. It must be programmed for input when used as the input for the receiver or transmitter clock, the DPLL, or the C/T.

01 The pin is an output for the counter/timer. Refer to CTCRA/B description.

10 The pin is an output for the transmitter shift register clock.

11 The pin is an output for the receiver shift register clock.

[2:0] TRxC—

000 The pin is an input. It must be programmed for input when used as the input for the receiver or transmitter clock, the DPLL, or the C/T.

001 The pin is an output from the crystal oscillator divided by two.

010 The pin is an output for the DPLL output clock.

011 The pin is an output for the counter/timer. Refer to CTCRA/B description.

100 The pin is an output for the transmitter BRG at 16X the rate selected by TTR [3:0].

101 The pin is an output for the receiver BRG at 16X the rate selected by RTR [3:0].

110 The pin is an output for the transmitter shift register clock.

111 The pin is an output for the receiver shift register clock.

Transmitter and Receiver Parameter and Timing Registers

This set of five registers contains the information which controls the operation of the transmitter and receiver for each channel. Table 3 shows the bit map format for each of these registers. The registers of this group are:

1. Transmitter parameter and timing registers (TPRA/B and TTRA/B)
2. Receiver parameter and timing registers (RPRA/B and RTRA/B)
3. Output and miscellaneous register (OMRA/B).

The first and second group of registers define the transmitter and receiver parameters and timing. Included in the receiver timing registers are the programming parameters for the DPLL. The last register of the group, OMR contains additional transmitter and receiver information and controls the logical state of the output pins when they are not used as a part of the channel configuration.

A channel cannot be dynamically reconfigured. Do not write to the RPR if the receiver is enabled, and do not write to the TPR if the transmitter is enabled.

Table 2. Channel Configuration/Pin Definition Registers Bit Formats

CHANNEL MODE REGISTER 1

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	Data Encoding		Extended Control	Address Mode (BOP)		Channel Protocol Mode		
(CMR1A, CMR1B)	00—NRZ/Manchester 01—NRZI 10—FM0 11—FM1		BOP only 0—no 1—yes	00—8-bit 01—extended address 10—16-bit 11—16-bit w/group		000—BOP primary 001—BOP secondary 010—BOP loop 011—BOP loop - no adr. comp.		
			Parity*	Parity Mode (COP/ASYNC)				
			0—even 1—odd	00—no parity 01—reserved 10—with parity 11—force parity		100—COP dual SYN 101—COP dual SYN (BISYNC) 110—COP single SYN 111—asynchronous		

NOTE:
* In BISYNC protocol mode, 0 = EBCDIC, 1 = ASCII coding.

CHANNEL MODE REGISTER

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	Channel Connection		Data Transfer Interface			Frame Check Sequence Select		
(CMR2A, CMR2B)	00—normal 01—auto echo 10—local loop 11—reserved		000—half-duplex single address DMA 001—half-duplex dual address DMA 010—full-duplex single address DMA 011—full-duplex dual address DMA 100—wait on Rx only 101—wait on Tx only 110—wait on Rx or Tx 111—polled or interrupt			000—none 001—reserved 010—LRC8 preset 0s 011—LRC8 preset 1s 100—CRC 16 preset 0s 101—CRC 16 preset 1s 110—CRC CCITT preset 0s 111—CRC CCITT preset 1s		

SYN1/SECONDARY ADDRESS REGISTER 1

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
(S1RA, S1RB)	ASYNC—Character compare (5 - 8 bits) COP—SYN1 (5 - 8 bits) BOP—First address octet							

SYN2/SECONDARY ADDRESS REGISTER 2

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
(S2RA, S2RB)	ASYNC—not used COP—SYN2 (5 - 8 bits) BOP—Second address octet							

PIN CONFIGURATION REGISTER

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
	X2/IDS	GPO2/RTS	SYNOUT/RTS	RTxC Pin		TRxC Pin		
(PCRA, PCRB)	* 0—X2 1—IDC	0—GPO2 1—RTS	0—SYNOUT 1—RTS	00—input 01—C/T 10—TxCLK 1X 11—RxCLK 1X		000—input 001—XTAL/2 010—DPLL 011—C/T	100—TxCLK 16X 101—RxCLK 16X 110—TxCLK 1X 111—RxCLK 1X	

NOTE:
* PCRA only. Not used in PCRB.

Table 3. Transmitter and Receiver Parameter and Timing Register Bit Format

TRANSMITTER PARAMETER REGISTER

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
(TPRA, TPRB)	**Underrun Control**		**Idle**	**TEOM on Zero Cnt or Done**	**Tx RTS Control**	**CTS Enable Tx**	**Tx Character Length**	
COP	00—FCS-idle 01—reserved 10—MARKs 11 —SYNs		0—MARKs 1—SYNs	0—no 1—yes	0—no 1—yes	0—no 1—yes	00—5 bits 01—6 bits 10—7 bits 11—8 bits	
	Underrun Control		**Idle**	**TEOM on Zero Cnt or Done**				
BOP	00—FCS-FLAG-idle 01—reserved 10—ABORT-MARKs 11—ABORT-FLAGs		0—MARKs 1—FLAGs	0—no 1—yes				
	Stop Bits Per Character							
ASYNC	9/16 to 1, 17/16 to 1.5, 25/16 to 2 programmable in 1/16-bit increments							

TRANSMITTER TIMING REGISTER

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
(TTRA, TTRB)	**External Source**	**Transmitter Clock Select**			**Bit Rate Select**			
	0—RTxC 1—TRxC	000—1X external 001—16X external 010—DPLL 011—BRG 100—2X other channel C/T 101—32X other channel C/T 110—2X own channel C/T 111—32X own channel C/T			one of sixteen rates from BRG			

RECEIVER PARAMETER REGISTER

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
(RPRA, RPRB)	not used	not used	not used	**Rx RTS Control**	**Strip Parity**	**DCD Enable Rx**	**Rx Character Length**	
ASYNC				0—no 1—yes	0—no 1—yes	0—no 1—yes	00—5 bits 01—6 bits 10—7 bits 11—8 bits	
COP	**SYN Strip**	**FCS to FIFO**	**Auto Hunt & Pad Chk**	**Ext Sync**	**Strip Parity**			
	0—no 1—yes	0—no 1—yes	0—no 1—yes	0—no 1—yes	0—no 1—yes			
	not used	**FCS to FIFO**	**Overrun Mode**	not used	**All Parity Address**			
BOP		0—no 1—yes	0—hunt 1—cont		0—no 1—yes			

RECEIVER TIMING REGISTER

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
(RTRA, RTRB)	External Source	Receiver Clock Select			Bit Rate Select			
	0—RTxC 1—TRxC	000—1X external 001—16X external ⎫ ASYNC 010—BRG ⎬ protocol 011—C/T of channel ⎭ mode only 100—DPLL, source = 64X X1/CLK 101—DPLL, source = 32X External 110—DPLL, source = 32X BRG 111—DPLL, source = 32X C/T			one of sixteen rates from BRG			

OUTPUT AND MISC REGISTER

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
(OMRA, OMRB)	Tx Residual Character Length			TxRDY Activate	RxRDY Activate	OUT 2	OUT 1	RTS
	000—1 bit 001—2 bits 010—3 bits 011—4 bits 100—5 bits 101—6 bits 110—7 bits 111—same as TPR[1:0]			0—FIFO not full 1—FIFO empty	0—FIFO not empty 1—FIFO full	Bit Pin 0—H 1—L	Bit Pin 0—H 1—L	Bit Pin 0—H 1—L

Transmitter Parameter Register (TPRA, TPRB)

[7:6] Underrun Control—In BOP and COP modes, this field selects the transmitter response in the event of an underrun (i.e., the TxFIFO is empty).

00 Normal end of message termination. In BOP, the transmitter sends the FCS (if selected by CMR2[2:0]) followed by a FLAG and then either MARKs or FLAGs, as specified by [5]. In COP, the transmitter sends the FCS (if selected by CMR2[2:0]) and then either MARKs or SYNs, as specified by [5].

01 Reserved.

10 In BOP, the transmitter sends an ABORT (11111111) and then places the TxD output in a marking condition until receipt of further instructions. In COP, the transmitter places the TxD output in a marking condition until receipt of further instructions.

11 In BOP, the transmitter sends an ABORT (11111111) and then sends FLAGs until receipt of further instruction. In COP, the transmitter sends SYNs until receipt of further instructions.

[5] Idle—In BOP and COP modes, this bit selects the transmitter output during idle. Idle is defined as the state following a normal end of message until receipt of the next transmitter command.

0 Idle in marking condition.

1 Idle sending SYNs (COP) or FLAGs (BOP).

[4] Transmit EOM on Zero Count or Done—In BOP and COP modes, the assertion of this bit causes the end of message (FCS in COP, FCS-FLAG in BOP) to be transmitted upon the following events:

1. If the counter/timer is counting transmitted characters, after transmission of the character which causes the counter to reach zero count. (DONEN is also asserted as an output if the channel is in a DMA operation.)
2. If the channel is operating in DMA mode, after transmission of a character if DONEN was asserted when that character was loaded into the TxFIFO by the DMA controller.

[7:4] Stop Bits per character—In ASYNC mode, this field programs the length of the stop bit appended to the transmitted character as shown in Table 4.

Table 4. Stop Bits—Transmitted Character

[7:4]	5 BITS/CHAR	6, 7 or 8 BITS/CHAR
0000	1.063	0.563
0001	1.125	0.625
0010	1.188	0.688
0011	1.250	0.750
0100	1.313	0.813
0101	1.375	0.875
0110	1.438	0.938
0111	1.500	1.000
1000	1.563	1.563
1001	1.625	1.625
1010	1.688	1.688
1011	1.750	1.750
1100	1.813	1.813
1101	1.875	1.875
1110	1.938	1.938
1111	2.000	2.000

Stop bit lengths of 9/16 to 1 and 1-9/16 to 2 bits, in increments of 1/16-bit, can be programmed for character lengths of 6, 7, and 8 bits. For a character length of 5 bits, 1-1/16 to 2 stop bits can be programmed in increments of 1/16-bit. The receiver only checks for a 'mark' condition at the center of the first stop bit position (one bit time after the last data bit, or after the parity bit if parity is enabled) in all cases.

If an external 1X clock (or a 2X clock for counter/timer) is used for the transmitter, [7] = 0 selects one stop bit and [7] = 1 selects two stop bits to be transmitted. If Manchester, NRZI, or FM data encoding is selected, only integral stop bit lengths should be used.

[3] Transmitter Request-to-Send Control—This bit controls the deactivation of the RTSN output by the transmitter (see Detailed Operation).

0 RTSN is not affected by status of transmitter.

1 RTSN changes state as a function of transmitter status.

[2] Clear-to-Send Enable Transmitter—The state of this bit determines if the CTSN input controls the operation of the channel's transmitter (see Detailed Operation). The duration of CTS level change is described in the discussion of ICTSR[4].

0 CTSN has no affect on the transmitter.

1 CTSN affects the state of the transmitter.

[1:0] Transmitted Bits per Character—This field selects the number of data bits per character to be transmitted. The character length does not includes the start, parity, and stop bits in ASYNC or the parity bit in COP. In BOP modes the character length for the address and control field is always 8 bits, and the value of this field only applies to the information (I) field, except for the last character of the I field, whose length is specified by OMR[7:5].

Transmitter Timing Register (TTRA, TTRB)

[7] External Source—This bit selects the RTxC pin or the TRxC pin of the channel as the transmitter clock input when [6:4] specifies external. When used for input, the selected pin must be programmed as an input in the PCR [4:3] or [2:0].

0 External input form RTxC pin.

1 External input from TRxC pin.

[6:4] Transmitter Clock Select—This field selects the clock for the transmitter.

000 External clock from TRxC or RTXC at 1X the shift (baud) rate.

001 External clock from TRXC or RTxC at 16X the shift rate.

010 Internal clock from the phase-locked loop at 1X the bit rate. It should be used only in half-duplex operation since the DPLL will periodically resync itself to the received data if in full-duplex operation.

011 Internal clock from the bit rate generator at 32X the shift rate. The clock signal is divided by two before use in the transmitter which operates at 16X the baud rate. Rate selected by [3:0].

100 Internal clock from counter/timer of other channel. The C/T should be programmed to produce a clock at 2X the shift rate.

101 Internal clock from counter/timer of other channel. The C/T should be programmed to produce a clock at 32X the shift rate.

110 Internal clock from the counter/timer of own channel. The C/T should be programmed to produce a clock at 2X the shift rate.

111 Internal clock from the counter/timer of own channel. The C/T should be programmed to produce a clock at 32X the shift rate.

[3:0] Bit Rate Select—This field selects an output from the bit rate generator to be used by the transmitter circuits. The actual frequency output from the BRG is 32X the bit rate shown in Table 5. With a crystal or external clock of 14.7456MHz the bit rates are as given in Table 5 (this input is divided by two before being applied to the oscillator circuit).

Table 5. Receiver/Transmitter Baud Rates

[3:0]	BIT RATE	[3:0]	BIT RATE
0000	50	1000	1050
0001	75	1001	1200
0010	110	1010	2000
0011	134.5	1011	2400
0100	150	1100	4800
0101	200	1101	9600
0110	300	1110	19.2K
0111	600	1111	38.4K

Receiver Parameter Register (RPRA, RPRB)

[7] SYN Stripping—This bit controls the DUSCC processing in COP modes of SYN 'character patterns' that occur after the initial character synchronization. Refer to Detailed Operation of the receiver for details and definition of SYN 'patterns', and their accumulation of FCS.

0 Strip only leading SYN 'patterns' (i.e. before a message).

1 Strip all SYN 'patterns' (including all odd DLE's in BISYNC transparent mode).

[6] Transfer Received FCS to FIFO—In BISYNC and BOP modes, the assertion of this bit causes the received FCS to be loaded into the RxFIFO. When this bit is set, BOP mode operates correctly only if a minimum of two extra FLAGs (without shared zeros) are appended to the frame. If the FCS is specified to be transferred to the FIFO, the EOM status bit will be tagged onto the last byte of the FCS instead of to the last character of the message.

0 Do not transfer FCS to RxFIFO.

1 Transfer FCS to RxFIFO.

[5] Auto-Hunt and Pad Check (BISYNC)—In BISYNC mode, the assertion of this bit causes the receiver to go into hunt for character sync mode after detecting certain End-Of-Message (EOM) characters. These are defined in the Detailed Operations section for COP receiver operation. After the EOT and NAK sequences, the receiver also does a check for a closing PAD of four 1s.

0 Disable auto-hunt and PAD check.

1 Enable auto-hunt and PAD check.

[5] Overrun Mode (BOP)—The state of this control bit determines the operation of the receiver in the event of a data overrun, i.e., when a character is received while the RxFIFO and the Rx shift register are both full.

0 The receiver terminates receiving the current frame and goes into hunt phase, looking for a FLAG to be received.

1 The receiver continues receiving the current frame. The overrunning character is lost. (The five characters already assembled in the RxFIFO and Rx shift register are protected).

[4] Receiver Request-to-Send Control (ASYNC)—See Detailed Operation.

0 Receiver does not control RTSN output.

1 Receiver can negate RTSN output.

[4] External Sync (COP)—In COP single SYN mode, the assertion of this bit enables external character synchronization and receipt of SYN patterns is not required. In order to use this feature, the DUSCC must be programmed to COP single SYN mode, CMR 1[2:0] = 110, which is used to set up the internal data paths. In all other respects, however, the external sync mode operation is protocol transparent. A negative signal on the DCDN/SYNIN pin will cause the receiver to establish synchronization on the next rising edge of the receiver clock. Character assembly will start at this edge with the RxD input pin considered to have the second bit of data. The sync signal can then be negated. Receipt of the Active-High external sync input causes the SYN detect status bit (RSR[2]) to be set and the SYNBOUTN pin to be asserted for one bit time. When this mode is enable, the internal SYN (COP mode) detection and special character recognition (e.g., IDLE, STX, ETX, etc.) circuits are disabled. Character assembly begins as if in the I-field with character length as programmed in RPR[1:)]. Incoming COP frames with parity specified optionally can have it stripped by programming RPR[3]. The user must wait at least eight bit times after Rx is enabled before applying the SYNIN signal. This time is required to flush the internal data paths. The receiver remains in this mode and further external sync pulses are ignored until the receiver is disabled and then reenabled to resynchronize or to return to normal mode. See Figure 2.

0 External sync not enabled.

1 External sync enabled.

Note that EXT SYNC and DCD ENABLE Rx cannot be asserted simultaneously since they use the same pin.

[3] Strip Parity—In COP and ASYNC modes with parity enabled, this bit controls whether the received parity bit is stripped from the data placed in the receiver FIFO. It is valid only for programmed character lengths of 5, 6, and 7 bits. If the bit is stripped, the corresponding bit in the received data is set to zero.

0 Transfer parity bit as received.

1 Stop parity bit from data.

[3] All Parties Address—In BOP secondary modes, the assertion of this bit causes the receiver to 'wake-up' upon receipt of the address H'FF' or H'FF, FF', for single- and dual-octet address modes, respectively, in addition to its normal station address. This feature allows all stations to receive a message.

0 Don't recognize all parties address.

1 Recognize all parties address.

[2] DCD Enable Receiver—If this bit is asserted, the DCDN/SYNIN input must be Low in order for the receiver to operate. If the input is negated (goes High) while a character is being received, the receiver terminates receipt of the current message (this action in effect disables the receiver). If DCD is subsequently asserted, the receiver will search for the start bit, SYN pattern, or FLAG, depending on the channel protocol. (Note that the change of input can be programmed to generate an interrupt; the duration of the DCD level change is described in the discussion of the input and counter/timer status register (CTSR[5]).

0 DCD not used to enabled receiver.

1 DCD used to enabled receiver.

EXT SYNC and DCD ENABLE Rx cannot be asserted simultaneously since they use the same pin.

[1:0] Received Bits per Character—This field selects the number of data bits per character to be assembled by the receiver. The character length does not include the start, parity, and stop bits in the ASYNC or the parity bit in COP. In BOP modes, the character length for the address and control field is always 8 bits, and the value of this field only applies to the information field. If the number of bits assembled for the last character of the I-field is less than the value programmed in this field, RCL not zero (RSR[0]) is asserted and the actual number of bits received is given in TRSR[2:0].

Receiver Timing Register (RTRA, RTRB)

[7] External Source—This bit selects the RTxC pin or the TRxC pin of the channel as the receiver or DPLL clock input, when [6:4] specifies external. When used for input, the selected pin must be programmed as an input in the PCR [4:3] or [2:0].

0 External input form RTxC pin.

1 External input form TRxC pin.

[6:4] Receiver Clock Select—This field selects the clock for the receiver.

000 External clock from TRxC or RTxC at 1X the shift (baud) rate.

001 External clock from TRxC or RTxC at 16X the shift rate. Used for ASYNC mode only.

010 Internal clock from the bit rate generator at 32X the shift rate. Clock is divided by two before used by the receiver logic, which operates at 16X the baud rate. Rate selected by [3:0]. Used for ASYNC mode only.

011 Internal clock from counter/timer of own channel. The C/T should be programmed to produce a clock at 32X the shift rate. Clock is divided by two before use in the receiver logic. Used for ASYNC mode only.

100 Internal clock from the digital phase-locked loop. The clock for the DPLL is a 64X clock from the crystal oscillator or system clock input. (The input to the oscillator is divided by two).

101 Internal clock from the digital phase-locked loop. The clock for the DPLL is an external 32X clock from the RTxC or TRxC pin, as selected by [7].

110 Internal clock from the digital phase-locked loop. The clock for the DPLL is a 32X clock from the BRG. The frequency is programmed by [3:0].

111 Internal clock from the digital phase-locked loop. The clock for the DPLL is a 32X clock from the counter/timer of the channel.

[3:0] Bit Rate Select—This field selects an output from the bit rate generator to be used by the receiver circuits. The actual frequency output from the BRG is 32X the bit rate shown in Table 5.

Output and Miscellaneous Register (OMRA, OMRB)

[7:5] Transmitted Residual Character Length—In BOP modes, this field determines the number of bits transmitted for the last character in the information field. This length applies to:

- The character in the transmit FIFO accompanied by the FIFOed TEOM command.
- The character loaded into the FIFO by the DMA controller if DONEN is simultaneously asserted and TPR[4} is asserted.

- The character loaded into the FIFO which causes the counter to reach zero count when TPR[4] is asserted.

The length of all other characters in the frame's information field is selected by TPR[1:0]. If this field is 111, the number of bits in the last character is the same as programmed in TPR[1:0].

[4] TxRDY Activate Mode—

0 FIFO not full. The channel's TxRDY status bit is asserted each time a character is transferred from the transmit FIFO to the transmit shift register. If not reset by the CPU, TxRDY remains asserted until the FIFO is full, at which time it is automatically negated.

1 FIFO empty. The channel's TxRDY status bit is asserted when a character transfer from the transmit FIFO to the transmit shift register causes the FIFO to become empty. If not reset by the CPU, TxRDY remains asserted until the FIFO is full, at which time it is negated.

If the TxRDY status bit is reset by the CPU, it will remain negated regardless of the current state of the transmit FIFO, until it is asserted again due to the occurrence of one of the above conditions.

[3] RxRDY Activate Mode—

0 FIFO not empty. The channel's RxRDY status bit is asserted each time a character is transferred from the receive shift register to the receive FIFO. If not reset by the CPU, RxRDY remains asserted until the receive FIFO is empty, at which time it is automatically negated.

1 FIFO full. The channel's RxRDY status bit is asserted when a character transfer from the receive shift register to the receive FIFO causes the FIFO to become full. If not reset by the CPU, RxRDY remains asserted until the FIFO is empty, at which time it is negated.

The RxRDY status bit will also be asserted, regardless of the receiver FIFO full condition, when an end-of-message character is loaded in the RxFIFO (BOP/BISYNC), when a BREAK condition (ASYNC mode) is detected in RSR[2], or when the counter/timer is programmed to count received characters and the character which causes it to reach zero is loaded in the FIFO (all modes). (Refer to the Detailed Operation of the receiver.)

If reset by the CPU, the RxRDY status bit will remain negated, regardless of the current state of the receiver FIFO, until it is asserted again due to one of the above conditions.

[2] General Purpose Output 2—This general purpose bit is used to control the TxDRQN/GPO2/RTSN pin, when it is used as an output. The output is High when the bit is a 0 and is Low when the bit is a 1.

[1] General Purpose Output 1—This bit is used to control the RTxDRQN/GPO1N output, which is a general purpose output when the channel is not in DMA mode. The output is High when the bit is a 0 and is Low when the bit is a 1.

[0] Request-to-Send Output—This bit controls the TxDRQN/GPO2N/RTSN and SYNOUTN/RTSN pin, when either is used as a RTS output. The output is High when the bit is a 0 and is Low when the bit is a 1.

Counter/Timer Control and Value Registers

There are five registers in this set consisting of the following:

1. Counter/timer control register (CTCRA/B).
2. Counter/timer preset Highland Low registers (CTPRHA/B, CTPRLA/B).
3. Counter/timer (current value) High and Low registers (CTHA/B, CTLA/B)

The format of each of the registers of this set is contained in Table 6. The control register contains the operational information for the counter/timer. The preset registers contain the count which is loaded into the counter/timer circuits. The third group contains the current value of the counter/timer as it operates.

Counter/Timer Control Register (CTCRA/CTCRB)

[7] Zero Detect Interrupt—This bit determines whether the assertion of the C/T ZERO COUNT status bit (ICTSR[6]) causes an interrupt to be generated.

0 Interrupt disabled.

1 Interrupt enabled if master interrupt enabled (ICR[1] or ICR[0]) is asserted.

[6] Zero Detect Control—This bit determines the action of the counter upon reaching zero count.

0 The counter/timer is preset to the value contained in the counter/timer preset registers (CTPRL, CTPRH) at the next clock edge.

1 The counter/timer continues counting without preset. The value at the next clock edge will be H'FFFF'.

[5] Counter/Timer Output Control—This bit selects the output waveform when the counter/timer is selected to be output on TRxC or RTxC.

1 The output is a single clock positive width pulse each time the C/T reaches zero count. (The duration of this pulse is one clock period.)

0 The output toggles each time the C/T reaches zero count. The output is cleared to Low by either of the preset counter/timer commands.

[4:3] Clock Select—This field selects whether the clock selected by [2:0] is prescaled prior to being applied to the input of the C/T.

00 No prescaling.

01 Divide clock by 16.

10 Divide clock by 32.

11 Divide clock by 64.

[2:0] Clock Source—This field selects the clock source for the counter/timer.

000 RTxC pin. Pin must be programmed as input.

001 TRxC pin. Pin must be programmed as input.

010 Source is the crystal oscillator or system clock input divided by four.

011 This selects a special mode of operation. In this mode the counter, after receiving the 'start C/T' command, delays the start of counting until the RxD input goes Low. It continues counting until the RxD input goes High, then stops and sets the C/T zero count status bit. The CPU can use the value in the C/T to determine the bit rate of the incoming data. The clock is the crystal oscillator or system clock input divided by four

100 Source is the 32X BRG output selected by RTR[3:0] of own channel.

101 Source is the 32X BRG output selected by TTR[3:0] of own channel.

110 Source is the internal signal which loads received characters from the receive shift register into the receiver FIFO. When operating in this mode, the FIFOed EOM status bit (RSR[7]) shall be set when the character which

causes the count to go to zero is loaded into the receive FIFO.

111 Source is the internal signal which transfers characters from the data bus into the transmit FIFO. When operating in this mode, and if the TEOM on zero count or done control bit (TPR[4]) is asserted, the FIFOed send EOM command will be automatically asserted when the character which causes the count to go to zero is loaded into the transmit FIFO.

Table 6. Counter/Timer Control and Value Register Bit Formats

COUNTER/TIMER CONTROL REGISTER

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
(CTCRA, CTCRB)	Zero Detect Interrupt	Zero Detect Control	Output Control	Prescaler		Clock Source		
	0—disable 1—enabled	0—preset 1—continue	0—square 1—pulse	00—1 01—16 10—32 11—64		000—RTxC pin 001—TRxC pin 010—X1/CLK divided by 4 011—X1/CLK divided by 4 gated by RxD 100—Rx BRG 101—Tx BRG 110—Rx characters 111—Tx characters		

COUNTER/TIMER PRESET REGISTER HIGH

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
(CTPRHA, CTPRHB)	Most significant bits of counter/timer preset value.							

COUNTER/TIMER PRESET REGISTER LOW

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
(CTPRLA, CTPRLB)	Least significant bits of counter/timer preset value.							

COUNTER/TIMER REGISTER HIGH

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
(CTHA, CTHB)	Most significant bits of counter/timer.							

COUNTER/TIMER REGISTER LOW

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
(CTLA, CTLB)	Least significant bits of counter/timer.							

Counter/Timer Preset High Register (CTPRHA, CTPRHB)

[7:0] MSB—This register contains the eight most significant bits of the value loaded into the counter/timer upon receipt of the load C/T from preset register command or when the counter/timer reaches zero count and the zero detect control bit (CTCR[6]) is negated. The minimum 16-bit counter/timer preset value is H'0002'.

Counter/Timer Preset Low Register (CTPRLA, CTPRLB)

[7:0] LSB—This register contains the eight least significant bits of the value loaded into the counter/timer upon receipt of the load C/T from preset register command or when the counter/timer reaches zero count and the zero detect control bit (CTCR[6]) is negated. The minimum 16-bit counter/timer preset value is H'0002'.

Counter/Timer High Register (CTHA, CTHB)

[7:0] MSB—A read of this 'register' provides the eight most significant bits of the current value of the counter/timer. It is recommended that the C/T be stopped via a stop counter command before it is read in order to prevent errors which may occur due to the read being performed while the C/T is changing. This count may be continued after the register is read.

Counter/Timer Low Register (CTLA, CTLB)

[7:0] LSB—A read of this 'register' provides the eight least significant bits of the current value of the counter/timer. It is recommended that the C/T be stopped via a stop counter command before it is read, in order to prevent errors which may occur due to the read being performed while the C/T is changing. This count may be continued after the register is read.

Interrupt Control and Status Registers

This group of registers define mechanisms for communications between the DUSCC and the processor and contain the device status information. Four registers, available for each channel, and four common device registers comprise this group which consists of the following:

1. Interrupt Enable Register (IERA/B).
2. Receiver Status Register (RSRA/B).
3. Transmitter and Receiver Status Register (TRSRA/B).
4. Input and Counter/Timer Status Register (ICTSRA/B).
5. Interrupt Vector Register (IVR) and Modified Interrupt Vector Register (IVRM).
6. Interrupt control register (ICR).
7. General status register (GSR)

See Table 7 for bit formats and Figure 3 for table relationships.

Interrupt Enable Register (IERA, IERB)

This register controls whether the assertion of bits in the channel's status registers causes an interrupt to be generated. An additional condition for an interrupt to be generated is that the channel's master interrupt enabled bit, ICR[0] or ICR[1], be asserted.

[7] DCD/CTS—

0 Interrupt not enabled.

1 Interrupt generated if ICTSR[4] or ICTSR[5] are asserted.

[6] TxRDY—

0 Interrupt not enabled.

1 Interrupt generated if TxRDY (GSR[1] or GSR[5] for Channels A and B, respectively) is asserted.

[5] TRSR 73—

0 Interrupt not enabled.

1 Interrupt generated if bits 7, 6, 5, 4 or 3 of the TRSR are asserted.

[4] RxRDY—

0 Interrupt not enabled.

1 Interrupt generated if RxRDY (GSR[0] or GSR[4] for Channels A and B, respectively) is asserted.

[3] RSR 76—

0 Interrupt not enabled.

1 Interrupt generated if bits 7 or 6 of the RSR are asserted.

[2] RSR 54—

0 Interrupt not enabled.

1 Interrupt generated if bits 5 or 4 of the RSR are asserted.

[1] RSR 32—

0 Interrupt not enabled.

1 Interrupt generated if bits 3 or 2 of the RSR are asserted.

[0] RSR 10—

0 Interrupt not enabled.

1 Interrupt generated if bits 1 or 0 of the RSR are asserted.

Table 7. Interrupt Control and Status Register Bit Format

RECEIVER STATUS REGISTER

	BIT 7[1]	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
(RSRA, RSRB) ASYNC	Char compare[2]	RTS negated	Overrun error	not used	BRK end detect	BRK start detect	Framing error[2]	Parity error[2]
COP	EOM detect[2,3]	PAD error[3]	Overrun error	not used	not used	Syn detect	CRC error[2]	Parity error[2]
BOP	EOM detect[2]	Abort detect	Overrun error	Short frame detect	Idle detect	Flag detect	CRC error[2]	RCL not zero[2]
LOOP	EOM detect[2]	Abort/EOP detect	Overrun error	Short frame detect	Turn-around detect	Flag detect	CRC error[2]	RCL not zero[2]

TRANSMITTER AND RECEIVER STATUS REGISTER

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
(TRSRA, TRSRB) ASYNC	Transmitter empty	CTS underrun	not used	Send break ack	DPLL error	not used	not used	not used
COP	Transmitter empty	CTS underrun	Frame complete	Send SOM ack	DPLL error	not used	Rx hunt mode	Rx xpnt mode
BOP	Transmitter empty	CTS underrun Loop sending[4]	Frame complete	Send SOM/ abort ack	DPLL error	Rx Residual Character Length 000—0 bit 001—1 bits 010—2 bits 011—3 bits 100—4 bits 101—5 bits 110—6 bits 111—7 bits		

Table 7. Interrupt Control and Status Register Bit Format (Continued)

INPUT AND COUNTER/TIMER STATUS REGISTER

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
(ICTSRA, ICTSRB)	C/T running	C/T zero count	Delta DCD	Delta CTS/LC	DCD	CTS/LC	GPI2	GPI1

INTERRUPT ENABLE REGISTER

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
(IERA, IERB)	**DCD/CTS**	**TxRDY**	**TRSR [7:3]**	**RxRDY**	**RSR[7:6]**	**RSR [5:4]**	**RSR [3:2]**	**RSR [1:0]**
	0—no 1—yes	0—no 1—yes	0—no 1—yes	0—no 1—yes	0—no 1—yes	0—no 1—yes	0—no 1—yes	0—no 1—yes

INTERRUPT VECTOR REGISTER AND INTERRUPT VECTOR MODIFIED REGISTER

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
(IVR, IVRM)	8-bit interrupt vector							

GENERAL STATUS REGISTER

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
(GSR)	**Channel B**				**Channel A**			
	External or C/T Status	Rx/Tx status	TxRDY	RxRDY	External or C/T status	Rx/Tx status	TxRDY	RxRDY

INTERRUPT CONTROL REGISTER

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
(ICR)	**Channel A/B Interrupt Priority**		**Vector Mode**		**Bits to Modify**	**Vector Includes Status**	**Channel A Master Int Enable**	**Channel B Master Int Enable**
	00—Channel A 01—Channel B 10—interleaved A 11—interleaved B		00—vectored 01—vectored 10—vectored 11—non vectored		0—2:0 1—4:2	0—no 1—yes	0—no 1—yes	0—no 1—yes

NOTES:
1. All modes indicate character count complete.
2. Status bit is FIFOed.
3. COP BISYNC mode only
4. Loop mode only.

Receiver Status Register (RSRA, RSRB)

This register informs the CPU of receiver status. Bits indicated as 'not used' in a particular mode will read as zero. The logical OR of these bits is presented in GSR[2] or GSR[6] (ORed with the bits of TRSR) for Channels A and B, respectively. Unless otherwise indicated, asserted status bits are reset only be performing a write operation to the status register with the bits to be reset being ones in the accompanying data word, or when the RESETN input is asserted, or when a 'reset receiver' command is issued.

Certain status bits are specified as being FIFOed. This means that they occupy positions in a status FIFO that correspond to the data FIFO. As the data is brought to the top of the FIFO (the position read when the RxFIFO is read), the FIFOed status bits are logically ORed with the previous contents of the corresponding bits in the status register. This permits the user to obtain status either character by character or on a block basis. For character by character status, the SR bits should be read and then cleared before reading the character data from RxFIFO. For block status, the status register is initially cleared and then read after the message is received. Asserted status bits can be programmed to generate an interrupt (see Interrupt Enable Register).

[7] Character Count Complete (All Modes), Character compare (ASYNC), EOM (BISYNC/BOP/LOOP)—If the counter/timer is programmed to count received characters, this bit is asserted when the character which causes the count to go to zero is loaded into the receive FIFO. It is also asserted to indicate the following conditions:

ASYNC The character currently at the top of RxFIFO matched the contents of S1R. A character will not compare if it is received with parity error even if the data portion matches.

BISYNC The character currently at the top of the FIFO was either a text message terminator or a control sequence received outside of a text or header field. See Detailed Operation of COP Receiver. If transfer FCS to FIFO (RPR[6]) is set, the EOM will instead be tagged onto the last byte of the FCS. Note that if an overrun occurs during receipt of a message, the EOM character may be lost, but this status bit will still be asserted to indicate that an EOM was received. For 2 byte EOM comparisons, only the second byte is tagged (assuming the CRC is not transferred to the FIFO).

BOP, LOOP The character currently at the top of the FIFO was the last character of the frame. If transfer FCS to FIFO (RPR[6]) is asserted, the EOM will be tagged instead onto the last byte of the FCS. Note that if an overrun occurs, the EOM character may be lost, but this status bit will still be asserted to indicate that an EOM was received. This bit will not be set when an abort is received.

[6] RTS Negated (ASYNC), PAD Error (BISYNC), ABORT (BOP)—

ASYNC The RTSN output was negated due to receiving the start bit of a new character while the RxFIFO was full (see RPR[4]).

BISYNC PAD error detected (see RPR[5]).

LOOP An ABORT sequence consisting of a zero followed by seven ones was received after receipt of the first address octet but before receipt of the closing FLAG. The user should read RxFIFO until it is empty and determine if any valid characters from a previous frame are in the FIFO. If no character with a tagged EOM detect ([7]) is found, all characters are from the current frame and should be discarded along with any previously read by the CPU. An ABORT detect causes the receiver to automatically go into search for FLAG state. An abort during a valid frame does not cause the CRC to reset; this will occur when the next frame begins.

LOOP Performs the ABORT detect function as described for BOP without the restriction that the pattern be detected during an active frame. A zero followed by seven ones is the end-of-poll sequence which allows the transmitter to go active if the 'go active on poll' command has been invoked.

[5] Overrun Error (All Modes)—A new character was received while the receive FIFO was full and a character was already waiting in the receive shift register to be transferred to the FIFO. the DUSCC protects the five characters previously assembled (four in RxFIFO, one in the Rx shift register) and discards the overrunning character(s). After the CPU reads the FIFO, the character waiting in the RxSR will be loaded into the available FIFO position. This releases the RxSR and a new character assembly will start at the next character boundary. In this way, only valid characters will be assembled, i.e., no partial character assembly will occur regardless of when the RxSR became available during the incoming data stream.

[4] Short Frame (BOP/LOOP)—

ASYNC Not used

COP Not used

BOP, LOOP A closing flag was received with missing fields in the frame. See detailed operation for BOP receiver.

[3] BREAK End Detect (ASYNC), IDLE (BOP), Turnaround (LOOP)—

ASYNC 1X clock mode: The RxD input has returned to the marking state for at least one period of the 1X receiver clock after detecting a BREAK. 16X clock mode: The RxD input has returned to the marking (High) state for a least one-half bit time after detecting a BREAK. A half-bit time is defined as eight clock cycles of the 16X receiver clock.

COP Not used.

BOP An IDLE sequence consisting of a zero followed by fifteen ones was received. During a valid frame, an abort must precede an idle. However, outside of a valid frame, an idle is recognized and abort is not.

LOOP A turnaround sequence consisting of eight contiguous zeros was detected outside of an active frame. This should normally be used to terminate transmitter operation and return the system to the 'echoing RxD' mode.

[2] BREAK Start Detect (ASYNC), SYN Detect (COP), FLAG Detect (BOP/LOOP)—

ASYNC An all zero character, including parity (if specified) and first stop bit, was received. The receiver shall be capable of detecting breaks which begin in the middle of a previous character. Only a single all-zero character shall be put into the FIFO when a break is detected. Additional entries to the FIFO are inhibited until the end of break has been detected (see above) and a new character is received.

COP A SYN pattern was received. Refer to Detailed Operation for definition of SYN patterns. Set one bit time after detection of SYN pattern in HSRH, HSRL. See Figure 1 for receiver data path.

BOP, LOOP A FLAG frequency (01111110) was received. Set one bit time after FLAG is detected in CCSR. See Figure 1 for receiver data path.

[1] Framing Error (ASYNC), CRC Error (COP/BOP/LOOP)—

ASYNC At the first stop bit position the RxD input was in the Low (space) state. The receiver only checks for framing error at the nominal center of the first stop bit regardless of the number of stop bits programmed in TPR[7:4]. This bit is not set for BREAKS.

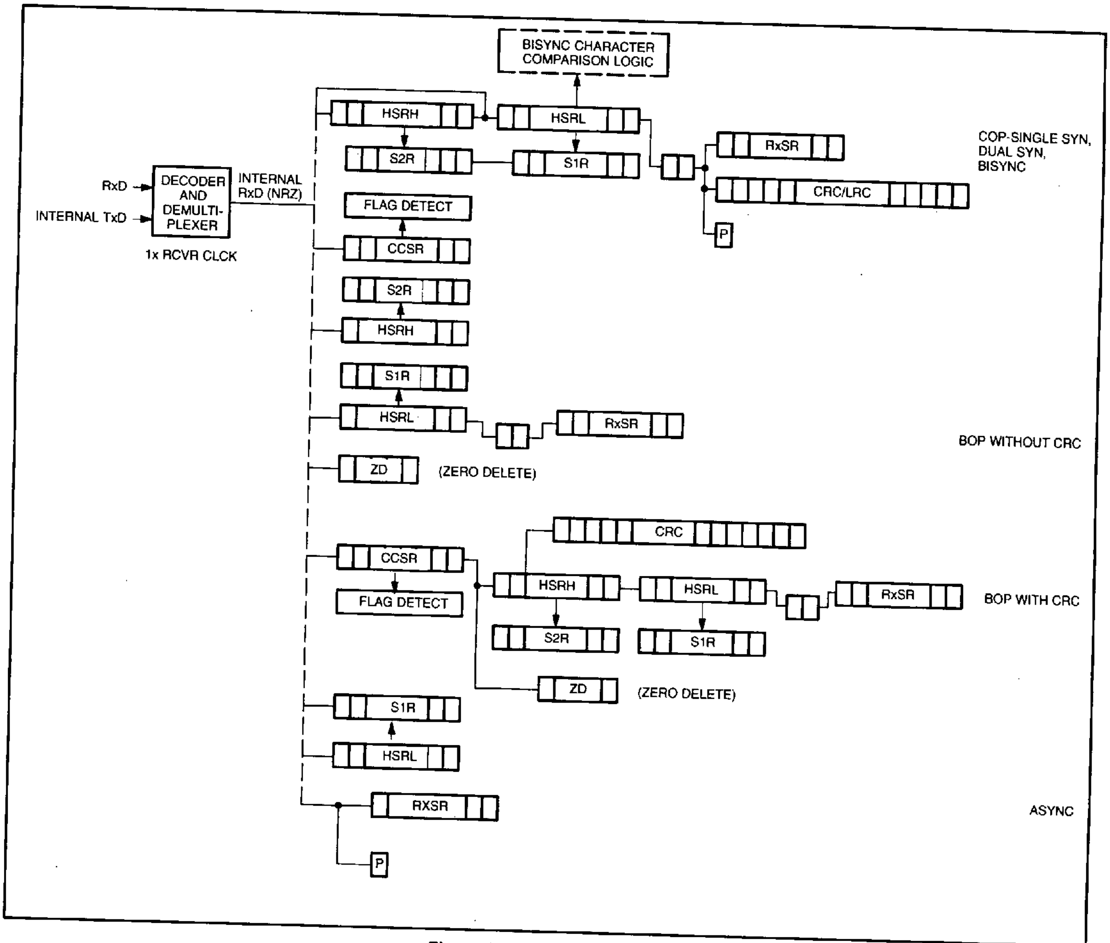


Figure 1. Receiver Data Path

COP — In BISYNC COP mode, this bit is set upon receipt of the BCC byte(s), if any, to indicate that the received BCC was in error. The bit is normally FIFOed with the last byte of the frame (the character preceding the first BCC byte). However, if transfer FCS to FIFO (RPR[6]) is asserted, this bit is FIFOed with the last BCC byte. The value of this bit should be ignored for non-test messages or if the received frame was aborted via an ENQ. In non-BISYNC COP modes, the bit is set with each received character if the current value of the CRC checker is not equal to the non-error value (see CMR2[2:0]).

BOP, LOOP — This bit is set upon receipt of the FCS byte(s), if any, to indicate that the received FCS was in error. The bit is normally FIFOed with the last byte of the I field (the character preceding the first FCS byte). However, if transfer FCS to FIFO (RPR[6]) is asserted, this bit is FIFOed with the last FCS byte.

[0] Parity Error (ASYNC/COP), RCL Not Zero (BOP/LOOP)—

ASYNC — The parity bit of the received character was not as expected. A parity error does not affect the parity bit put into the FIFO as part of the character when strip parity (RPR[3]) is negated.

COP — The parity bit of the received character was not as expected. A parity error does not affect the parity bit put into the FIFO as part of the character when strip parity (RPR[3]) is negated. A SYN or other character received with parity error is treated as a data character. Thus, a SYN with parity error received while in SYN search state will not establish character sync. Characters received with parity error while in the SYN search state will not set the error bit.

BOP, LOOP — The last character of the I field did not have the character length specified in RPR[1:0]. The actual received character length of this byte can be read in TRSR[2:0]. This bit is FIFOed with the EOM character but TRSR[2:0] is not. An exception occurs if the command to transfer the FCS to the FIFO is active. In this case, the bit will be FIFOed with the last byte of the FCS, i.e., with REOM. In the event that residual characters from two consecutive frames are received and are both in the FIFO, the length in TRSR[2:0] applies to the last received residual character.

Transmitter/Receiver Status Register (TRSRA, TRSRB)

This register informs the CPU of transmitter and receiver status. Bits indicated as not used in a particular mode will read as zero, except for bits [2:0], which may not be zero. The logical-OR of bits [7:3] is presented in GSR[2] or GSR[6] (ORed with the bits of RSR) for channels A and B, respectively. Unless otherwise indicated, asserted status bits are reset only:

1. By performing a write operation to the status register with the bits to be reset being ones in the accompanying data word [7:3].
2. When the RESETN input is asserted.
3. For [7:4], when a 'reset transmitter' command is issued.
4. For [3:0], when a 'reset receiver' command is issued.
5. For [2:0], see description in BOP mode.

Asserted status bits in [7:3] can be programmed to generate an interrupt. See IER.

[7] Transmitter Empty—Indicates that the transmit shift register has completed serializing a character and found no other character to serialize in the TxFIFO. The bit is not set until at least one character from the transmit FIFO (not including PAD characters in synchronous modes) has been serialized. The transmitter action after transmitter empty depends on operating mode:

ASYNC The TxD output is held in the MARK state until another character is loaded into the TxFIFO. Normal operation then continues.

COP Action is specified by TPR[7:6].

BOP, LOOP Action is specified by TPR[7.6].

[6] CTS Underrun (ASYNC/COP/BOP), Loop sending (LOOP)—

ASYNC, COP, BOP This bit is set only if CTS enable Tx (TPR[2]) is asserted. It indicates that the transmit shift register was ready to begin serializing a character and found the CTSN input negated. In ASYNC mode, this bit will be reasserted if cleared by the CPU while the CTSN input is negated.

LOOP Asserted when the go active on poll command has been invoked and an EOP sequence has been invoked and an EOP sequence has been detected, causing the transmitter to go active by changing the EOP to a FLAG (see Detailed Operation of transmitter).

[5] Frame Complete (COP/BOP)—

ASYNC Not used.

COP Asserted at the beginning of transmission of the end of message sequence invoked by which is either a TEOM command, or when TPR[4] = 1, or TPR[7:6] = 00. The CPU can invoke the TSOM command after this bit is set to control the number of SYNs between transmitted frames.

BOP Asserted at the beginning of transmission of the end of message sequence which is invoked by either a TEOM command, or when TPR[4] = 1, or TPR[7:6] = 00. The CPU can invoke the TSOM command after this bit is set to control the number of FLAGs between transmitted frames. In COP/BOP modes, the frame complete status bit is set during the next-to-last bit (on TxD pin) of the last character in the data/information field. In BOP mode, if a 1-bit residual character is selected through OMR[7:5], then this bit is set during the next-to-last bit (on TxD pin) of the last full length character of the information field.

[4] Send Break Ack (ASYNC)/Send SOM ACK (COP)/Send SOM-Abort Ack (BOP—

ASYNC Set when the transmitter begins transmission of a break in response to the send break command. If the command is reinvoked, the bit will be set again at the beginning of the next character time. The user can control the length of the break by counting character times through this mechanism.

COP Set when the transmitter begins transmission of a SYN pattern in response to the TSOM or TSOMP command. If the command is reinvoked, the bit will be set again at the beginning of the next transmitted SYN pattern. The user can control the number of SYNs which are sent through this mechanism.

BOP Set when the transmitter begins transmission of a FLAG/ABORT in response to the TSOM or TSOMP or TABRK command. If the command is reinvoked, the bit will be set again at the beginning of the next transmitted FLAG/ABORT. The user can control the number of FLAGs/ABORTs which are sent through this mechanism

[3] DPLL Error—Set while the DPLL is operating in FM mode to indicate that a data transition was not detected within the detection window for two consecutive bits and that the DPLL was forced into search mode. This feature is disabled when the DPLL is specified as the clock source for the transmitter via TTR[6:4].

[2:0] Received Residual Character Length (BOP)—

BOP This field should be examined to determine the length of the last character of the I field (character tagged with REOM status bit) if RSR[0] is set to indicate that the length was not equal to the character length specified in RPR[1:0]. This field is negated when a reset receiver or disabled receiver command is issued, or when the first control character for the next frame of data is in HSRL (see Figure 1). Care must be taken to read TRSR[2:0] before these bits are cleared.

[1] Receiver in Hunt Mode (COP)—

COP This bit is asserted after the receiver is reset or disabled. It indicates that the receiver is in the hunt mode, searching the data stream for a SYN sequence to establish character synchronization. The bit is negated automatically when character sync is achieved.

[0] Receiver in Transparent Mode (BISYNC)—

COP Indicates that a DLE-STX sequence was received and the receiver is operating in BISYNC transparent mode. Set two bit times after detection of STX in HSRL. See Figure 1 for receiver data path. Transparent mode operation is terminated and the bit is negated automatically when one of the terminators for transparent text mode is received (DLE-ETX/ETB/ITB/ENQ).

Input and Counter/Timer Status Register (ICTSRA, ICTSRB)

This register informs the CPU of status of the counter/timer and inputs. The logical-OR of bits [6:4] is presented in GSR[3] or GSR[7] for Channels A and B, respectively. Unless otherwise specified, bits of this register are reset only:

1. By performing a write operation to the status register with the bits to be reset (ones in the accompanying data word for bits [6:4] only)

2. When the RESETN input is asserted (bits [7:4]) only.

[7] Counter/Timing Running—Set when the C/T is started by start C/T command and reset when it is stopped by a stop C/T command.

[6] Counter/Timer Zero Detect—Set when the counter/timer reaches zero count, or when the bit length measurement is enabled (CTCR [2:0] = 011) and the RxD input has returned High. The assertion of this bit causes an interrupt to be generated if ICTCR[7] and the channel's master interrupt enable (ICR[1] or ICR[0]) are asserted.

[5] Delta DCD—The DCD input is sampled approximately every 6.8μs using the 32X, 4800 baud output from the BRG. After synchronizing with the sampling clock, at least two consecutive samples at the same level are required to establish the level. As a consequence, a change of state at the DCD input, lasting at least 17μs, will set this bit. The reset circuitry initializes the sampling circuits so that a change is not falsely indicated at power on time. The assertion of this bit causes an interrupt to be generated if IER[7] and the channel's master interrupt enable (ICR[1] or ICR[0]) are asserted.

[4] Delta CTS/LC—When not in loop mode, the CTS input is sampled approximately every 6.8μs using the 32X, 4800 baud output form the BRG. After synchronizing with the sampling clock, at least two consecutive samples at the same level are required to establish the level. As a consequence, a change of state at the CTS input, lasting at least 17μs, will set this bit. The reset circuitry initializes the sampling circuits so that a change is not falsely indicated at power on time. The assertion of this bit causes an interrupt to be generated if IER[7] and the channel's master interrupt enable (ICR[1] or ICR[0]) are asserted.

In SDLC loop mode, this bit is set upon transitions of the LC output. LC is asserted in response to the 'go on-loop' command when the receiver detects a zero followed by seven ones, and negated in response to the 'go off-loop' command when the receiver detects a sequence of eight ones.

[3:2] State of DCD and CTS—ICTSRx[3] reflects the state of the DCDxN input pin, while ICTSRx[2] reflects the state of CTSxN. When the bits are 0, the inputs are High, when they are 1, the pins are Low.

[1:0] Current State of GPI2 and GPI1—These fields provide the current state of the channels general purpose input pins. The bits valve are latched at the beginning of the read cycle.

Interrupt Vector Register (IVR) and Modified Vector Register (IVRM)

[7:0] Register Content—If ICR[2] = 0, the content of IVR register is output on the data bus when the DUSCC has issued an interrupt request and the responding interrupt acknowledge (IACKN) is received. The value in the IVR is initialized to H'0F' on master reset. If 'vector includes status' is specified by ICR[2] = 1, bit [2:0) or [4:2] (depending on ICR[3]), of the vector are modified as shown in Table 8 to indicate the highest priority interrupt currently active. The priority is programmable through the ICR. This modified vector is stored in the IVRM. When ICR[2] = 1, the content of the IVRM is output on to the data bus on the interrupt acknowledge. The vector is not modified, regardless of the value of ICR[2], if the CPU has not written an initial vector into this register.

Either the modified or unmodified vector can also be read by the CPU via a normal bus read cycle (see Table 1). The vector value is locked at the beginning of the IACK or read cycle until the cycle is completed. If no interrupt is pending, an H'FF' is output when reading the IVRM or the IVR.

Interrupt Control Register (ICR)

[7:6] Channel A/B Interrupt Priority—Selects the relative priority between Channels A and B. The state of this bit determines the value of the interrupt vector (see Interrupt Vector Register). The priority within each channel, from highest to lowest, is as follows:

0 Receiver ready.

1 Transmitter ready

2 Rx/Tx status.

3 External or C/T status.

00 Channel A has the highest priority. The DUSCC interrupt priorities from highest to lowest are as follows: A(0), A(1), A(2), A(3), B(0), B(1), B(2), B(3).

01 Channel B has the highest priority. the DUSCC interrupt priorities from highest to lowest are as follows: B(0), B(1), B(2), B(3), A(0), A(1), A(2), A(3).

10 Priorities are interleaved between channels, but Channel A has the highest priority between events of equal channel priority. The DUSCC interrupt priorities from highest to lowest are as follows: A(0), B(0), A(1), B(1), A(2), B(2), A(3), B(3)

11 Priorities are interleaved between channels, but Channel B has the highest priority between events of equal channel priority. The DUSCC interrupt priorities from highest to lowest are as follows: B(0), A(0), B(1), A(1), B(2), A(2), B(3), A(3).

Table 8. Interrupt Status Encoding

IVRM [2:0]/ [4:2]	HIGHEST PRIORITY INTERRUPT CONDITION
000	Channel A receiver ready
001	Channel A transmitter ready
010	Channel A Rx/Tx status
011	Channel A external or C/T status
100	Channel B receiver ready
101	Channel B transmitter ready
110	Channel B Rx/Tx status
111	Channel B external or C/T status

[5:4] Vector Mode—The value of this field determines the response of the DUSCC when the interrupt acknowledge (IACKN) is received from the CPU.

00 or 01 or 10 Vectored mode. Upon interrupt acknowledge, the DUSCC locks its current interrupt status until the end of the acknowledge cycle. If it has an active interrupt pending, it responds with the appropriate vector and then asserts DTACKN. If it does not have

an interrupt, it propagates the acknowledge through its X2/IDCN output if this function is programmed in PCRA[7]. Otherwise, the IACKN is ignored. Locking the interrupt status at the leading edge of IACKN prevents a device at High position in the interrupt daisy chain from responding to an IACK issued for a lower priority device while the acknowledge is being propagated to that device.

11 Non-vectored mode. The DUSCC ignores an IACK if one is received; the interrupt vector is not placed on the data bus. The internal interrupt status is locked when a read of the IVR or IVRM is performed. Except for the absence of the vector on the bus, the DUSCC performs as it does in vectored mode—the vector is prioritized and modified if programmed.

[3] Vector Bits to Modify—Selects which bits of the vector stored in the IVR are to be modified to indicate the highest priority interrupt pending in the DUSCC. See Interrupt Vector Register.

0 Modify bits 2:0 of the vector.

1 Modify bits 4:2 of the vector.

[2] Vector Includes Status—Selects whether the modified (includes status) (IVRM) or unmodified vector (IVR) is output in response to an interrupt acknowledge (see Interrupt Vector Register).

0 Unmodified vector.

1 Modified vector.

[1] Channel A Master Interrupt Enable—

0 Channel A interrupts are disabled.

1 Channel A interrupts are enabled.

[0] Channel B Master Interrupt Enable—

0 Channel B interrupts are disabled.

1 Channel B interrupts are enabled.

General Status Register (GSR)

This register provides a 'quick look' at the overall status of both channels of the DUSCC. A write to this register with 1s at the corresponding bit positions causes TxRDY (bits 5 and 1) and/or RxRDY (bits 4 and 0) to be reset. The other status bits can be reset only by resetting the individual status bits that they point to.

[7] Channel B External or Counter/Timer Status—This bit indicates that one of the following status bits is asserted. ICTSRB[6:4].

[6] Channel B Receiver or Transmitter Status—This bit indicates that one of the following status bits is asserted: RSRB[7:)], TRSRB[7:3].

[5] Channel B Transmitter Ready—The assertion of this bit indicates that one or more characters may be loaded into the Channel B transmitter FIFO to be serialized by the transmit shift register. See description of OMR[4]. This bit can be asserted only when the transmitter is enabled. Disabling or resetting the transmitter negates TxRDY.

[4] Channel B Receiver Ready—The assertion of this bit indicates that one or more characters are available in the Channel B receiver FIFO to be read by the CPU. See description of OMR[3]. RxRDY is initially reset (negated) by a chip reset or when a 'reset Channel B receiver' command is invoked.

[3] Channel A External or Counter/Timer Status—This bit indicates that one of the following status bits is asserted: ICTSRA[6:4].

[2] Channel A Receiver or Transmitter Status—This bit indicates that one of the following status bits is asserted: RSRA[7:0], TRSRA[7:3].

[1] Channel A Transmitter Ready—The assertion of this bit indicates that one or more characters may be loaded into the Channel A transmitter FIFO to be serialized by the transmit shift register. See description of OMR[4]. This bit can be asserted only when the transmitter is enabled. Disabling or resetting the transmitter negates TxRDY.

[0] Channel A Receiver Ready—The assertion of this bit indicates that one or more characters are available in the Channel A receiver FIFO to be read by the CPU. See description of OMR[3]. RxRDY is initially reset (negated) by a chip reset or when a 'reset Channel A receiver' command is invoked.

Channel Command Register (CCRA, CCRB)—Commands to the DUSCC are entered through the channel command register. The format of that register is shown in Table 9. A read of this register returns the last invoked command (with bits 4 and 5 set to 1).

Transmitter Commands

0000 Reset transmitter. Causes the transmitter to cease operation immediately. The transmit FIFO is cleared and the TxD output goes into the marking state. Also clears the transmitter status bits (TRSR[7:4]) and resets the TxRDY status bit (GSR[1] or GSR[5] for Channels A and B, respectively). The counter/timer and other registers are not affected.

0001 Resest transmit CRC. This command is appended to and FIFOed along with the next character loaded into the transmit FIFO. It causes the transmitter CRC generator to be reset to its initial state prior to beginning transmission of the appended character.

0010 Enable transmitter. Enables transmitter operation, conditioned by the state of the CTS ENABLE Tx bit, TPR[2]. Has no effect if invoked when the transmitter has previously been enabled.

0011 Disable transmitter. Terminates transmitter operation and places the TxD output in the marking state at the next occurrence of a transmit FIFO empty condition. All characters currently in the FIFO, or any loaded subsequently prior to attaining an empty condition, will be transmitted.

0100 Transmit start of message. Used in COP and BOP modes to initiate transmission of a frame after the transmitter is first enabled, prior to sending the contents of the FIFO. Can also be used to precisely control the number of SYN/FLAGs at the beginning of transmission or in between frames.

When the transmitter is first enabled, transmission will not begin until this command (or the transmit SOM with PAD command, see below) is issued. The command causes the SYN (COP) or FLAG (BOP) pattern to be transmitted. SEND SOM ACK (TRSR[4]) is set when transmission of the SYN/FLAG begins. The CPU may then reinvoke the command if multiple SYN/FLAGs are to be transmitted. Transmission of the FIFO characters begin when the command is no longer invoked. If the FIFO is empty, SYN/FLAGs continue to be transmitted until a character is loaded into the FIFO, but the status bit (TRSR[4]) is not set. Insertion of SYN/FLAGs between frames can be accomplished by invoking this command after the frame complete status bit (TRSR[5]) has been asserted in response to transmission of the end-of message sequence.

0101 Transmit start of message with opening PAD. Used in COP and BOP modes after the transmitter is first enabled to send a bit pattern for DPLL synchronization prior to transmitting the opening SYN (COP) or FLAG

(BOP). the SYN/FLAG is sent at the next occurrence of a transmit FIFO empty condition. All characters currently in the FIFO, or any loaded subsequently prior to attaining an empty condition, will be transmitted. While the PAD characters are transmitted, the character length is set to 8 bits, (regardless of the programmed length), and parity generation (COP), zero insertion (BOP) and LRC/CRC accumulation are disabled. SEND SOM ACK (TRSR[4]) is set when transmission of the SYN/FLAG begins. The CPU may then invoke the transmit SOM command if multiple SYN/FLAGs are to be transmitted.

The TSOM/TSOMP commands, described above, are sampled by the controller in alternate bit times of the transmitter clock. As a consequence, the first bit time of a COP/BOP frame will be transmitted on the TxD pin, after a maximum of three bit times, after the command is issued. (The additional 1-bit delay in the data path is due to the data encoding logic.)

0110 Transmit end-of-message. This command is appended to the next character loaded into the transmit FIFO. It causes the transmitter to send the end-of message sequence (selected FCS in COP modes, FCS-FLAG in BOP modes) after the appended character is transmitted. Frame complete (TRSR[5]) is set when transmission of the FCS begins. This command is also asserted automatically if the TEOM on zero count or one control bit (TPR[4]) is asserted, and the counter/timer is programmed to count transmitted characters when the character which causes the count to go to zero is loaded into the transmit FIFO. TEOM is not recognized if the transmitter FIFO is full.

0111 Transmit Abort BOP/Transmit Break ASYNC. In BOP modes, causes an abort (eight ones) to be transmitted after transmission of the character currently in the shift register is completed. The transmitter then sends MARKs or FLAGs depending on the state of underrun control (TPR[7:6]). Send SOM/abort ack (TRSR[4]) is set when the transmission of the abort begins. If the command is reasserted before transmission of the previous ABORT is completed, the process will be repeated. This can be used to send the idle sequence. The 'transmit SOM' command must be used to initiate transmission of a new message. In either mode, invoking this command causes the transmit FIFO to be flushed (characters are not transmitted).

In ASYNC mode, causes a break (space) to be transmitted after transmission of the character currently in the shift register is completed. Send break ack (TRSR[4]) is set when the transmission of the break begins. The transmitter keeps track of character times. If the command is reasserted, send break ack will be set again at the beginning of the next character time. The user can use this mechanism to control the length of the break in character time multiples. Transmission of the break is terminated by issuing a 'reset Tx' or 'disable Tx' command.

1000 Transmit DLE. Used in COP modes only. This command is appended to and FIFOed with the next character loaded into the transmitter FIFO. It causes the transmitter to send a DLE, (EBCDIC H'10', ASCII H'10') prior to transmitting the appended character. If the transmitter is operating in BISYNC transparent mode, the transmitter control logic automatically causes a second DLE to be transmitted whenever a DLE is detected at the top of the FIFO. In this case, the TDLE command should not be invoked. An extra (third) DLE, however, will not be sent if the transmit DLE command is invoked.

1001 Go active on poll. Used in BOP loop mode only. Causes the transmitter, if it is enabled, to begin sending when an EOP sequence consisting of a zero followed by seven ones is detected. The last one of the EOP is changed to zero, making it another FLAG, and then the transmitter operates as described in the detailed operation section. The loop sending status bit (TRSR[6]) is asserted concurrent with the beginning of transmission.

1010 Reset go active on poll. Clears the stored 'go active on poll' command.

1011 Go on-loop. Used in BOP loop mode to control the assertion of the LCN output. This output provides the means of controlling external loop interface hardware to go on-loop and off-loop. When the command is asserted, the DUSCC will look for the receipt of a zero followed by seven ones, at which time it will assert the LCN output and set the delta DCD/LC status bit (ICTSR[4]). This allows the DUSCC to break into the loop without affecting loop operation. This command must be used to initiate loop mode operation.

1100 Go off-loop. Used in BOP loop mode to control the negation of the LCN output. This output provides the means of controlling external loop interface hardware to go on-loop and off-loop. When the command is asserted, the DUSCc will look for the receipt of eight contiguous ones, at which time it will negate the LCN output and set the delta DCD/LC status bit (ICTSR[4]). This allows the DUSCC to get off the loop operation. This command is normally used to terminate loop mode operation.

1101 Exclude from CRC. This command is appended to and FIFOed along with the next character loaded into the transmit FIFO. It causes the transmitter CRC generator to be disabled while the appended character is being transmitted. Thus, that character is not included in the CRC accumulation.

Receiver Commands

0000 Reset Receiver. Causes the receiver to cease operation, clears the receiver FIFO, clears the data path, and clears the receiver status (RSR[7:0], TRSR[3:0], and either GSR[0] or GSR[4] for Channels A and B, respectively). The counter/timer and other registers are not affected.

0001 Reserved.

0010 Enable receiver. Causes receiver operation to begin, conditioned by the state of the DCD ENABLED Rx bit, RPR[2]. Receiver goes into START, SYN, or FLAG search mode depending on channel protocol mode. Has no effect if invoked when the receiver has previously been enabled.

0011 Disable receiver. Terminates operation of the receiver. Any character currently being assembled will be lost. Does not affect FIFO or any status. While in COP mode, disabling the receiver does not clear the data path; in all other cases, it does.

Counter/Timer Commands

0000 Start. Starts the counter/timer and prescaler.

0001 Stop. Stops the counter/timer and prescaler. Since the command may be asynchronous with the selected clock source, the counter/timer and/or prescaler may count one or more additional cycles before stopping.

0010 Preset to FFFF. Presets the counter timer to H'FFFF' and the prescaler to its initial value. This command causes the C/T output to go Low.

0011 Preset from CTPRH/CTPRL. Transfers the current value in the counter/timer preset registers to the counter/timer and presets the prescaler to its initial value. This command causes the C/T output to go Low.

Digital Phase-Locked Loop Commands

0000 Enter Search Mode. This command causes the DPLL counter to be set to the value 15 and the clock output will be forced Low. The counter will be disabled until a transition on the data line is detected, at which point it will start incrementing. After the counter reaches a count of 31, it will reset to zero and cause the clock output to go from Low to High. The DPLL will then continue normal operation. This allows the DPLL to be locked onto the data without pre-frame transitions. This command should not be used if the DPLL is programmed to supply the clock for the transmitter is active.

0001 Disable DPLL. Disables operation of the DPLL.

0010 Set FM Mode. Sets the DPLL to the FM mode of operation, used when FM0, FM1, or Manchester (NMRZ) is selected by CMR1[7:6].

0011 Set NRZI Mode. Sets the DPLL to the NRZI mode of operation, used when NRZ or NRZI is selected by CMR1[7:6].

0100 Reserved for test.

0101 Reserved for test.

Table 9. Command Register Bit Format

CHANNEL COMMAND REGISTER

	BIT 7 / BIT 6	BIT 5	BIT 4	BIT 3 – BIT 0
(CCRA, CCRB)				**Transmitter Command**
	00 = Transmitter CMD	don't care	don't care	0000 — reset Tx 0001 — reset TxCRC* 0010 — enable Tx 0011 — disable Tx 0100 — transmit SOM (TSOM) 0101 — transmit SOM with PAD (TSOMP) 0110 — transmit EOM (TEOM)* 0111 — transmit ABORT/BREAK (TABRK) 1000 — transmit DLE (TDLE)* 1001 — go active on poll 1010 — reset go active on poll 1011 — go on-loop 1100 — go off-loop 1101 — exclude form CRC*
				Receiver Command
	01 = Receiver CMD	don't care	don't care	0000 — reset Rx 0001 — reserved 0010 — enable Rx 0011 — disable Rx
				Counter/Timer Command
	10 = C/T CMD	don't care	don't care	0000 — start 0001 — stop 0010 — preset to FFFF 0011 — preset from CTPRH/CTPRL
				DPLL Command
	11 = DPLL CMD	don't care	don't care	0000 — enter search mode 0001 — disable DPLL 0010 — set FM mode 0011 — set NRZI mode 0100 — reserved for test 0101 — reserved for test

DETAILED OPERATION

Interrupt Control

A single interrupt output (IRQN) is provided which is activated upon the occurrence of any of the following conditions:

Channel A external or C/T special condition

Channel B external or C/T special condition

Channel A Rx/Tx error or special condition

Channel B Rx/Tx error or special condition

Channel A TxRDY

Channel B TxRDY

Channel A RxRDY

Channel B RxRDY

Each of the above conditions occupies a bit in the General Status Register (GSR). If ICR[2] is set, the eight conditions are encoded into three bits which are inserted into bits [2:0] or [4:2] of the interrupt vector register. This forms the content of the IVRM during an interrupt acknowledge cycle. Unmodified and modified vectors can read directly through specified registers. Two of the conditions are the inclusive OR of several other maskable conditions:

- External or C/T special condition: Delta DCD, Delta CTS or C/T zero count (ICTSR[6:4]).
- Rx/Tx error or special condition: any condition in the Receiver Status Register (RSR[7:0]) or a transmitter or DPLL condition in the Transmitter and Receiver Status Register (TRSR[7:3]).

The TxRDY and RxRDY conditions are defined by OMR[4] and OMR[3], respectively. Also associated with the interrupt system are the Interrupt Enable Register (IER), one bit in the Counter/Timer Control Register (CTCR), and the Interrupt Control Register (ICR).

The IER is programmed to enable specified conditions or groups of conditions to cause an interrupt by asserting the corresponding bit. A negated bit prevents an interrupt from occurring when the condition is active and hence masks the interrupt. In addition to the IER, CTCR[7] could be programmed to enable or disable an interrupt upon the C/T zero count condition. The interrupt priorities within a channel are fixed. Priority between channels is controlled by ICR[7:6]. Refer to Table 8 and ICR[7:6].

The ICR contains the master interrupt enables for each channel (ICR[1] and ICR[0]) which must be set if the corresponding channel is to cause an interrupt. The CPU vector mode is specified by ICR[5:4] which selects either vectored or non-vectored operation. If vectored mode is selected, the content of the IVR or IVRM is placed on the data bus when IACK is activated. If ICR[2] is set, the content of IVRM is output which contains the content of IVR and the encoded status of the interrupting condition.

Upon receiving an interrupt acknowledge, the DUSCC locks its current interrupt status until the end of the acknowledge cycle. If it has an active interrupt pending, it responds with the appropriate vector and then asserts DTACKN. If it does not have an interrupt, it propagates the acknowledge through its X2/IDCN output if this function is programmed in PCRA[7]; otherwise, the IACKN is ignored. Locking the interrupt status at the leading edge of IACKN prevents a device at a High position in the interrupt daisy chain from responding to an IACK issued for a lower priority device while the acknowledge is being propagated to that device.

DMA Control

The DMA control section provides the interface to allow the DUSCC to operate with an external DMA controller. One of four modes of DMA can be programmed for each channel independently via CMR2[5:3]:

- Half-duplex single address. In this mode, a single pin provides both DMA read and write requests. Acknowledgement of the requests is via a single DMA acknowledge pin. The data transfer is accomplished in a single bus cycle—the DMA controller places the memory address of the source or destination of the data on the address bus and then issues the acknowledge signal, which causes the DUSCC to either write the data into its transmit FIFO (write request) or to output the contents of the top of the receive FIFO (read request). The cycle is completed when the DTCN input is asserted by the DMA controller. This mode can be used when channel operation is half-duplex (e.g., BISYNC) and allows a single DMA channel to service the receiver and transmitter. The receiver and transmitter should not be enabled at the same time when half-duplex mode is programmed.
- Half-duplex dual address. In this mode, a single pin provides both DMA read and write requests. Acknowledgement of the requests is via normal bus read and write cycles. The data transfer requires two bus cycles—the DMA controller acquires the data from the source (memory for a Tx DMA or DUSCC for a Rx DMA) on the first cycle and deposits it at the destination (DUSCC for a Tx DMA or memory for a Rx DMA) on the second bus cycle. This mode is used when channel operation is half-duplex (e.g., BISYNC) and allows a single DMA channel to service the receiver and transmitter.
- Full-duplex single address. This mode is similar to half-duplex single address mode but provides separate request and acknowledge pins for the receiver and transmitter.
- Full-duplex dual address. This mode is similar to half-duplex dual address mode but provides duplex dual address mode and provides separate request pins for the receiver and transmitter

Figures 4 through 7 describe operation of the DUSCC in the various DMA environments. Table 10 summarizes pins used for the DMA request and acknowledge function for the transmitter and receiver for the different DMA modes.

The DMA request signals are functionally identical to the TxRDY and RxRDY status signals for each serial channel except that the DMA request signals are negated on the leading edge of the acknowledge signal when the subsequent transfer causes the FIFO to become full (transmitter request) or empty (receiver request).

In non-DMA operation TxRDY and RxRDY signals are automatically negated only after the transfer is completed. The DMA read request can be programmed through OMR[3] be asserted either when any character is in the receive FIFO or only when the receive FIFO is full. Likewise, the DMA write request can be programmed through OMR[4] to be asserted either when the transmit FIFO is not full or only when the transmit FIFO is empty (The transmitter must be enabled for a DMA request to be asserted). The request signals are automatically negated when the respective data transfer cycle is completed and the FIFO becomes full (transmitter request) or empty (receiver request). If a transfer is completed and the FIFO is not left full (transmitter) or empty (receiver), the request stays Low. The request may be negated by the CPU with a status reset write cycle. (Although DONEN terminates all DMA transfers, it has no effect on the requests. The requests are a function of the FIFO status, but they can be negated by writing into the GSR.) When the serial channel is not operating in DMA mode, the request and acknowledge pins for the channel can be programmed for other functions (see Pin Descriptions).

DMA DONEN Operation

As an input, DONEN is asserted by the DMA controller concurrent with the corresponding DMA acknowledge to indicate to the DUSCC that the character being transferred into the TxFIFO is the last character of the transmission frame. In synchronous modes, the DUSCC can be programmed through TPR[4] to automatically transmit the frame termination sequence (e.g., FCS-FLAG in BOP mode) upon receipt of this signal.

As an output, DONEN is asserted by the DUSCC under the following conditions:

a. In response to the DMA acknowledge for a receiver DMA request if the FIFOed RECEIVED EOM status bit (RSR[7]) is set for the character being transferred.

b. In response to the DMA acknowledge for a receiver DMA request if the counter/timer has been programmed to count transmitted characters and the terminal count has occurred.

Block Transfers Using DTACK

The DTACKN line may be used to synchronize data transfers to and from the DUSCC utilizing a 'wait' state. Either the receive or the transmitter or both may be programmed for this mode of operation, independently for each channel, via CMR2[5:3].

In this mode, if the CPU attempts a write to the transmit FIFO and an empty FIFO position is not available, the DTACKN line will remain negated until a position empties. The data will then be written into the FIFO and DTACKN will be asserted to signify that the transfer is complete.

Similarly, a read of an empty receive FIFO will be held off until data is available to be transferred. Potentially, this mode can cause the microcomputer system to hang up if, for example, a read request was made and no further data was available.

Table 10. DMA REQ and ACK Pins for Operational Modes

FUNCTION	HALF DUPLEX SINGLE ADDR DMA	HALF DUPLEX DUAL ADDR DMA	FULL DUPLEX SINGLE ADDR DMA	FULL DUPLEX DUAL ADDR DMA
RCVR REQ	RTxDRQN	RTxDRQN	RTxDRQN	RTxDRQN
TRAN REQ	Same as RCVR REQ	Same as RCVR REQ	TxDRQN	TxDRQN
RCVR ACK	RTxDAKN	Normal read RCVR FIFO	RTxDAKN	Normal read RCVR FIFO
TRAN ACK	Same as RCVR ACK	Normal write TRAN FIFO	TxDAKN	Normal write TRAN FIFO

Timing Circuits

The timing block for each channel consists of a crystal oscillator, a Bit Rate Generator (BRG), a Digital Phase-Locked Loop (DPLL) and a 16-bit Counter/Timer (C/T) (see Figure 8).

Crystal Oscillator

The crystal oscillator operates directly from a crystal (normally 14.7456MHz if the internal BRG is to be used) connected across the X1/CLK and X2/IDCN pins with a minimum of external components. If an external clock of the appropriate frequency is available, it may be connected to the X1/CLK pin. This signal is divided by two to provide the internal system clock.

Bit Rate Generator

The BRG operates from the oscillator or external clock and is capable of generating 16-bit rates. These are available to the receiver, transmitter, DPLL, and C/T. The BRG output is at 32X the base bit rate. Since all sixteen rates are generated simultaneously, each receiver and transmitter may select its bit rate independently. The transmitter and receiver timing registers include a 4-bit field for this purpose (TTR[3:0], RTR[3:0])

Digital Phase-Locked Loop

Each channel of the DUSCC includes a DPLL used in synchronous modes to recover clock information from a received data stream. The DPLL is driven by a clock at nominally 32 times the data rate. This clock can be programmed, via RTR[7:4], to be supplied from an external input, from the receiver BRG, from the C/T, or directly from the crystal oscillator.

The DPLL uses this clock, along with the data stream to construct a data clock which may then be used as the DUSCC receive clock, transmit clock, or both. The output of the DPLL is a square wave at 1X the data rate. The derived clock can also be programmed to be output on a DUSCC pin; only the DPLL receiver output clock is available at the TRxC pin. Four commands are associated with DPLL operation: Enter search mode, set FM mode, set NRZI mode, and disable DPLL. The commands are described in the Command Register Description. Waveforms associated with the DPLL are illustrated in Figure 9.

DPLL NRZI Mode Operation—This mode is used with NRZ and NRZI data encoding. With this type of encoding, the transitions of the data stream occur at the beginning of the bit cell. The DPLL has a six-bit counter which is incremented by a 32X clock. The first edge detected during search mode sets the counter to 16 and begins operation. The DPLL output clock then rises at a count of 0 and falls at 16. Data is sampled on the rising edge of the clock. When a transition in the data stream is detected, the count length is adjusted by one or two counts, depending on the counter value when the transition occurs (see Table 11). A transition detection at the roll-over point (third column in Figure 11) is treated as a transition occurring at zero count.

The count length adjustments cause the rising edge of the DPLL output block to converge to the nominal center of the bit cell. In the worst case, which occurs when a DPLL pulse is coincident with the data edge, the DPLL converges after 12 data transitions.

For NRZ encoded data, a stream of alternating ones and zeros should be used as a synchronizing pattern. For NRZI encoded data, a stream of zeros should be used.

Table 11. NRZI Mode Count Length

COUNT WHEN TRANSITION DETECTED	COUNT LENGTH ADJUST-MENT	COUNTER RESET AFTER COUNT REACHES
0—7	-2	29
8—15	-1	30
16—23	+1	32
24—30	+2	33
None detected	0	31

DPLL FM Mode Operation—FM operation is used with FM0, FM1, and Manchester data encoding. With this type of encoding, transitions in the data stream always occur at the beginning of the bit cell for FM0 and FM1, or at the center of the bit cell for Manchester. The DPLL 6-bit counter is incremented by a 32X clock. The first edge detected during search mode sets the counter to 16 and begins operation. The DPLL receiver clock then rises on a count of 8 and falls on 24. (The DPLL transmitter clock output falls on a count of 16. It rises on a count of 0 if a transition has been detected between count of 16 and 23. For other cases, it rises 1/2 count of the 32X input clock sooner.) This provides a 1X clock with edges positioned at the nominal centers of the two halves of the bit cell. The transition detection circuit is enabled between counts of 8 and 23, inclusive. When a transition is detected, the count length is adjusted by one, depending on when the transition occurs (see Table 12).

If a transition is not detected for two consecutive data bits, the DPLL is forced into search mode and the DPLL error status bit

(TRSR[3]) is asserted. This feature is disabled when the DPLL output is used only as the transmitter clock.

To prevent the DPLL from locking on the wrong edges of the data stream, an opening PAD sequence should be transmitted. For FM0, a stream of at least 16 ones should be sent initially. For FM1, a minimum stream of 16 zeros should be sent and for Manchester encoding the initial data stream should consist of alternating ones and zeros.

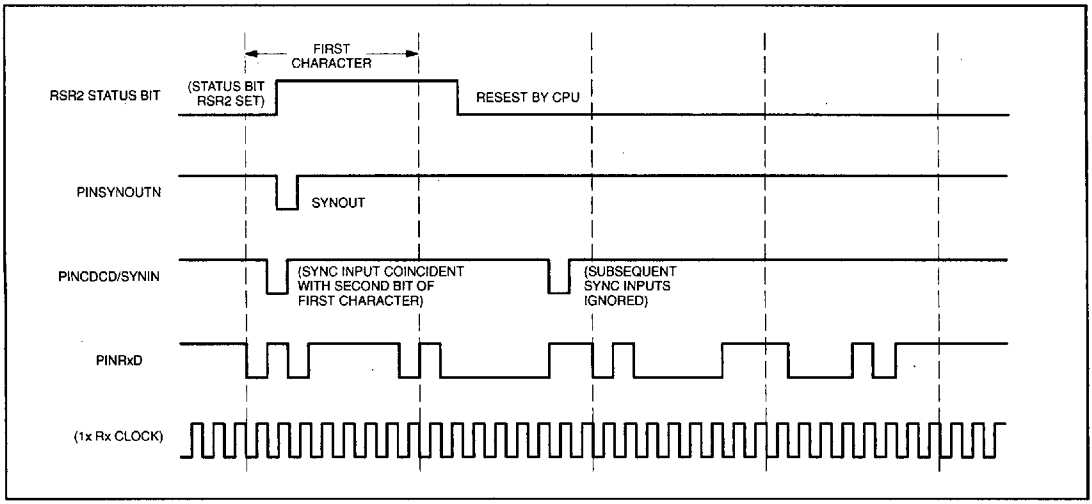


Figure 2. External Sync Mode

Table 12. FM Mode Count Length

COUNT WHEN TRANSITION DETECTED	COUNT LENGTH ADJUST-MENT	COUNTER RESET AFTER COUNT REACHES
8—15	-1	30
16—23	+1	32
24—7	Disabled	
None detected	0	31

Counter/Timer

Each channel of the DUSCC contains a Counter/Timer (C/T) consisting of a 16-bit down counter, a 16-bit preset register, and associated control circuits. Operation of the counter/timer is programmed via the Counter/Timer Control Register (CTCR). There are also four commands associated with C/T operation, as described in the Command Description section.

The C/T clock source, clock prescaling, and operating mode are programmed via CTCR[2:0], CTCR[4:3], and CTCR[6], respectively. The preset register is loaded with minimum of 2 by the CPU and its contents can be transferred into the down counter by a command, or automatically upon reaching terminal count if CTCR[6] is negated. Commands are also available to stop and start the C/T and to preset it to an initial value of FFFF. Counting is triggered by the falling edge of the clocking input. The C/T zero count status bit, ICTSR[6], is set when the C/T reaches the terminal count of zero and ICTSR[7] indicates whether the counter is currently enabled or not.

An interrupt is generated upon reaching zero count if CTCR[7] and the channel's master interrupt enable are asserted. The output of the C/T can be programmed to be output on the channel's RTxC or TRxC pin (via PCR[4:0]) as either a single pulse or a square wave, as programmed in CTCR[5].

The contents of the C/T can be read at any time by the CPU, but the C/T should normally be stopped before this is done. Several C/T operating modes can be selected by programming of the counter/timer control register. Typical applications include:

1. Programmable divider. The selected clock source, optionally prescaled, is divided by the contents of the preset register. The counter automatically reloads itself each time the terminal count is reached. In this mode, the C/T may be programmed to be used as the Rx or Tx bit rate generator, as the input to the DPLL, or it may be output on a pin as either a pulse or a square wave. The C/T interrupt should be disabled in this mode.
2. Periodic interrupt generator. This mode is similar to the programmable divider mode, except that the C/T interrupt is enabled, resulting in a periodic interrupt to the CPU.
3. Delay timer. The counter is preset from the preset register and a clock source, optionally prescaled, is selected. An interrupt is generated upon reaching terminal count. The C/T continues counting without reloading itself and its contents may be read by the CPU to allow additional delay past the zero count to be determined.
4. Character counter. The counter is preset to FFFF by command and the clock source becomes the internal signal used to control loading of the Rx or Tx characters. This operation is selected by CTCR[2:0]. The C/T counts characters loaded into the RxFIFO by the receiver or loaded into the transmit FIFO by the CPU, respectively. The current character count can be determined by the CPU by reading the contents of the C/T and taking its ones complement. Optionally, a preset number may be loaded into the counter and an interrupt generated when the count is exhausted. When counting Tx characters, the terminal count condition can be programmed through TPR[4] to cause an end of message sequence to be transmitted. When counting received characters, the FIFOed EOM status bit is asserted when the character which causes the count to go to zero is loaded into the receive FIFO. The channel's

'reset Tx' or 'reset Rx' commands have no effect on the operation of the C/T.

5. External event counter. The counter is preset to FFFFF by command and an external clock source is selected. The current count can be determined by the CPU by reading the contents of the C/T and taking its ones complement. Optionally, a preset number may be loaded into the counter and an interrupt generated when the count is exhausted.

6. Bit length measurement. The counter is preset to FFFF by command and the X1/CLK/4 clock input gated by RxD mode (optionally prescaled) is programmed. The C/T starts counting when RxD goes Low and stops counting when RxD goes High. At this time, ICTSR[6] is set and an interrupt (if enabled) is generated. The resulting count in the counter can be read by the CPU to determine the bit rate of the input data. Normally this function is used for asynchronous operation.

Communication Channels A and B

Each communication channel of the DUSCC is a full-duplex receiver and transmitter that supports ASYNC, COP, and BOP transmission formats. The bit rate clock for each receiver and transmitter can be selected independently to come from the bit rate generator, C/T, DPLL, or an external input (such as a modem generated clock).

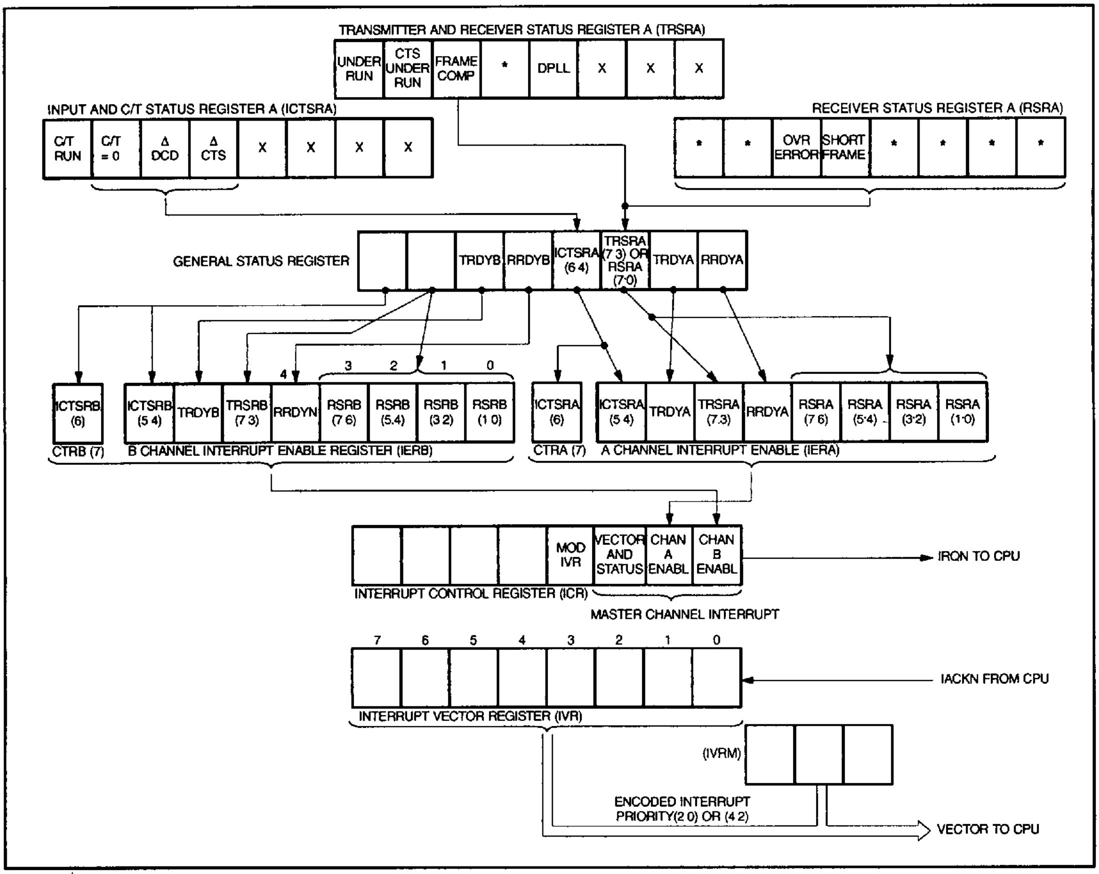


Figure 3. Interrupt Control and Status Register

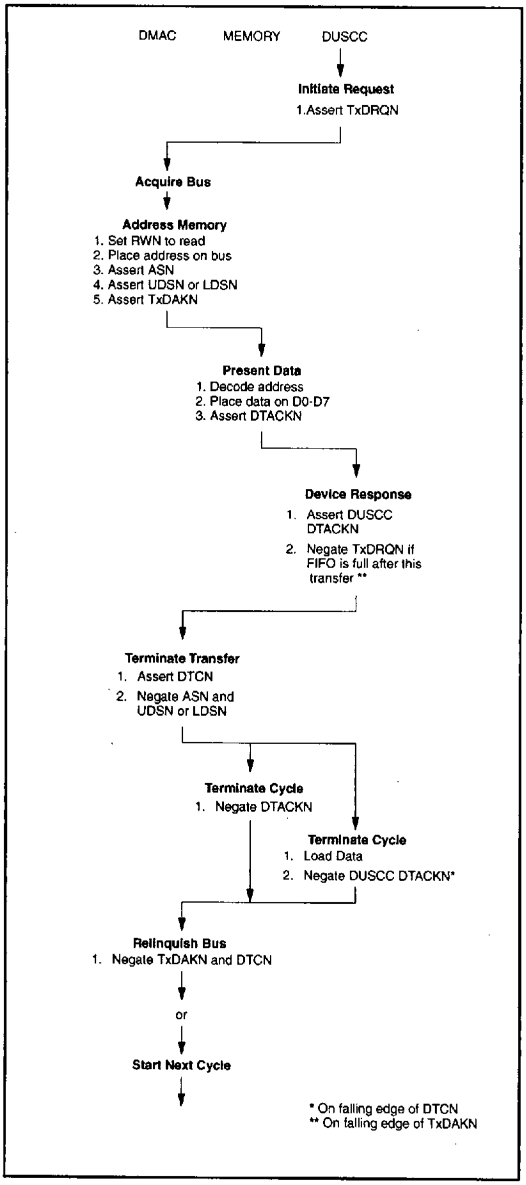


Figure 4. Transmitter DMA Request Operation— Single Address Mode

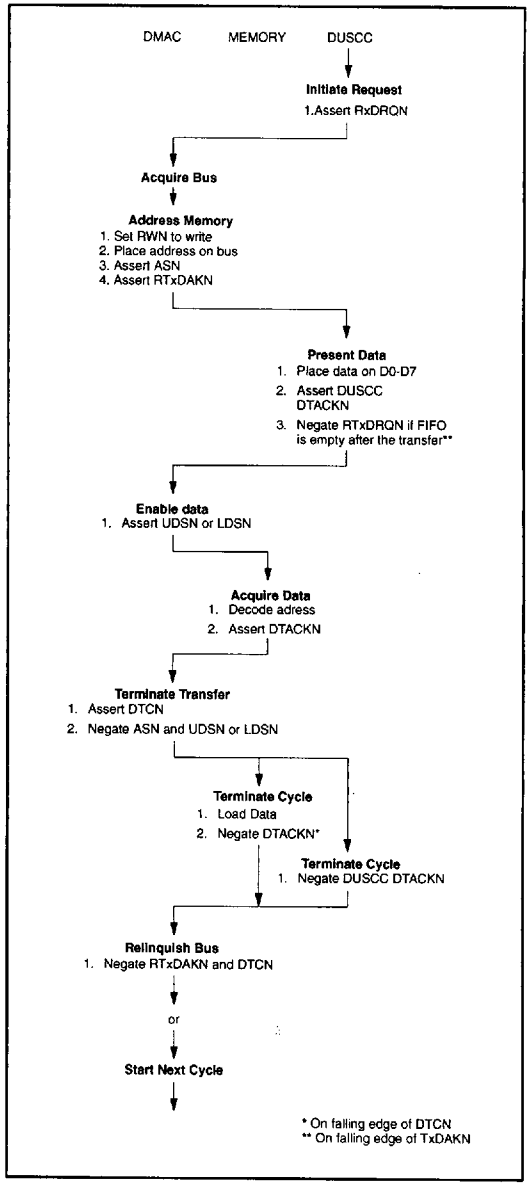


Figure 5. Receiver DMA Request Operation— Single Address Mode

7110826 0085092 656

Dual universal serial communications controller (DUSCC)

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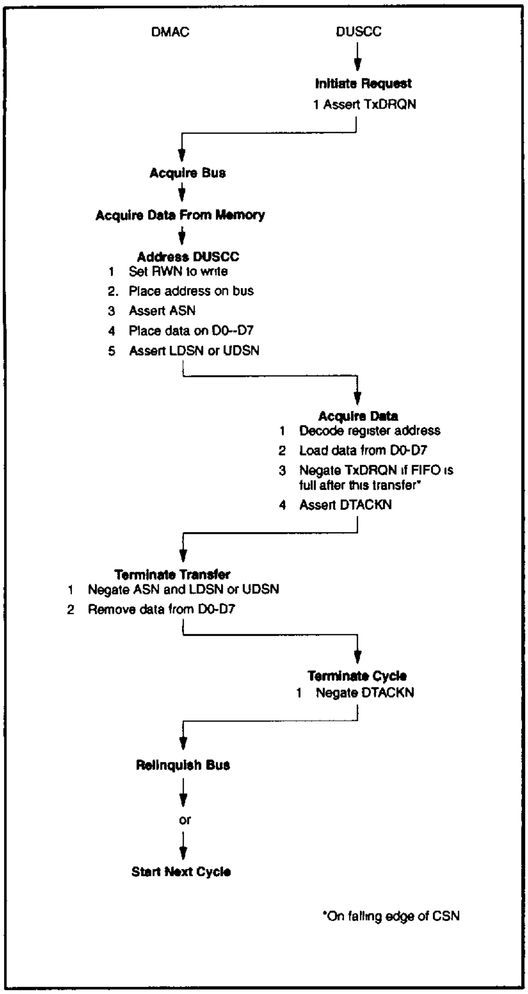

Figure 6. Transmitter DMA Request Operation—Dual Address Mode

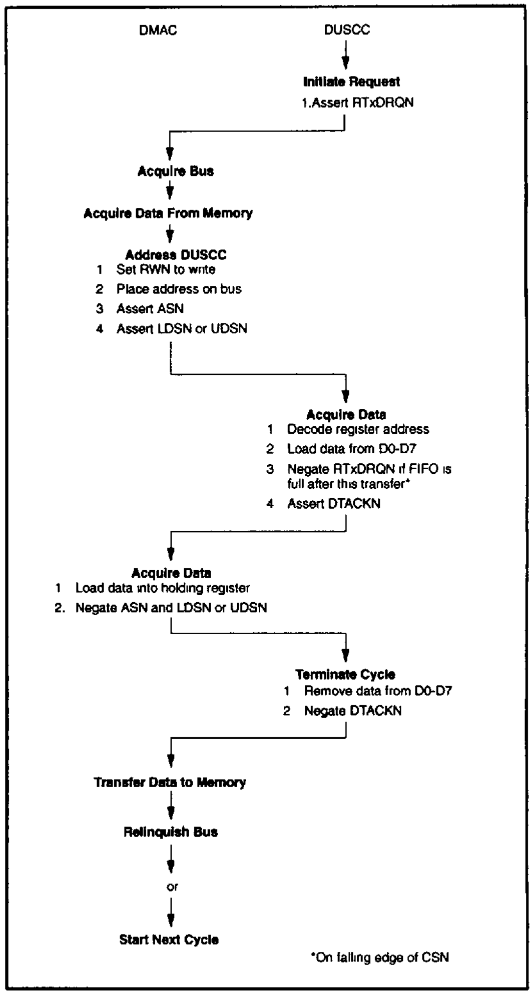

Figure 7. Receiver DMA Request Operation—Dual Address Mode

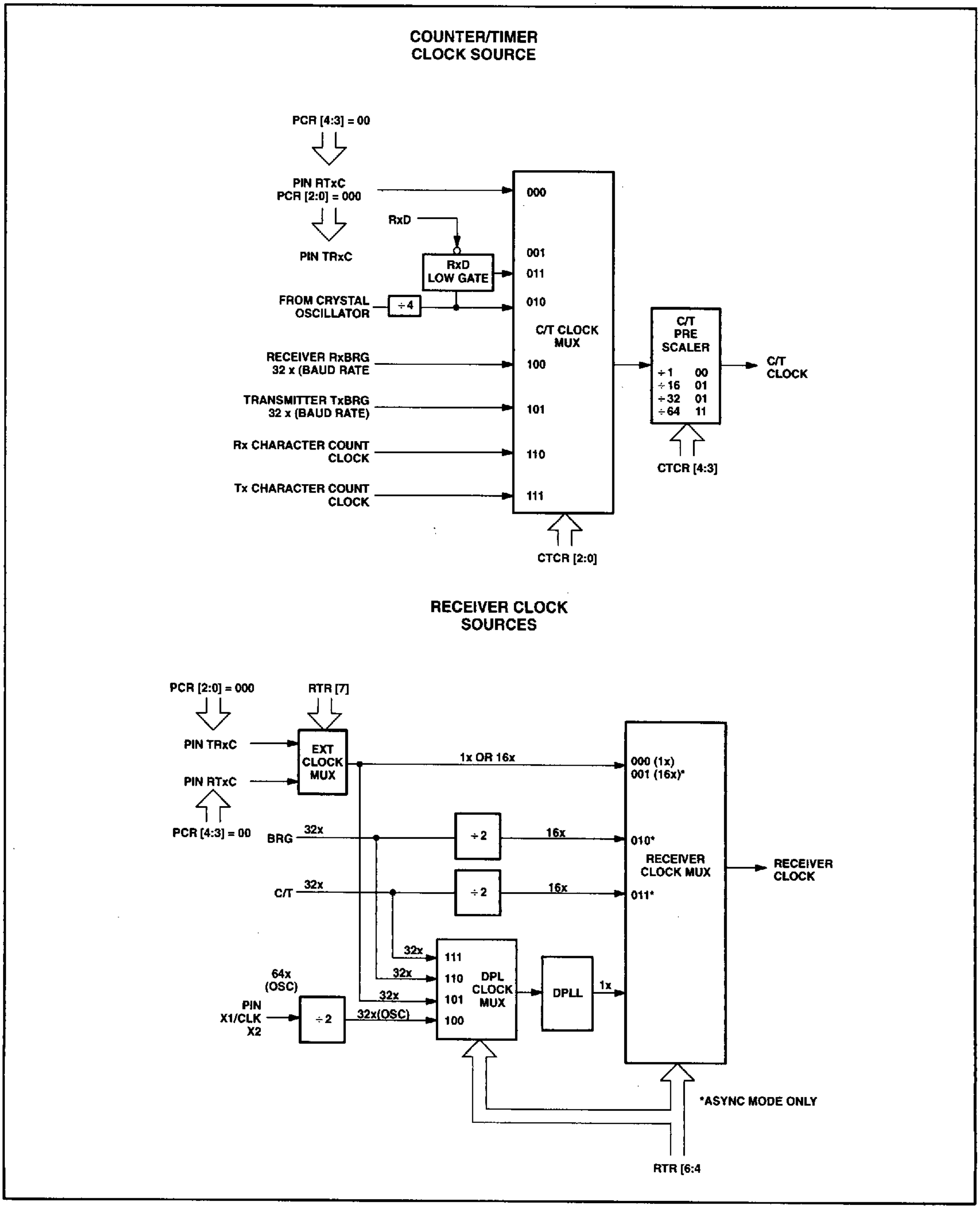

Figure 8. Timing Block

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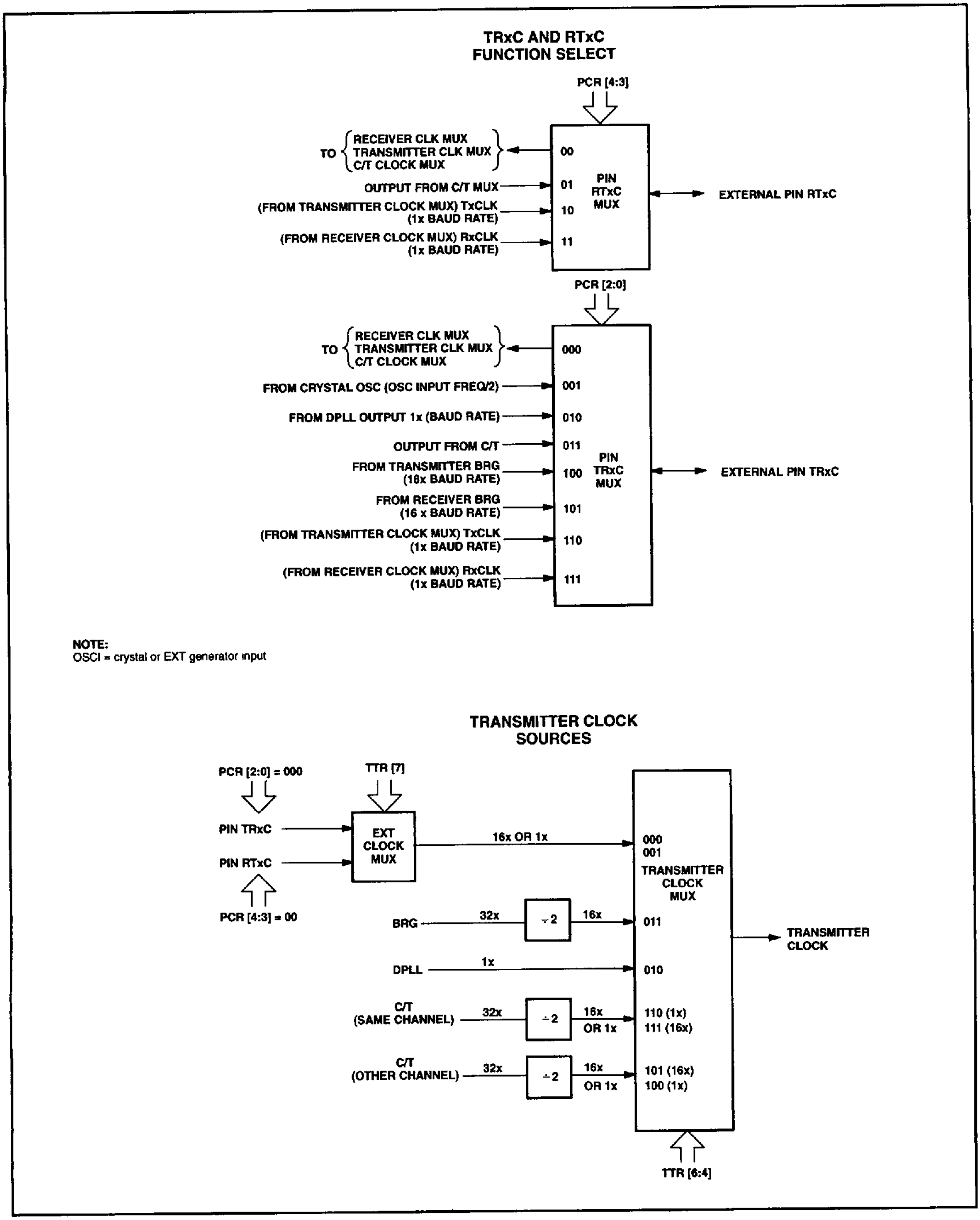


Figure 8. Timing Block (Continued)

TRANSMITTER

Transmitter TxFIFO and TxRDY

The transmitter accepts parallel data from the data bus and loads it into the TxFIFO, which consists of four 8-bit holding registers. This data is then moved to the Transmitter Shift Register (TxSR) which serializes the data according to the transmission format programmed. The TxSR is loaded from the TxFIFO, from special character logic, or from the CRC/LRC generator. The LSB is transmitted first, which requires right justification of characters by the CPU. TxRDY (GSR[5] or GSR[1]) and underrun (TRSR[7]) indicate the state of the TxFIFO. The TxFIFO may be addressed at any of four consecutive locations (see Table 1) to allow use of multiple byte work instructions. A write to any valid address always writes data to the next empty FIFO location.

TxRDY is set when the transmitter is enabled and there is an empty position in the TxFIFO (OMR[4] = 0) or when the TxFIFO becomes empty (OMR[4] = 1). The CPU may reset TxRDY through a status reset write cycle. If this is done, it will not be reasserted until a character is transferred to the TxST (OMR[4] = 0) or when the TxFIFO becomes empty again (OMR[4] = 1). The assertion of TxRDY, enabling of the IER [6] and the enabling of the channel master interrupt ICR[0] or [1] allow an interrupt to be generated.

If DMA operation is programmed, either RTxDRN (half-duplex) or TxDRQN (full-duplex) follows the state of TxRDY if the transmitter is enabled. These operations differ from normal ready in that the request signal is negated on the leading edge of the DMA acknowledge signal when the subsequent transfer causes the transmit FIFO to become full, while the TxRDY signal is negated only after the transfer is completed. Underrun status TRS[7] set indicates that one or more data character (not PAD characters) have been transmitted and the TxFIFO and TxSR are both empty.

In 'wait on Tx', a write to a full FIFO causes the write cycle to be extended until a FIFO position is available. DTACKN is asserted to acknowledge acceptance of the data. In non-wait modes, if an attempt is made to load data into a full TxFIFO, the TxFIFO data is preserved and the overrun data character(s) is lost. A normal DTACKN will be issued, and no indication of this occurrence is provided. The transmitter is enabled by the enable transmitter command. When the disable transmitter command is issued, the transmitter continues to operate until the TxFIFO becomes empty. The TxRDY does not become valid until the transmitter is enabled. Characters can be loaded into the FIFO while disabled. However, if the FIFO is full when the transmitter is enabled, TxRDY is not asserted.

TxRTS Control

If TxRTS CONTROL, TPR[3], is programmed, the channel's RTS output is negated 5-bit times after the last bit (stop bit in ASYNC mode) of the last character is transmitted. RTS is normally asserted and negated by writing to OMR[0]. Setting of TPR[3] causes RTS to be reset automatically (if the transmitter is not enabled) after all characters in the transmitter FIFO (if any) are transmitted and five bit times after the 'last character' is shifted out. This feature can be used to automatically terminate the transmission of a message as follows:

- Program auto-reset mode: TPR[3] = 1.
- Enable transmitter.
- Assert RTSN: OMR[0] = 1.
- Send message.
- Disable transmitter after the last character is loaded into the TxFIFO.
- The last character will be transmitted and OMR[0] will be reset five bit times after the last bit, causing RTSN to be negated. The TxD output will remain in the marking state until the transmitter is enabled again.

The 'last bit' in ASYNC is simply the last stop bit of the character. In BOP and COP, the last character is defined either explicitly by either appending it with TEOM or implicitly through the selection of the frame underrun control sequence, TPR[7:6] (Transmitter Parameter Register). Table 13 summarizes the relationship of the selected underrun sequence and the protocol mode.

Tx CTS Operation

If CTS enable Tx, TPR[2], is set, the CTSN input must be asserted for the transmitter to operate. Changes in CTSN while a character is being transmitted do not affect transmission of that character. However, if the CTS input becomes negated when TPR[2] is set and the transmitter is enabled and ready to start sending a new character, CTS underrun, TRSR[6], is asserted and the TxD output is placed in the marking (High) state. In ASYNC mode, operation resumes when CTSN is asserted again. In COP and BOP modes, the transmission of the message is terminated and operation of the transmitter will not resume until CTS is asserted and a TSOM or TSOMP command is invoked. Prior to issuing the command and retransmitting the message, the transmitter must be reset. After a change-of-state STS is established by the input sampling circuits (refer to the description of ICTSR[4], it is sampled by the Tx controller 1-1/2 bit times before each new character is serialized out of the Tx shift register. (This is 2-1/2 bits before the LSB of the new character appears on the TxD pin; there is an additional 1-bit delay in the transmitter data path due to the data encoding logic.)

Tx Special Bit Pattern Transmission

The DUSCC provides features transmit special bit patterns (see Table 14).

The TxD pin is held marking after a hardware reset, a reset Tx command, when the transmitter is not enabled, and during underrun/idle, if this feature is selected through TPR[7:5]. The TxD pin is also held marking if the transmitter is enabled, and the TxFIFO is empty (ASYNC), or if a TSOM or TSOMP command has not been issued (SYNC modes).

The following command bits can be appended to characters in the TxFIFO: TEOM, TDLE, exclude from CRC, and reset TxCRC. An invoked command(s) is appended to the next character loaded into the TxFIFO and follows the character through the FIFO until that character is ready to be loaded into the TxSR. The transmitter for the various protocols.

Tx ASYNC Mode

Serialization begins when the TxFIFO data is loaded into the TxSR. The transmitter first sends a start bit, then the programmed number of bits/character (TPR[1,0]), a parity bit (if specified), and the programmed number of stop bits. following the transmission of the stop bits, if a new character is not available in the TxFIFO, the TxD output goes to marking and the underrun condition (TRSSR[7]) is set.

Transmission resumes when the CPU loads a new character into the TxFIFO or issues a send break command. The send break command clears the TxFIFO and forces a continuous space (Low) on the TxD output after the character in TxSR (if any) is serialized. A send break acknowledge (TRSR[4]) is returned to the CPU to facilitate reassertion of the send break command in order to send an integral number of break characters. The send break condition is cleared when the reset Tx or disable Tx command is issued.

Tx COP Modes

Transmitter commands associated with all COP modes are: transmit SOM (TSOM, transmit start of message), transmit SOM with PAD (TSOMP0, transmit EO (TEOM, transmit end of message), reset TxCRC, exclude from CTC, and transmit DLE.

A TSOM or send TSOMP command must be issued to start COP transmission. TSOM (without PAD) causes the TxCRC/LRC generator to be initialized and one or two SYN characters from S1R/S2R to be loaded into the TXSR and shifted out on the TxD output. A parity bit, if specified, is appended to each SYN character after the MSB. Send SOM acknowledge (TRSR[4]) is asserted when the SYN output begins. The user may reinvoke the command to cause multiple SYNs to be transmitted. If the command is not reinvoked and the TxFIFO is empty, SYN patterns continue to be transmitted until the TxFIFO is loaded. If data is present in the FIFO, the first character is loaded into the TxSR and serialization of the data begins. Note that the TxFIFO may be preloaded with data before the TSOM is issued.

The TSOMP command causes all characters in the TxFIFO (PAD characters) to be loaded into the TxSR and serialized if the Tx is enabled. Unlike the transmit SOM without PAD command, data (non-PAD characters) cannot be preloaded into the TxFIFO. While the PAD is transmitted, parity is disabled and character length is automatically set to 8 bits regardless of the value in TPR[1:0]. When the TxFIFO becomes empty after the PAD, the TxCRC/LRC generator is initialized, the SYN character(s) are transmitted with optional parity appended, and send SOM acknowledge asserted. Operation then proceeds in the same manner as the TSOM command; the user has the option to invoke the TSOM command to cause multiple SYNs to be transmitted.

After the TSOM/TSOMP command is executed, characters in the TxFIFO are loaded into the TxSR and shifted out with a parity bit, if specified, appended after the MSB. If, after the opening SYN(s) and at least one data has been transmitted, the TxFIFO is empty, a data underrun condition results and TRSR[7] is asserted. The transmitter's action on data underrun is determined by TPR[7:6] and the COP protocol. If TRP[7:6] = '10', the transmitter line fills with MARK characters until a character is loaded into the FIFO. I TRP[7:6] and the COP protocol. If TPR[7:6] = '11' is selected, the transmitter line fills with SYN, SYN1-SYN2, or DLE-SYN1 for monosync, dual sync, and BISYNC transparent modes, respectively. If TPR[7:6] = '00', the BCC characters are transmitted and frame complete (TRSR[6]) is set. TxD then assumes the programmed idle state (TPR[5]) of MARKs or SYN1/SYN1-SYN2.

Operation resumes with the transmission of a SYN sequence when a TSOM command is invoked. A TSOMP command is ignored unless the transmitter is disabled and then reenabled.

An appended TEOM command also terminates the frame as described above. It occurs after transmission of the character to which the TEOM is appended. The TEOM command can be explicitly asserted through the channel command register. If TPR[4] = '1', the TEOM is automatically appended to a character in DMA mode, if the DONEN input is asserted when that character is loaded into the TxFIFO, or if the counter/timer is counting transmitted characters when the character which causes the counter to reach zero count is loaded.

The TDLE command when appended to a character in the TxFIFO, causes the DLE character to be loaded into the the TxSR and serialized before the TxFIFO character is loaded into the TxSR and serialized. This feature is particularly useful for BISYNC operation. The DLE character will be excluded from the CRC accumulation in BISYNC transparent mode (see below), but will be included in all other COP modes.

In BISYNC mode, transmission of a DLE-STX character sequence (either via a send TDLE command appended to the STX character, or via DLE and STX loaded into the TxFIFO) puts the transmitter into the transparent test mode of operation. In this mode, normally restricted character sequences can be transmitted as 'normal' bit sequences. The switch occurs after transmission of the two characters, so that the DLE and STX are included in the BCC accumulation. If the DLE-STX is to be excluded from the CRC, the user should issue a 'reset CRC' command prior to loading the next character

Another method of excluding the two characters from the CRC is to invoke the 'exclude from CRC' command prior to loading the character(s) into the FIFO. While in transparent mode, the transmitted line fills with DLE-SYN1 and automatically transmits an extra DLE if it finds a DLE in the TxFIFO ('DLE stuffing'). The transmitter reverts to non-transparent mode when the frame complete status is set in TRSR[5].

CRC/LRC accumulation can be specified in all COP modes; the type of CRC is specified via CMR2[2:0]. The TSOM/TSOMP commands set the CRC/LRC accumulator to its initial state and accumulation begins with the first non-SYN character after the initial SYN(s) are transmitted. PAD characters are not subject to CRC accumulation. In non-BISYNC or BISYNC normal modes, all transmitted characters except linefill characters (SYNs or MARKs) are subject to accumulation. In BISYNC transparent mode, odd (stuffed) DLEs and the DLE-SYN1 linefill are excluded from the accumulation. Characters can be selectively excluded from the accumulation by invoking the 'exclude form CRC' command prior to loading the character into the FIFO.

Accumulation stops when transmission of the first character of the BCC begins. The CPU can set the accumulator to its initial state prior to the transmission of any character by using the appended reset CRC command. The CRC generator is also automatically initialized after the EOM is sent

Table 13. Abort Sequence—Protocol Mode

TPRA[7:6]	PROTOCOL	LAST CHARACTER
00	BOP	FLAG following either FCS (if selected) or last data character
	COP	Last byte of FCS before line begins SYN or MARKing
10	BOP	Abort sequence (11111111) prior to MARKing
	COP	Last byte of FCS before line begins SYN or MARKing
11	BOP	Abort sequence (11111111) prior to FLAG
	COP	First SYN of SYN sequence

Table 14. Special Bit Patterns

PROTOCOL	BIT PATTERN
ASYNC-BREAK	An all 0's character including parity bit (if specified) and stop bits. Used for send break command.
COP-SYN	Contained in S1R (single SYN mode) or in S1R/S2R (dual SYN modes). Used for TSOM and TSOMP commands and for non-transparent mode linefill and IDLE.
COP-DLE	Used for TDLE command and for BISYNC transparent mode linefill and to generate BISYNC control sequences.
COP-CRC	16/8 bits from the CRC/LRC accumulator used for TEOM command or for auto-EOM modes.
BOP-FLAG	01111110. Used for TSOM, TSOMP, and TEOM commands, for auto-EOM modes, and as an IDLE line fill.
BOP-ABORT	11111111. Used for send ABORT command or during TxFIFO underrun.
BOP-CRC	16 bits from the CRC accumulator used for TEOM command or for auto-EOM modes.
BOP/COP MARK	All 1's pattern on data line.

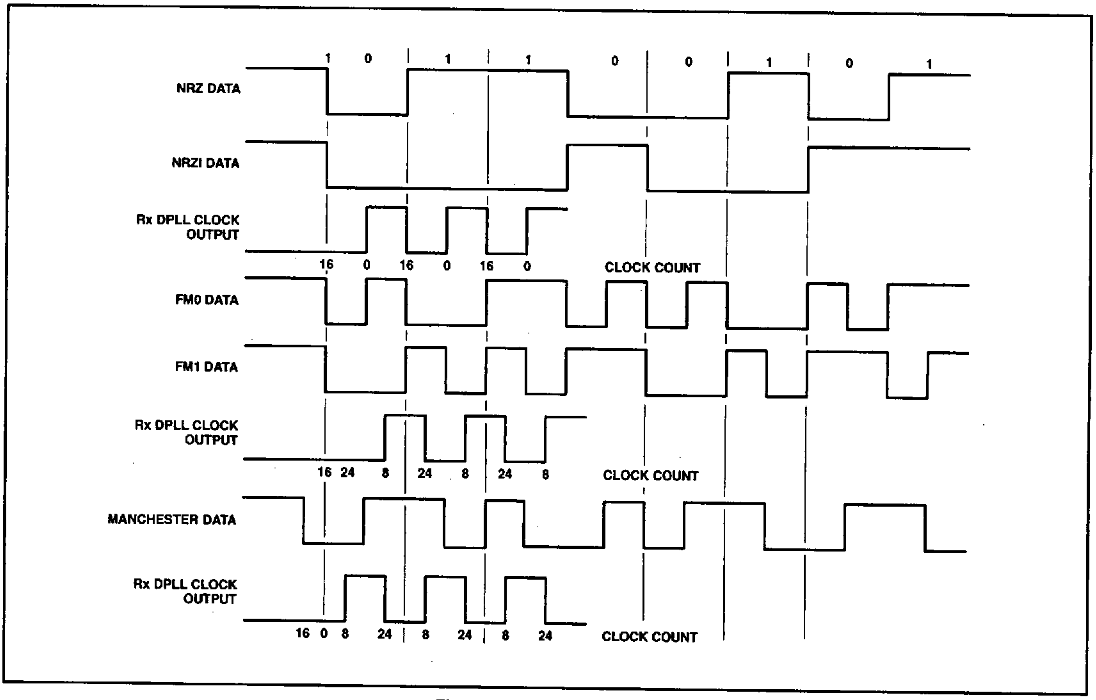


Figure 9. DPLL Waveforms

TxBOP Modes

Transmitter commands associated with BOP modes are TSOM, TSOMP, TEOM, and transmit ABORT (TABRK). The TSOM and TSOMP commands are identical to COP modes except that a FLAG character (01111110) is used as the start of message sequence instead of the SYNs, and FLAG(s) that continue to be sent until the TxFIFO is loaded. There is no zero insertion (see below) during transmission of the PAD characters, and they are not preceded by a FLAG or accumulated in the CRC. Character length is automatically set to 8 bits regardless of TPR[1:0].

The first characters loaded into the TxSR from the TxFIFO are the address and control fields, which have fixed character lengths of eight bits. The number of address field bytes is determined by CMR1[4:3]. If extended address field is specified, the field is terminated if the first address octet is H'00' or if the LSB of the octet is a 1. The number of control field bytes is selected by CMR1[5]. If any information field characters follow the control field (forming an I field), they are transmitted with the number of bits per character programmed in TPR[1:0]. The TEOM command can be appended to the last character whether explicitly or automatically as described for COP mode. When the character with the appended TEOM is loaded from the TxFIFO, it is transmitted with the character length specified by OMR[7:5]. In this way, a residual character of 1 - 8 bits is transmitted without requiring the CPU to change the Tx character length for this last character.

After opening the FLAG and first address octet have been transmitted, an underrun occurs (TRSR[7] = 1) if the TxFIFO is empty when the transmitter requires a new character. The underrun control bits (TPR[7:6]) determine whether the transmitter line fills with either ABORT-MARKs, ABORT-FLAGs (see below), or ends transmission with the 'normal' end of message sequence.

EOM on underrun is functionally similar to EOM due to an appended TEOM command. If the EOM is due to underrun, the normal character length applies to the last data character. After the last character is transmitted, the FCS (inverted CRC) and closing FLAG are sent, frame complete (TRSR[5]) is set, and the TxCRC is initialized. If the TxFIFO is empty after the closing FLAG has been sent, TXD will assume the programmed idle state of FLAGs or MARKs (TPR[5]) and wait for a character to be loaded into the FIFO or for a TSOM command to be issued. If the TXFIFO is not empty at that time, the TxFIFO data will be loaded into the TxSR and serialized. In that case, the closing FLAG is the opening FLAG of the next frame.

The user can control the number of FLAGs between frames by invoking the TSOM command after frame complete is asserted. The DUSCC then operates in the same manner as for transmission of multiple FLAGs at the beginning of a frame. When the command is no longer reinvoked, transmission of the TxFIFO data will begin. If the FIFO is empty, FLAGs continue to be transmitted

The DUSCC provides automatic zero insertion in the data stream to prevent erroneous transmission of the FLAG sequence All data characters loaded into the TxSR from the TxFIFO and characters transmitted from the CRC generator are subject to zero insertion For this feature a zero is inserted in the serial data stream each time five consecutive ones (regardless of character boundaries) have been transmitted.

A send ABORT command clears the TxFIFO and inserts an ABORT character of eight ones (not subject to zero insertion) into the TxSR for transmission after the current character has been serialized. A send abort ack (TRSR[4]) facilitates reassertion of send abort by the user to guarantee transmission of multiple abort characters. This feature can be used to send the 15-ones idle sequence.

The transmitter sends either marks or FLAGs after the abort character(s) has been transmitted, depending on TPR[7:6]. Operation resumes with the transmission of a FLAG when a TSOM command is invoked. A TSOMP command is ignored unless the transmitter is disabled and then reenabled.

CRC accumulation can be specified in all BP modes. The type of CRC is specified via CMR2[2:0], and is normally selected as CRC-CCITT preset to ones, although any option is valid. Note that LRC8 option is not allowed in BOP modes.

The TSOM/TSOMP command sets the CRC accumulator to its initial state and accumulation begins with the first address octet after the initial FLAG(s). Accumulation stops when transmission of the first character of the FCS begins. The CPU can set the accumulator to its initial state prior to the transmission of any character by using the appended reset CRC command and can exclude any character from the accumulation by use of the exclude from CRC command, but these features would not normally be used in BOP modes The CRC generator is also automatically initialized after the EOM or an ABORT are sent.

TxBOP Loop Mode

The loop modes are used by secondary stations on the loop, while the primary station operates in the BOP primary mode. Both the transmitter and receiver must be enabled and should be programmed to use the same clock source. Loop operation is initiated by issuing the 'go on-loop' command. The receiver looks for the receipt of seven contiguous ones and then asserts the LCN output to cause external loop control hardware to put the DUSCC into the loop, with the TxD output echoing the RxD input with a 2-bit time delay The echoing process continues until a Go Active on Poll (GAP) command is invoked. The DUSCC then looks for receipt of an EOP bit pattern (a zero followed by seven ones, 11111110) and changes the last one of the EOP into a zero making it an opening FLAG. Loop sending (TRSR[6]) is asserted at that same time. The action of the transmitter after sending the initial FLAG depends on the status of the transmit FIFO.

If the transmit FIFO is not empty, a normal frame transmission begins. The operation is then similar to normal BOP operation with the following differences:

1. An ABORT command, an underrun, or receipt of the turnaround sequence (H'00') or FLAG cause the transmitter to cease operation and to revert to echoing the RxD input with a 2-bit time delay A new transmission cannot begin until the GAP command is reinvoked and a new EOP sequence is received
2. Subsequent to sending the EOM sequence of FCS-FLAG, the DUSCC examines the internal GAP flip-flop If it is not set (having been reset by the 'reset GAP' command, the DUSCC reverts to echoing the received data If the internal GAP flip-flop is still set, transmission of a new frame begins, with the user having control of sending multiple FLAGs between frames by use of the 'send SOM' command. If the FIFO is empty at this time, the DUSCC continues to send FLAGs until the data is loaded into the FIFO or until GAP is reset. If the latter occurs, it reverts to echoing RxD.

   When the DUSCC reverts to echoing RxD in any of the above cases, the last transmitted zero and seven ones will form an EOP for the next station down the loop.

   If the TxFIFO is empty when the EOP is recognized, the transmitter continues to send FLAGs until there is data in the FIFO If a turnaround sequence or the reset GAP command is received before the FIFO is loaded, the transmitter switches to echoing RxD without any data transmission. Otherwise a frame transmission begins as above when a character is loaded into the FIFO. The mechanism provides time for the CPU to examine the received frame (the frame preceding the EOP) to determine if it should respond or not, while holding its option to initiate a transmission.

Termination of operation in the loop mode should be accomplished by use of the 'go off-loop' command. When the command is invoked, the DUSCC looks for the receipt of eight contiguous ones It then negates the LCN output to cause the external loop control hardware to remove the DUSCC from the loop without affecting operation of other units remaining on the loop.

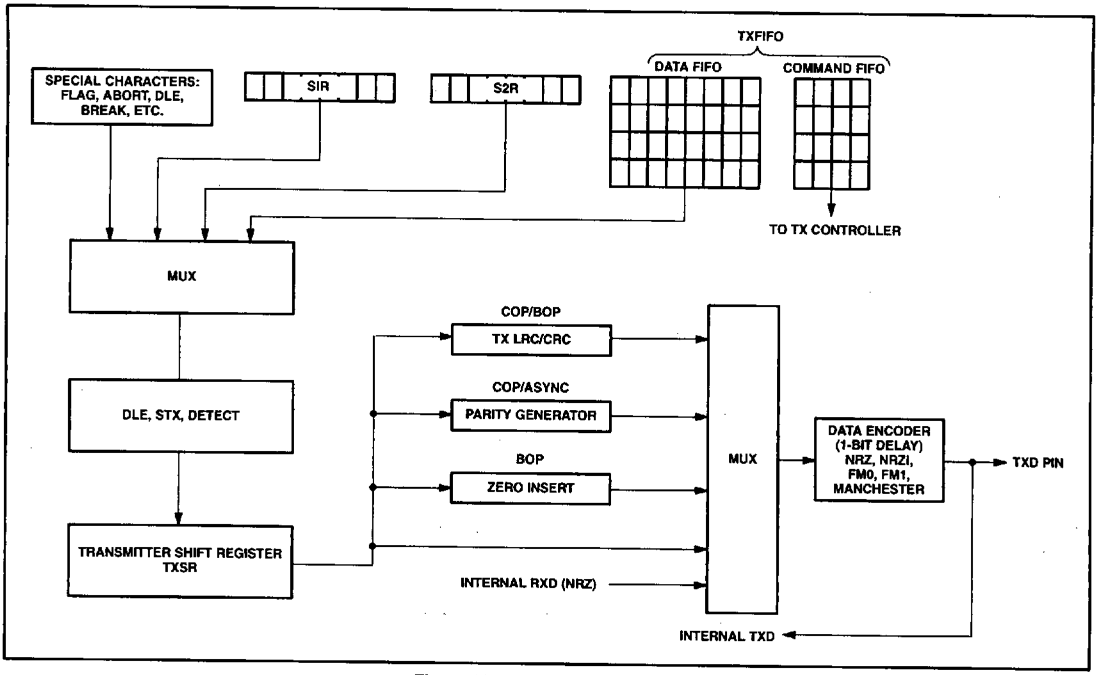


Figure 10. Transmitter Data Path

RECEIVER

The receiver data path includes two 9-bit holding registers, HSRH and HSRL, an 8-bit character comparison register, CCSR, two synchronizing flip-flops, a receiver shift register, RxST, the programmable SYN comparison registers, S1R and S2R, and BISYNC character comparison logic. The DUSCC configures the circuitry and utilizes it according to the operational mode selected for the channel through the two mode registers CMR1 and CMR2. For all data paths, character data is assembled according to the character bit count, in the RxSR, and is moved to the RxFIFO with any appended statuses when assembly is completed. Figure 1 depicts the four data paths created in the DUSCC for the previous protocols.

Receiver RxFIFO, RxRDY

The receiver converts received serial data on RxD (LSB first) into parallel data according to the transmission format programmed. Data is shifted through a synchronizing flip-flop and one or more shift registers, the last of which is the 8-bit receiver shift register (RxST). Bits are shifted into the RxSR on the rising edge of each 1X receive clock until the LSB is in RxSR[0]. Hence, the received character is right justified, with all unused bits in the RxSR cleared to zero. A receive character length counter generates a character boundary signal for synchronization of character assembly, character comparisons, break detection (ASYNC), and RxSR to RxFIFO transfers (except for BOP residual characters). During COP and BOP hunt phases, the SYN/GLAG comparison is made each receive bit time, as abort, and idle comparisons in BOP modes.

An internal clock from the BRG, the DPLL or the counter/timer, or an external 1X or 16X clock may be used as the receiver clock in ASYNC mode. The BRG or counter/timer cannot be used directly for the receiver clock in synchronous modes, since these modes require a 1X receive clock that is in phase with the received data. This clock may come externally from the RTxC or TRxC pins, or it may be derived internally from the DPLL. Received data is internally converted to NRZ format for the receiver circuits by using clock pulses generated by the DPLL.

When a complete character has been assembled in the RxSR, it is loaded into the receive FIFO with appended status bits. The most significant data bits of the character are set to zero if the character length is less than eight bits. In ASYNC and COP modes the user may select, via RPR[3], whether the data transferred to the FIFO includes the received parity bit or not. The receiver indicates to the CPU or DMA controller that it has data in the FIFO by asserting the channel's RxRDY status bit (GSR[4] or GSR[0] and, if in DMA mode, the corresponding receiver DMA request pin.

The RxFIFO consists of four 8-bit holding registers with appended status bits for character count complete indications (all modes), character compare indication (ASYNC), EOM indication (BISYNC/BOP), and parity, framing, and CRC errors. Data is loaded into the RxFIFO from the RxSR and extracted (read) by the CPU or DMA controller via the data bus. AN RxFIFO read create an empty RxFIFO position for new data from the RxSR.

RxRDY assertion depends on the state of OMR[3]:

1. If OMR[3] is 0 (FIFO not empty), RxRDY is asserted each time a character is transferred form the receive shift register to the receive FIFO. If it is not reset by the CPU, RxRDY remains asserted until the receive FIFO becomes empty, at which time it is automatically negated. If it is reset by the CPU, it will remain negated, regardless of the current state of the receive FIFO, until a new character is transferred from the RxSR to the RxFIFO.

2. If OMR[3] is 1 (FIFO full), RxRDY is asserted:

a. When a character transfer from the receive shift register to the receive FIFO causes it to become full.

b. When a character with a tagged EOM status bit is loaded into the FIFO (BISYNC or BOP) regardless of RxFIFO full condition.

c. When the counter/timer is programmed to count received characters and the character which causes it to reach zero count is loaded into the FIFO (ICTSR[6]).

d When the beginning of break is detected in ASYNC mode regardless of the RxFIFO full condition.

If it is not reset by the CPU, RxRDY remains asserted until the FIFO becomes empty, at which time it is automatically negated. If it is reset by the CPU, it will remain negated regardless of the current state of the receive FIFO, until it is asserted again due to one of the above conditions.

The assertion of RxRDY causes an interrupt to be generated if IER[4] and the channel's master interrupt enable (ICR[0] or ICR[1]) are asserted.

When DMA operation is programmed, the RxRDY status bit is routed to the DMA control circuitry for use as the channel receiver DMA request. Assertion of RxRDY results in assertion of RTxDRQN output.

Several status bits are appended to each character in the RxFIFO. When the FIFO is read, causing it to be 'popped', the status bits associated with the new character at the top of the RxFIFO are logically ORed into the RSR. Therefore, the user should read RSR before reading the RxFIFO in response to RxRDY activation. If character-by character status is desired, the RSR should be read and cleared each time a new character is received. The user may elect to accumulate status over several characters or over a frame by clearing RSR at appropriate times. This mode would normally also be used when operating in DMA mode. If the RxFIFO is empty when a read is attempted, and wait mode as specified in CMR2[5:3], is not being used, a H'FF' is output on the data bus.

In all modes, the DUSCC protects the contents of the FIFO and the RxSR from overrun. If a character is received while in FIFO is full and a character is already in the RxSR waiting to be transferred into the FIFO, the overrunning character is discarded and the OVERRUN status bit (RSR[5]) is asserted. If the overrunning character is an end-of-message character, the character is lost but the FIFOed EOM status bit will be asserted when the character in the RxSR is loaded into the FIFO.

Operation of the receiver is controlled by the enable receiver command. When this command is issued, the DUSCC goes into the search for start bit state (ASYNC), search for SYN state (COP modes), or search for FLAG state (BOP modes). When the disable receiver command is issued, the receiver ceases operation immediately. The RxFIFO is cleared on master reset, or by a rest receiver command. However, disabling the receiver does not affect the RxFIFO, RxRDY, or DMA request operation.

Receiver DCD and RTS Controls
If DCD enable Rx, RPR[2], is asserted, the DCD input must be asserted and the sampling circuit detects that the DCD input has been negated, the receiver ceases operation immediately. Operation resumes when the sampled DCD is asserted again. A change of state detector is provided on the DCD input of each channel. The required duration of the DCD level change is described in the discussion of ICTSR[5]. The user may program a change of state to cause an interrupt to be generated (master interrupt enable ICR[0] or [1] and IER[7] must be set) so that appropriate action can be taken.

In ASYNC mode, RPR[4] can be programmed to control the deactivation of the RTSN output by the receiver. RTSN can be manually asserted and negated by writing to OMR[0]. However, the assertion of RPR[4] causes RTS to be negated automatically upon receipt of a valid start bit if the channel's receive FIFO is already full. When this occurs, the RTSN negated status bit, RSR[6], is set. This may be used as a flow control feature to prevent overrun in the receiver by using the RTSN output signal to control the CTSN input of the remote transmitter. The new character will be assembled in the RxSR, but its transfer to the FIFO will be delayed until the CPU reads the FIFO, making the FIFO position available for the new character.

Once enabled, receiver operation depends on channel protocol mode. The following describes the receiver operation for the various protocols.

RxASYNC Mode
When first enabled, the receiver goes into the search for start bit state, looking for a High-to-Low (mark-to-space) transition of the start bit on the RxD input. If a transition is detected, the state of the RxD pin is sampled again each 16X clock for 71/2 clocks (16X clock mode) or at the next rising edge of the bit time clock (1X clock mode). If RxD is sampled High, the start bit is invalid and the search for a valid start bit begins again.

If RxD is still Low, a valid start bit assumed and the receiver continues to sample the input at one bit time intervals (16 periods of the 16X Rx clock; one period of the 1X Rx clock) at the theoretical center of the bit, until the proper number of data bits and the parity bit (if specified) have been assembled, and the first stop bit has been detected

The assembled character is then transferred to the RxFIFO with appended parity error (if parity is specified) and framing error status bits. The DUSCC can be programmed to compare this character to the contents of S1R. The appended character compare status bit, RSR[7], is set if the data matches and there is no parity error.

After the stop bit is sampled, the receiver will immediately look for the next start bit. However, if a non-zero character was received without a stop bit (i.e., framing error) and RxD remains Low for one-half of the bit period after the stop bit was sampled, then the receiver operates as if a new start bit transition had been detected at that point (one-half bit time after the stop bit was sampled).

If a break condition is detected (RxD Low for entire character time including optional parity and first stop bit), only one character consisting of all zeros will be loaded into the RxFIFO and break start detect, RSR[2], will be set. The RxD input must return to a High condition for at least one half of a bit time (16X clock mode) or for one bit time (1X clock mode) before the break condition is terminated and the search for the next start bit begins. At that time, the break end detect condition, RSR[3], is set. Note that the maximum speed in the receiver when in asynchronous mode must not exceed 2Mbs.

Rx COP Modes
When the receiver is enabled in COP modes, it first goes into the SYN hunt phase, testing the received data each bit time for receipt of the appropriate SYN bit pattern, Plus parity if specified, to establish character boundaries. Receipt of the SYN bit pattern terminates hunt phase and places the receive in the data phase, in which all leading SYNs are stripped and the RxFIFO begins to load starting with the first non-SYN character. In COP single SYN protocol mode, S1R contains the SYN character required to establish character synchronization. In COP dual SYN and BISYNC protocol modes, S1R and S2R contain the first and second SYN characters, respectively, required to establish character synchronization. The SYN character length is the same as the character length

programmed in RPR[1:0], plus the parity bit if parity is specified. SYN characters received with a parity error, when parity is specified, are considered invalid and will not cause synchronization to be achieved.

In COP mode, resetting the receiver clears the receiver data path, while disabling the receiver does not. If not reset, partial sync patterns remaining in the receiver will be recognized when it is enabled.

If external synchronization is programmed (RPR[4] = 1), the internal SYN detection and special character recognition logic are disabled and receipt of SYN characters is not required. A pulse on the SYNI input pin will establish character synchronization and terminate hunt phase. The SYNI pin is ignored after the first input on the SYNIN pin is received. The receiver must be disabled and then reenabled to resynchronize or to return to normal mode. This must be programmed in conjunction with CMR1[2:0] = 110. Refer to the description of RPR[4] for further details

The SYN detect status bit RSR[2], is set whenever SYN1, SYN1-SYN2, or DLE-SYN1 is detected for single SYN, dual SYN/BISYNC normal, and BISYNC transparent modes, respectively, and the SYNOUT pin will go active for one receive clock period one bit time after SYN detection in HSRH/HSRL. After character sync has been attained, the receiver enters the data phase and assembles characters in the RxSR, beginning with the first non-SYN character, with the least significant bit received first. It computes the BCC if specified, checks parity if specified, and checks for overrun errors.

The operation of the BCC (CRC/LRC) logic depends on the particular COP mode in use. The BCC is initialized upon first entering the data phase. For non-BISYNC modes, all received characters after entering data phase are included in the BCC computation, except for leading SYNs and SYNs which are specified to be stripped by RPR[7]. As each received character is transferred from the RxSR to the FIFO, the current value of the BCC characters is checked and the CRC ERROR status bit (RSR[1]) is set if the value of the CRC remainder is not the expected value. RSR[1] gets set when the character reaches the top of the FIFO. The EOM status bit, RSR[7], is not set since there is no defined end-of-message character. The receiver computes the BCC for test messages automatically when operating in BISYNC protocol mode.

BISYNC Features

The DUSCC provides support for both BISYNC normal and transparent operations. The following summarizes the features provided. Both EBCDIC and ASCII text messages can be handled by the DUSCC as selected by CMR1[5]. The receiver has the capability of recognizing special characters for the BISYNC protocol mode (see Table 15).

All sequences in Table 15, except SOH and STX, when detected explicitly cause a status to be affected. The following describes the conditions when this occurs.

The first character received when entering data phase for a header or text message should be an SOH, an STX, or a DLE-STX two-character sequence. Receipt of any of these initializes the CRC generator and starts the CRC accumulation. The SOH places the receiver in header mode, receipt of the STX places it in text mode, the receipt of the DLE-STX sequence (at any time) automatically places the receiver in transparent mode and sets the XPNT mode status bit, TRSR[0]. There is no explicit status associated with SOH and STX. If any characters are received when entering the data phase, the message is treated as a control message and will not be accumulated in CRC.

After the data phase is established, the receiver searches the data stream for an end of message control character(s):

Header field: ENQ, ETB, or ITB

Normal text field: ENQ, ETX, ETB, or ITB

Transparent text field: DLE-ENQ, DLE-ETX, DLE-ETB, or DLE-ITB

Control message field: EOT, NAK, ACK0, ACK1, WACK, RVI or TTD

Detection of any one of these sequences causes the EOM status bit, RSR[7], to be set. Also if RPR[5] is set and the receiver does not detect a closing PAD (four 1's) after the 'EOT' or 'NAK', the PAD error status bit, RSR[6], is set. When the abort sequence ENQ or DLE-ENQ is detected, the character is tagged with an EOM status and transferred to the FIFO, but the appended CRC error status bit should be ignored. For the other EOM control sequences, the receiver waits for the next two bytes (the CRC bytes) to be received, checks the value of the CRC generator, and tags the transferred character with a CRC error, RSR[1], if the CRC remainder is not correct. See Figure 11 for an example of BCC accumulation in various BISYNC messages.

The CRC bytes are normally not transferred to the FIFO, unless the transfer FCS to FIFO control bit, RPR[6], is asserted. In this case the EOM and CRC error status bits will be tagged onto the last byte of the last FCS byte instead of to the last character of the message. After detecting one of the End-Of-Message (EOM) character sequences and setting RSR[7], the receiver automatically goes into auto hunt mode for the SYNC characters and PAD check if RPR[5] is set.

SYN Pattern Stripping

Leading SYNs (before a message) are always stripped and excluded from the FCS, but SYN patterns within a message are treated by the receiver according to the RPR[7] bit. SYN character patterns are defined for the various COP modes as follows:

COP single SYN mode—SYN1

COP dual SYN mode—SYN1, and SYN2 when immediately preceded by SYN1.

BISYNC normal mode—SYN1, and SYN2 when immediately preceded by SYN1. SYN1 is always stripped, even if it is not followed by SYN2 when stripping is selected.

BISYNC transparent mode—DLE-SYN1, where the DLE is the last of an odd number of consecutive DLEs.

0 Strip only RPR[7] leading the SYN and do not accumulate in FCS.

1 Strip all SYNs. Additionally, strip odd DLEs when operating in BISYNC transparent mode. Do not accumulate stripped characters in FCS.

Processing of the SYN patterns is determined by the RPR[7] bit, the COP mode, and the position of the pattern in the frame. This is summarized in Table 16.

The value of the RPR[7] field does not affect the setting of the SYN DETECT status bit, RSR[2], and the generation of a SYNOUT pulse when a SYN pattern is received.

RxBOP Mode

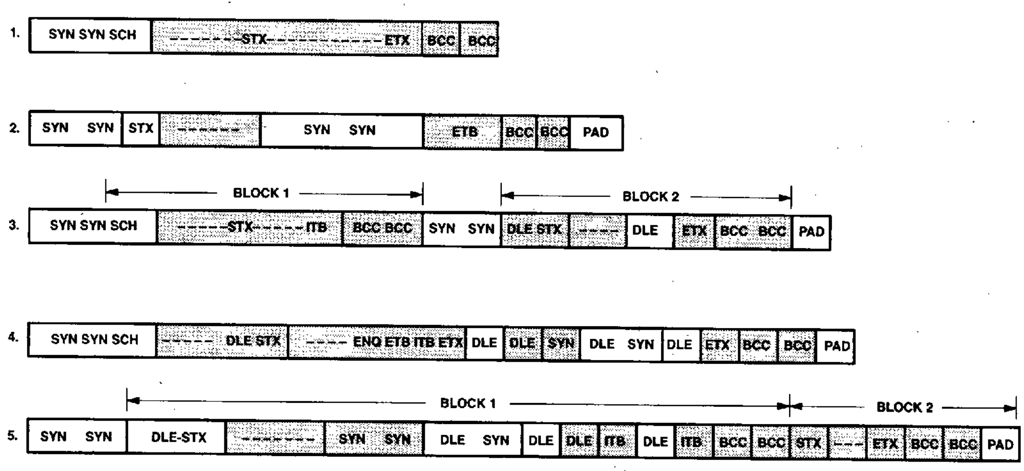
In BOP protocol mode, the receiver may be in any one of four phases: hunt phase, address field (A) phase, control field (C) phase, or information field (I) phase. The character length for the A and C phases is always 8 bits. The I field character length is specified in RPR[1:0].

Note that if the residual character length is not zero, the unused most significant bits in the receiver FIFO are not necessarily zero. the unused bits should be ignored, this will not cause a CRC error.

After an enable receiver command is executed, the receiver enters hunt phase, in which a comparison for the string (01111110) is done every Rx bit time. The FLAG delineates the beginning (and end) of a received frame and establishes the character boundary. Each FLAG match in CCSR causes the FLAG detect status bit (RSR[2]) to be set and SYNOUTN pin to be activated one bit time later for one receive clock period. FLAGs with an overlapping zero will be detected. All FLAGs are deleted from the data stream.

Table 15. BISYNC Features

BISYNC—Single-Character Sequences			
Sequences	**ASCII**	**EBCDIC**	**Description**
SOH	H'01'	H'01'	Start of header
STX	H'02'	H'02'	Start of text
ETX	H'83'	H'03'	End of text
EOT	H'04'	H'37'	End of transmission
ENQ	H'85'	H'2D'	Enquiry
DLE	H'10'	H'10'	Data link escape
NAK	H'15'	H'3D'	Negative ack
ETB	H'97'	H'26'	End of transmission block
ITB	H'1F'	H'1F'	End of intermediate transmission block
BISYNC—Two-Character Sequences			
Sequence	**ASCII**	**EBCDIC**	**Description**
ACK0	H'10,B0'	H'10,70'	Acknowledge 0
ACK1	H'10,31'	H'10,61'	Acknowledge 1
WACK	H'10,3B'	H'10,6B'	Wait before transmit positive ack
RVI	H'10,BC'	H'10,7C'	Reverse interrupt
TTD	H'02,85'	H'02,2D'	Temporary text delay
BISYNC—(Transparent Text Mode)—Two-Character Sequences			
Sequence	**ASCII**	**EBCDIC**	**Description**
DLE-ENQ	H'10,85'	H'10,2D'	Enquiry
DLE-ITB	H'10,1F'	H'10,1F'	End of intermediate transmission block
DLE-ETB	H'10,97'	H'10,26'	End of transmission block
DLE-ETX	H'10,83'	H'10,03'	End of text
DLE-STX	H'10,02'	H'10,02'	Start of transparent text mode



NOTES:
The BCC accumulator is stopped after the end of message character sequence is accumulated. All shaded areas are accumulated.
ENQ (DLE - ENQ) in a text message should be treated as an abort.
Opening SYNs will be stripped by the receiver.

Figure 11. Example of BCC Accumulation in Various BISYNC Messages

Table 16. SYN Pattern Processing

MODE	RPR [7]	LEADING SYNs	WITHIN A MESSAGE
BISYNC	0	no FCS no FIFO	no FCS Pattern into FIFO
	1	no FCS no FIFO	no FCS no FIFO
COP	0	no FCS no FIFO	Accumulate in FCS Pattern into FIFO
	1	no FCS no FIFO	no FCS no FIFO

Once a FLAG has been detected, the receiver will exit hunt phase and enter address phase. The handling of the address field is determined by the values programmed in CMR1[2:0], which selects one of the BOP modes. The BOP secondary address modes are selected by CMR1[4:3] and function as in the description that follows.

Single-Octet Address
For receive, the address comparison for a secondary station is made on the first octet following the opening FLAG. A match occurs if the first octet after the FLAG matches occurs if the first octet after the FLAG matches the contents of S1R, or if all parties address (RPR[3]) is asserted and the first octet is equal to H'FF'.

Dual Octet Address
For receive, the address comparison for a secondary station is made on the first two octets following the opening FLAG.

A match occurs if the first two octets after the FLAG match the contents of S1R and S2R respectively, or if all parties address (RPR[3]) is asserted and the first two octets are equal to H'FF, FF'.

Dual Address with Group Mode
For receive, the address comparison for a secondary station is made on the first two octets following the opening FLAG. A match occurs for one of three possible conditions. If the first two octets after the FLAG match the contents of S1R and S2R, respectively, or if the first octet is H'FF' and the second matches the contents of S2R (group mode), or when all parties address (RPR[3]) is asserted and the first two octets are equal to H'FF,FF'. The second condition (group mode) allows a selected group of stations to receive a message.

Extended Address Mode
Extend address field to the next octet if the LSB of the current address octet is zero. Address field is terminated if the LSB of the address is a one. The address field will be terminated after the first octet if the null address H'00' is received/transmitted as the first address octet. For this mode the receiver does not perform an address comparison (all received characters after the opening FLAG are transferred to the FIFO) but does determine when the address field is terminated.

The length of the A field may be a single octet, a dual octet, or more octets, as described above. A primary station or an extended address secondary station does not perform an address comparison, and all characters in the A, C, and I fields after the flag are transferred to the FIFO. Although address field comparisons are not performed, the length of the address field is still determined by CMR1[4:3]. For the other secondary address modes, if there is a match, or the received character(s) match either of the other enabling conditions (group or all-parties address), all characters in the A, C, and I field are transferred to the FIFO. If there is no match, the receiver returns to the FLAG hunt phase.

C phase begins after A phase is terminated. The receiver receives one or two control characters, CMR1[5]. After this phase is terminated, the character length is switched automatically from 8 bits to the number of bits specified in RPR[1:0] and the information field phase is entered.

The frame is terminated when a closing FLAG is detected. The same FLAG can also serve as the opening FLAG of the next frame. The 16 bits received prior to the closing FLAG form the frame check sequence (if an FCS is specified in CMR2[2:0]). All non-FLAG characters of the frame are accumulated in the CRC checker and the result is compared to the expected remainder. Failure to match will cause a CRC error. EOM detect RSR[7], RCL not zero RSR[0], and CRC error RSR[1] are normally FIFOed with the last character of the I field. RCL not zero RSR[0] is set if the length of the last character of the I field does not have the length programmed in RPR[1:0]. The residual character length in TRSR[2:0] is also valid at that time. The CRC characters themselves are normally not passed to the RxFIFO. However, if the transfer FCS to FIFO control bit RPR[6] is asserted, the FCS bytes will be transferred to the FIFO. In this case the EOM, CRC error, and RCL not zero status bits will be tagged onto the last byte of the CRC sequence instead of to the last character of the message.

If the closing FLAG is received prior to receipt of the appropriate number of A field, C field as programmed in CMR1[5:3], and FCS field octets, a short frame will be detected and RSR[4] will be set. The I field need not be present in a valid frame. An abort (11111110) comparison is done after an opening FLAG has been received and up to receipt of the closing FLAG. A match causes the abort detect status bit (RSR[6]) to be set. The receiver then enters FLAG search mode. The abort is stripped from the received data stream.

If a zero followed by 15 contiguous ones is detected, the idle detect status bit RSR[3] is set. This comparison is done whenever the receiver is enabled. Therefore, it can occur before or after a received frame.

Zero deletion is performed during BOP receive. A zero after 5 contiguous ones is deleted from the data stream regardless of character boundaries. Deleted zeros are not subject to CRC accumulation. FLAG, ABORT, and IDLE comparisons are done prior to zero deletion.

If external synchronization is programmed (RPR[4] - 1), the internal FLAG detection and address comparison logic is disabled and receipt of FLAGs is not required. In this arrangement, a pulse on the SYNI-N input pin will establish synchronization and terminate hunt phase. The receiver will then go immediately into the I-field mode with zero deletion disabled, assembling and transferring characters into the FIFO with the character length specified in RPR[1:)]. The SYNI-N pin is ignored after the first input on the SYNI-N pin is received. The receiver must be disabled and then reenabled to resynchronize or to return to normal operating mode.

This mode must be programmed in conjunction with CMR1[2:0] = 110. Refer to the description of RPR[4] for further details.

BOP Loop Mode

Operation of the receiver in BOP loop protocol mode is similar to operation in other BOP modes, except that only certain frame formats are supported. Several character detection functions that interact with the operation of the transmitter commands are added:

1. When the 'go on-loop' command is invoked, the receiver looks for the receipt of a zero followed by seven ones and then asserts the LCN output.
2. When the 'go off-loop' command is invoked, the receiver looks for the receipt of eight contiguous ones and then negates the LCN output.
3. The TxD output normally echoes the receive input with a two bit time delay. When the 'go active on poll' command is asserted, the receiver looks for an EOP (a zero followed by seven ones) and then switches the TxD output line to the normal transmitter output. Receipt of an EOP or an ABORT sets RSR[6].
4. Receipt of a turnaround sequence (eight contiguous zeros) terminates the transmitter operation, if any, and returns the TxD output to echoing the RxD input. RSR[3] is set if a turnaround is received.

See transmitter operation for additional details.

SUMMARY OF COP FEATURES

COP Dual SYN Mode	
SYN detect	SYN1-SYN2
Linefill	SYN1-SYN2
SYN stripping	SYN1-SYN2 used to establish character sync, i.e., leading SYNs. Subsequent to this (after receiving first non-SYN character), SYN1 and SYN1-SYN2 if stripping is specified by RPR[7].
Excluded form FCS**	SYN1 and SYN1-SYN2 before beginning of message, i.e., leading SYNs and, if SYN stripping is specified by RPR[7] anywhere else in the message for the Rx; linefill SYN1-SYN2 for Tx regardless of RPR[7]. (If SYN stripping is not specified, then SYNs within a message will be included in FCS by Rx.)
BISYNC normal mode	
SYN detect	SYN1-SYN2
Linefill	FYN1-SYN2
SYN stripping	SYN1-SYN2 used to establish character sync, i.e., leading SYNs. Subsequent to this (after receiving first non-SYN character), SYN1 and SYN1-SYN2 if stripping is specified by RPR[7].
Excluded from FCS	All SYNs either before or within a message, regardless of RPR[7], plus additional characters as required by the protocol.
BISYNC transparent mode	
SYN detect	*DLE-SYN1
Linefill	*DLE-SYN1
SYN/DLE stripping	*DLE-SYN1 and odd DLEs if stripping is specified by RPR[7].
Excluded from FCS	*DLE-SYN1 and odd DLEs, regardless of RPR[7] plus additional characters as required by the protocol.
COP single SYN mode	
SYN detect	SYN1
Linefill	SYN1
SYN stripping	SYN1 used to establish character sync, i.e., leading SYNs. Subsequent to this, SYN1 if stripping is specified by RPR[7].
Excluded from FCS**	SYN1 before beginning of message, i.e., leading SYNs, and if SYN stripping is specified by RPR[7], anywhere else in the message for the Rx; linefill SYN1 for Tx regardless of RPR[7]. (If SYN stripping is not specified, then SYNs within a message will be included in FCS by Rx.)

NOTES:

* DLE indicates last DLE of an odd number of consecutive DLEs.

** In non-BISYNC COP modes (single or dual SYN case), if SYN stripping is off, i.e., RPR[7] = 0, then SYNs within a message will be included in FCS by receiver. Therefore, the remote DUSCC transmitter should be careful not to let the TxFIFO underrun since the linefill SYN characters are not accumulated in FCS by the transmitter regardless of RPR[7]. Letting the TxFIFO underrun will result in a CRC error in the receiver.

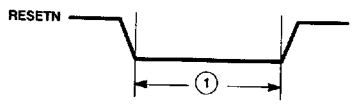


Figure 12. Reset Timing

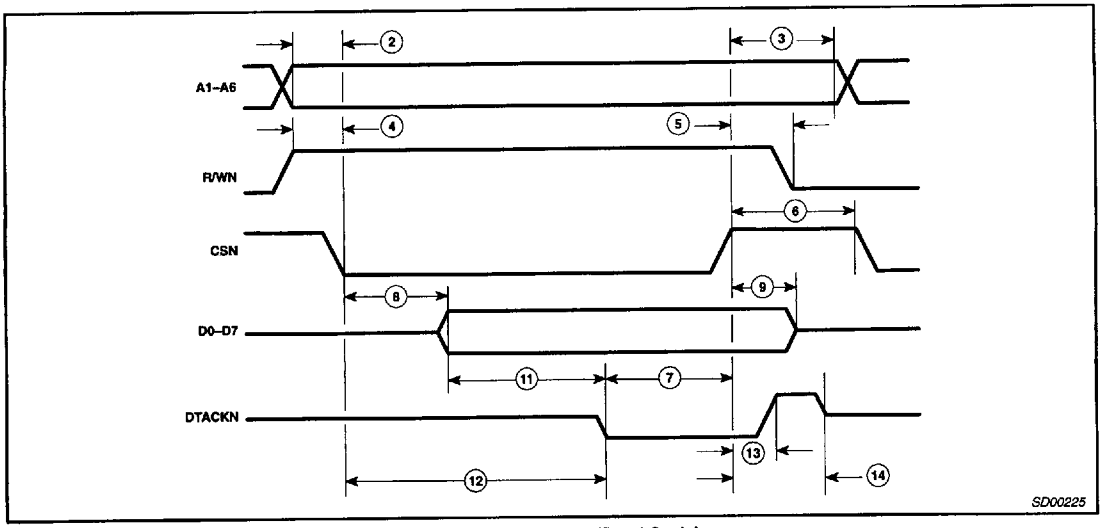


Figure 13. Bus timing (Read Cycle)

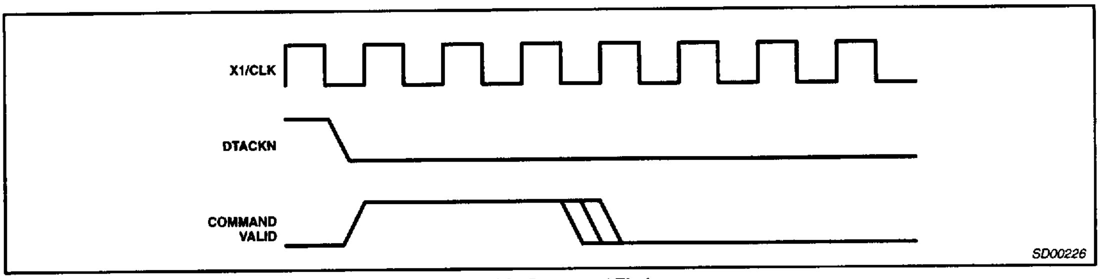


Figure 14. Command Timing

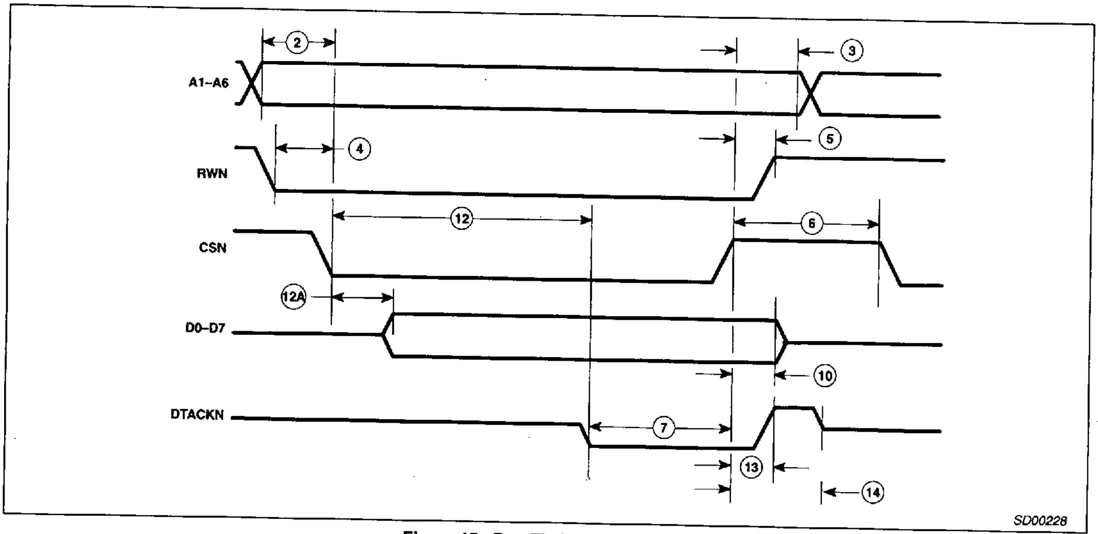


Figure 15. Bus Timing (Write Cycle)

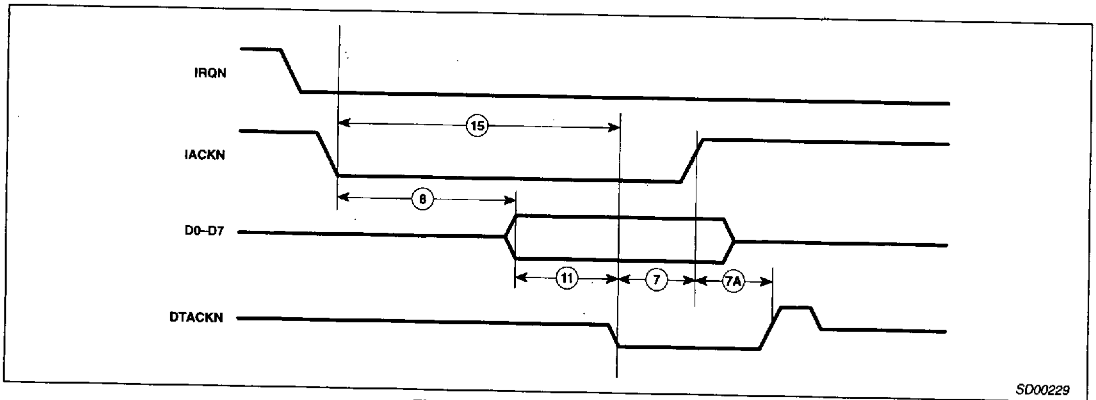


Figure 16. Interrupt Cycle Timing

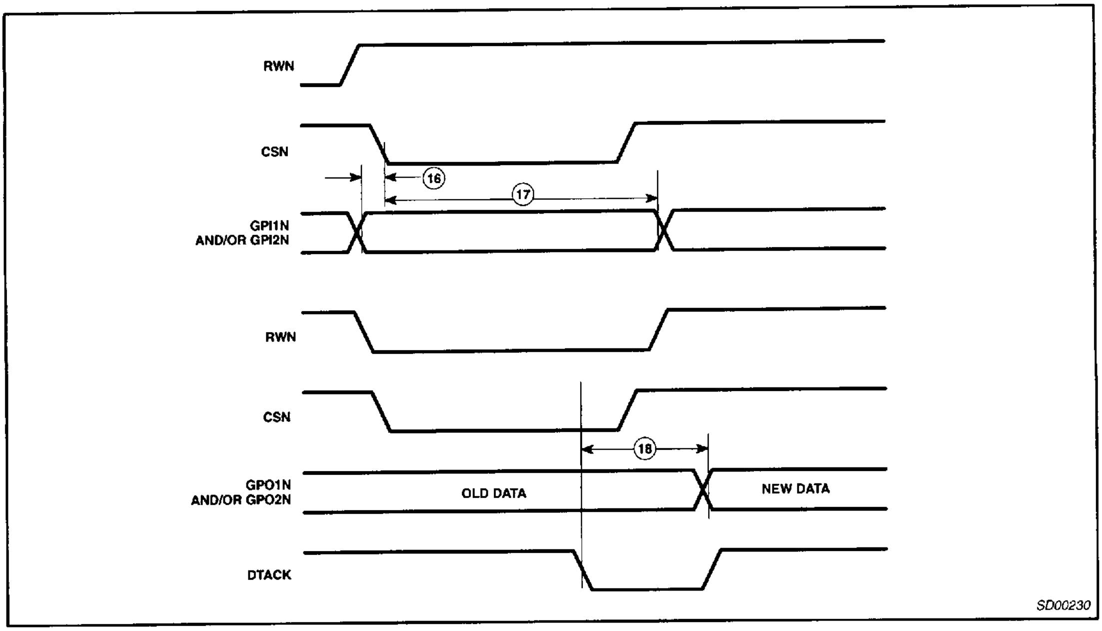


Figure 17. Port Timing

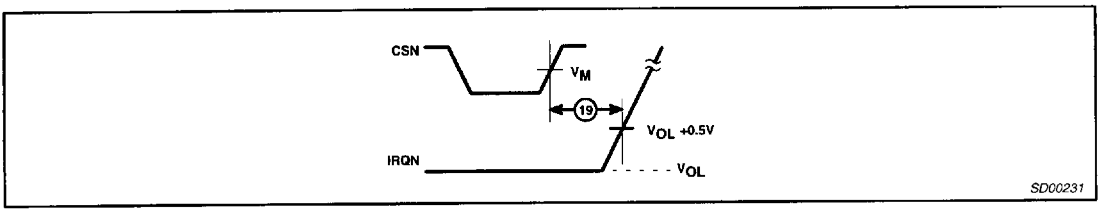


Figure 18. Interrupt Timing

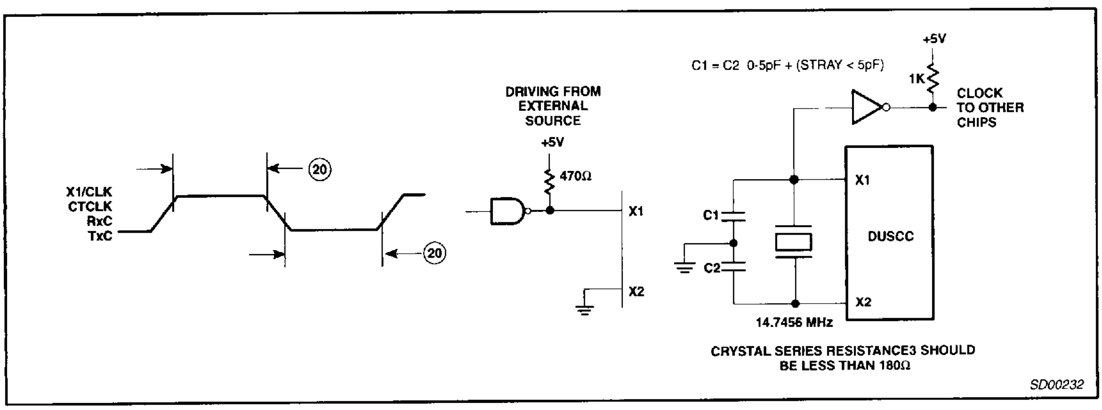


Figure 19. Clock Timing

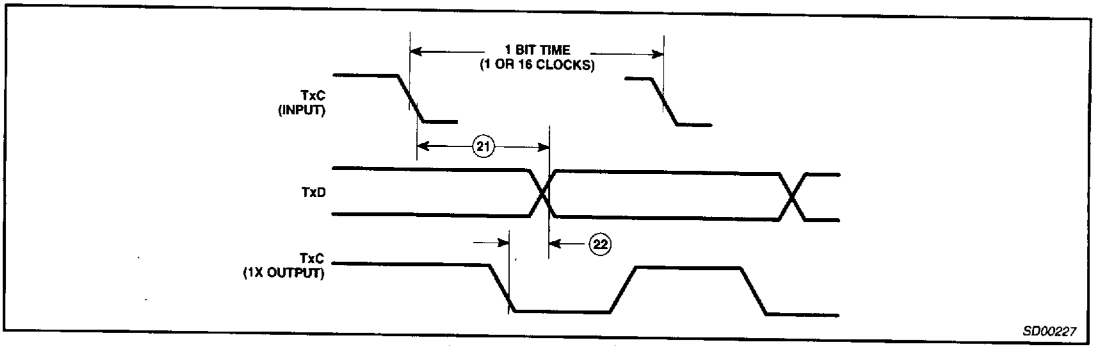


Figure 20. Transmit Timing

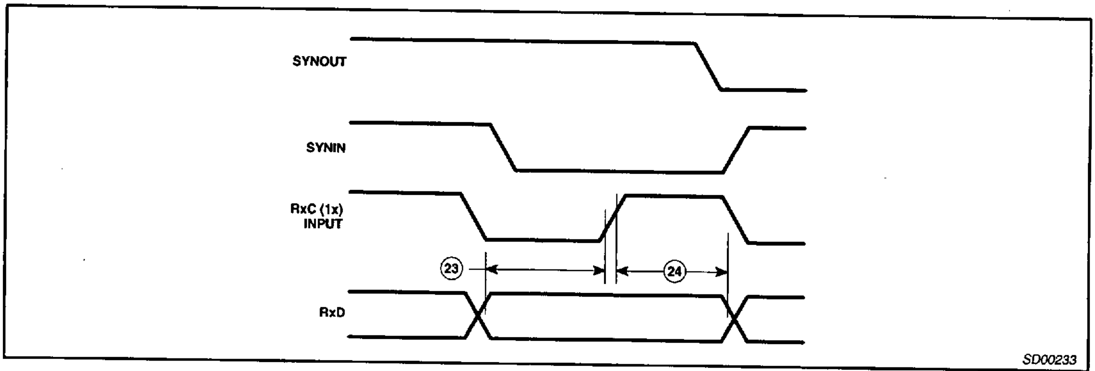


Figure 21. Receive Timing

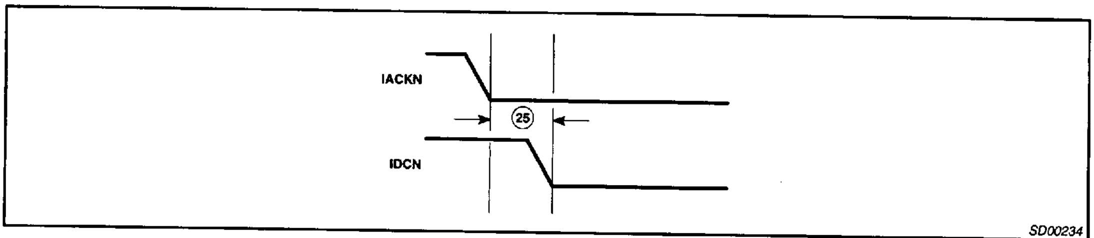


Figure 22. Interrupt Daisy Chain Timing

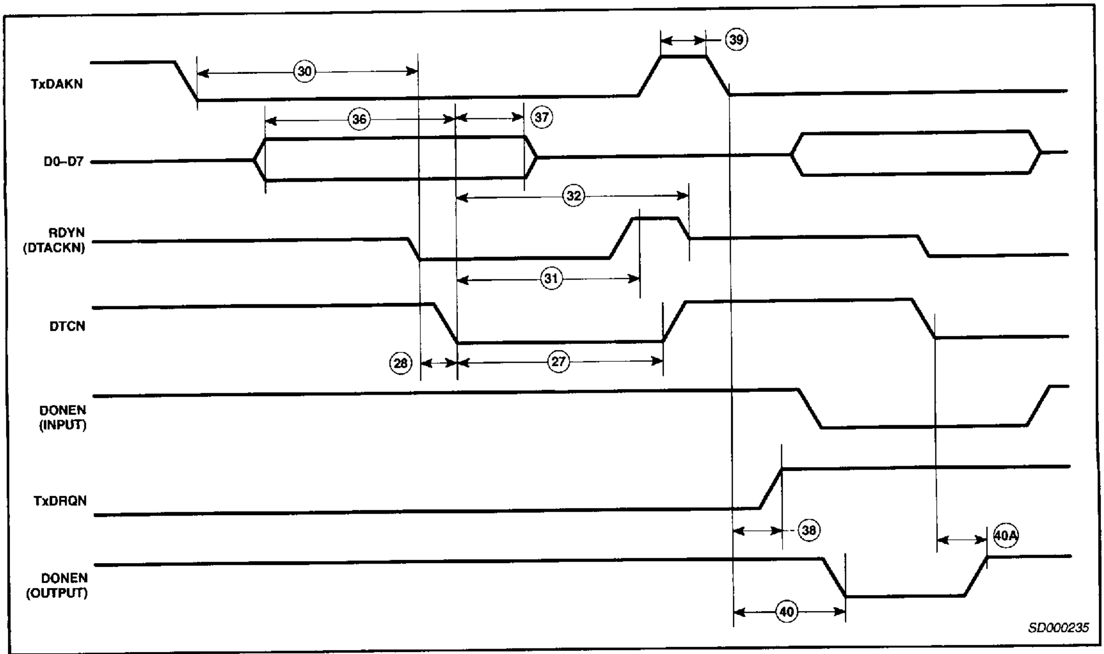


Figure 23. DMA Transmit Write Timing—Single Address DMA Mode

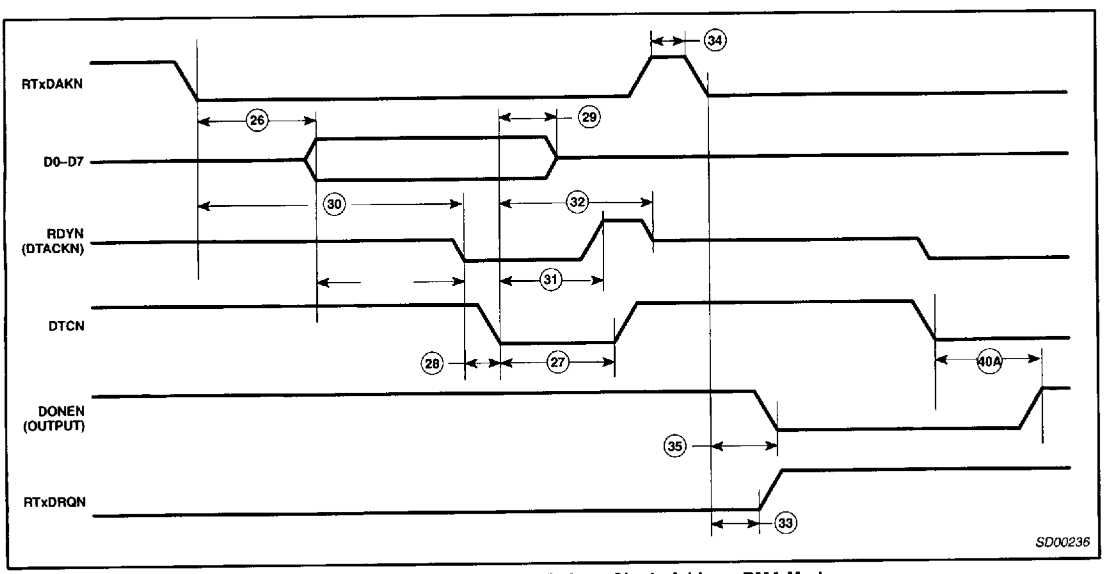


Figure 24. DMA Receiver Read Timing—Single Address DMA Mode

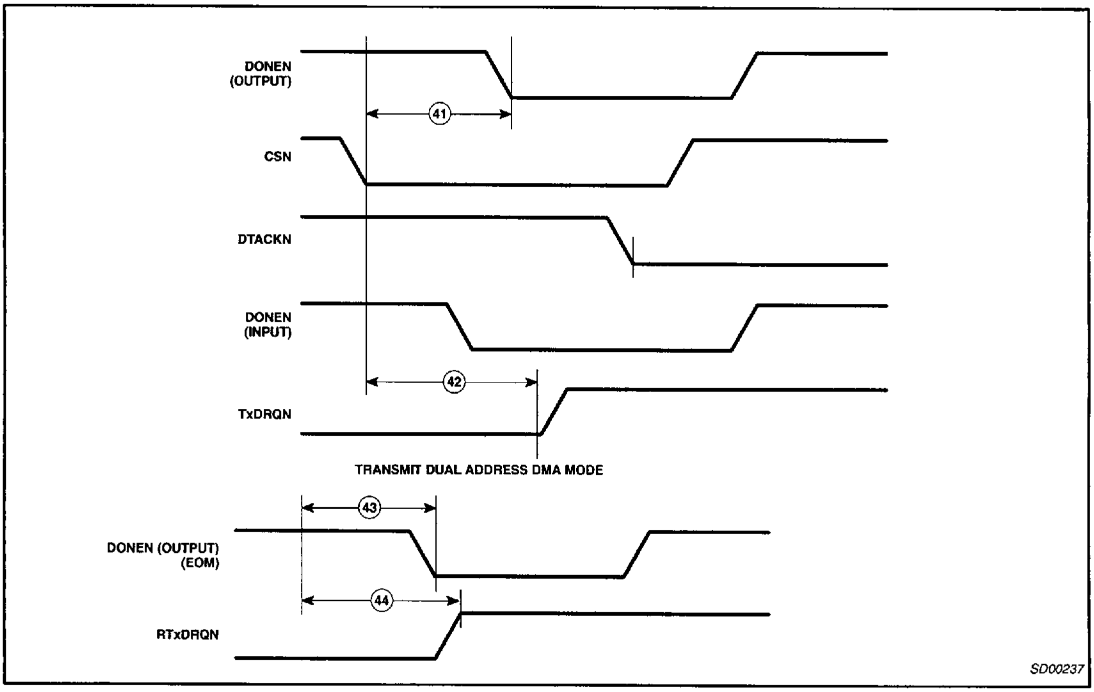


Figure 25. Dual Address DMA Mode Timing