National Semiconductor

December 1995

74ABT162244
16-Bit Buffer/Line Driver with 25Ω Series Resistors in the Outputs

General Description

The 'ABT162244 contains sixteen non-inverting buffers with TRI-STATE® outputs designed to be employed as a memory and address driver, clock driver, or bus oriented transmitter/receiver. The device is nibble controlled. Individual TRI-STATE control inputs can be shorted together for 8-bit or 16-bit operation.

The 25Ω series resistors in the outputs reduce ringing and eliminate the need for external resistors.

Features

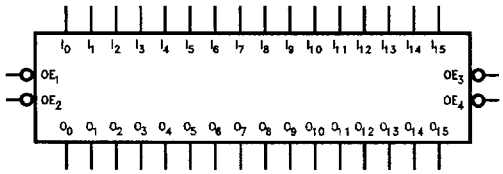
- Separate control logic for each nibble
- 16-bit version of the 'ABT2244
- Guaranteed latch protection
- High impedance glitch free bus loading during entire power up and power down cycle
- Non-destructive hot insertion capability

Commercial	Package Number	Package Description
74ABT162244CSSC (Note 1)	MS48A	48-Lead (0.300" Wide) Molded Shrink Small Outline, JEDEC (SSOP)
74ABT162244CMTD (Notes 1, 2)	MTD48	48-Lead Molded Thin Shrink Small Outline, JEDEC (TSSOP)

Note 1: Devices also available in 13" reel. Use suffix = SSCX and MTDX.

Note 2: Contact factory for package availability

Logic Symbol



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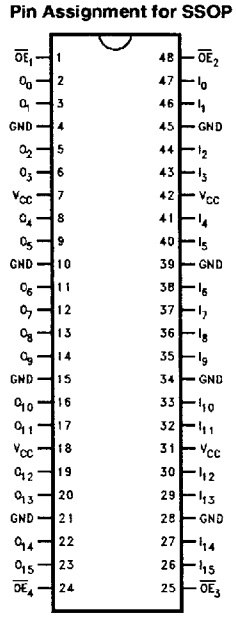
Pin Description

Pin Names	Description
$\overline{OE}_n$	Output Enable Input (Active Low)
I_0–I_{15}	Inputs
O_0–O_{15}	Outputs

Connection Diagram

Pin Assignment for SSOP



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RRD-B30M125/Printed in U. S. A.

Functional Description

The 'ABT162244 contains sixteen non-inverting buffers with TRI-STATE outputs. The device is nibble (4 bits) controlled with each nibble functioning identically, but independent of the other. The control pins can be shorted together to obtain full 16-bit operation.

Truth Tables

Inputs		Outputs
$\overline{OE}_1$	I_0–I_3	O_0–O_3
L	L	L
L	H	H
H	X	Z

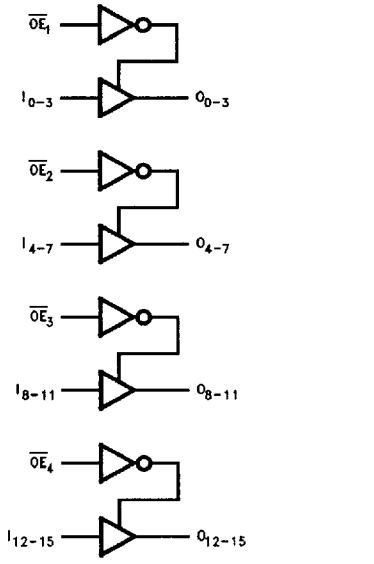
Inputs		Outputs
$\overline{OE}_2$	I_4–I_7	O_4–O_7
L	L	L
L	H	H
H	X	Z

Inputs		Outputs
$\overline{OE}_3$	I_8–I_{11}	O_8–O_{11}
L	L	L
L	H	H
H	X	Z

Inputs		Outputs
$\overline{OE}_4$	I_{12}–I_{15}	O_{12}–O_{15}
L	L	L
L	H	H
H	X	Z

H = High Voltage Level
L = Low Voltage Level
X = Immaterial
Z = High Impedance

Logic Diagrams



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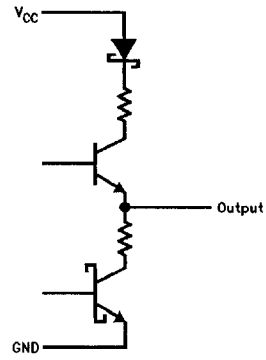
Schematic of each Output



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Absolute Maximum Ratings (Note 1)

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	
Plastic	−55°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Any Output	
in the Disabled or Power-off State	−0.5V to 5.5V
in the HIGH State	−0.5V to V_{CC}
Current Applied to Output in LOW State (Max)	twice the rated I_{OL} (mA)
DC Latchup Source Current	−500 mA
Over Voltage Latchup (I/O)	10V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs

Recommended Operating Conditions

Free Air Ambient Temperature	
Commercial	−40°C to +85°C
Supply Voltage	
Commercial	+4.5V to +5.5V
Minimum Input Edge Rate ($\Delta V/\Delta t$)	
Data Input	50 mV/ns
Enable Input	20 mV/ns

DC Electrical Characteristics

Symbol	Parameter		ABT162244 Min	Typ	Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		Recognized HIGH Signal
V_{IL}	Input LOW Voltage				0.8	V		Recognized LOW Signal
V_{CD}	Input Clamp Diode Voltage				−1.2	V	Min	I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	74ABT	2.5			V	Min	I_{OH} = −3 mA
		74ABT	2.0			V	Min	I_{OH} = −32 mA
V_{OL}	Output LOW Voltage	74ABT			0.8	V	Min	I_{OL} = 12 mA
I_{IH}	Input HIGH Current				5 5	μA	Max	V_{IN} = 2.7V (Note 1) V_{IN} = V_{CC}
I_{BVI}	Input HIGH Current Breakdown Test				7	μA	Max	V_{IN} = 7.0V
I_{IL}	Input LOW Current				−5 −5	μA	Max	V_{IN} = 0.5V (Note 1) V_{IN} = 0.0V
V_{ID}	Input Leakage Test		4.75			V	0.0	I_{ID} = 1.9 μA All Other Pins Grounded
I_{OZH}	Output Leakage Current				50	μA	0 − 5.5V	V_{OUT} = 2.7V; $\overline{OE}_n$ = 2.0V
I_{OZL}	Output Leakage Current				−50	μA	0 − 5.5V	V_{OUT} = 0.5V; $\overline{OE}_n$ = 2.0V
I_{OS}	Output Short-Circuit Current		−100		−275	mA	Max	V_{OUT} = 0.0V
I_{CEX}	Output High Leakage Current				50	μA	Max	V_{OUT} = V_{CC}
I_{ZZ}	Bus Drainage Test				100	μA	0.0	V_{OUT} = 5.5V; All Others GND
I_{CCH}	Power Supply Current				2.0	mA	Max	All Outputs HIGH
I_{CCL}	Power Supply Current				60	mA	Max	All Outputs LOW
I_{CCZ}	Power Supply Current				2.0	mA	Max	$\overline{OE}_n$ = V_{CC} All Others at V_{CC} or GND
I_{CCT}	Additional I_{CC}/Input	Outputs Enabled			3.0	mA	Max	V_I = V_{CC} − 2.1V Enable Input V_I = V_{CC} − 2.1V Data Input V_I = V_{CC} − 2.1V All Others at V_{CC} or GND
		Outputs TRI-STATE			3.0	mA		
		Outputs TRI-STATE			50	μA		
I_{CCD}	Dynamic I_{CC} (Note 1)	No Load			0.1	mA/MHz	Max	Outputs Open $\overline{OE}_n$ = GND One Bit Toggling, 50% Duty Cycle

Note 1: Guaranteed, but not tested

AC Electrical Characteristics

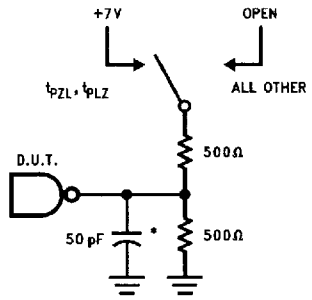
Symbol	Parameter	74ABT $T_A = +25°C$, $V_{CC} = +5V$, $C_L = 50$ pF			74ABT $T_A = -40°C$ to $+85°C$, $V_{CC} = 4.5V-5.5V$, $C_L = 50$ pF		Units
		Min	Typ	Max	Min	Max	
t_{PLH}	Propagation Delay Data to Outputs	1.0	2.4	3.9	1.0	3.9	ns
t_{PHL}		1.0	3.2	4.7	1.0	4.7	
t_{PZH}	Output Enable Time	1.5	3.5	6.3	1.5	6.3	ns
t_{PZL}		1.5	4.2	6.9	1.5	6.9	
t_{PHZ}	Output Disable Time	1.0	4.2	6.7	1.0	6.7	ns
t_{PLZ}		1.0	3.8	6.7	1.0	6.7	

Capacitance

Symbol	Parameter	Typ	Units	Conditions, $T_A = 25°C$
C_{IN}	Input Capacitance	5.0	pF	$V_{CC} = 0.0V$
C_{OUT}(Note 1)	Output Capacitance	9.0	pF	$V_{CC} = 5.0V$

Note 1: C_{OUT} is measured at frequency f = 1 MHz per MIL-STD-883B, Method 3012

AC Loading



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*Includes jig and probe capacitance

FIGURE 1. Standard AC Test Load

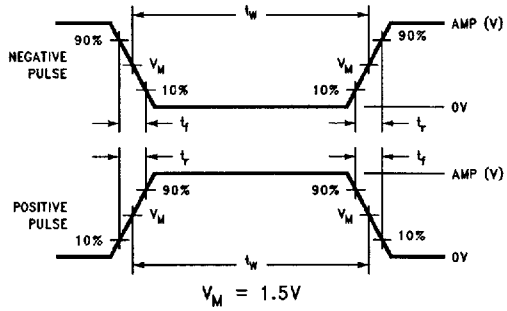

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FIGURE 2a. Input Pulse Requirements

Amplitude	Rep. Rate	t_w	t_r	t_f
3.0V	1 MHz	500 ns	2.5 ns	2.5 ns

FIGURE 2b. Test Input Signal Requirements

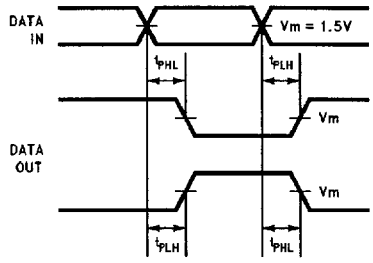

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FIGURE 3. Propagation Delay Waveforms for Inverting and Non-Inverting Functions

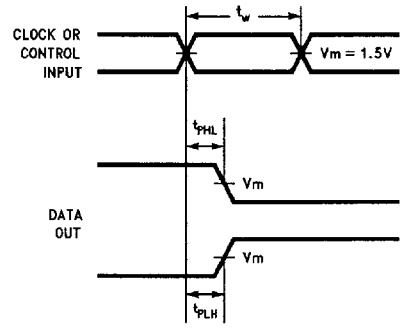

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FIGURE 4. Propagation Delay, Pulse Width Waveforms

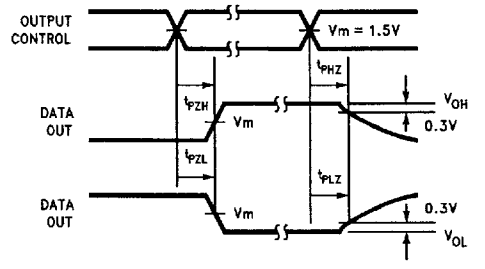

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FIGURE 5. TRI-STATE Output HIGH and LOW Enable and Disable Times

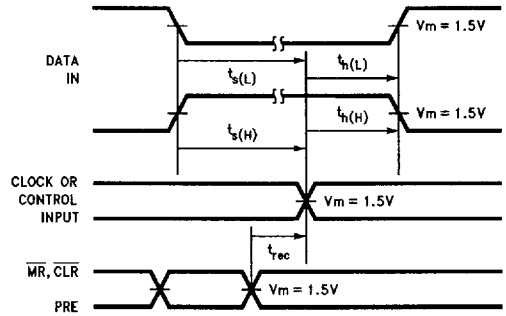

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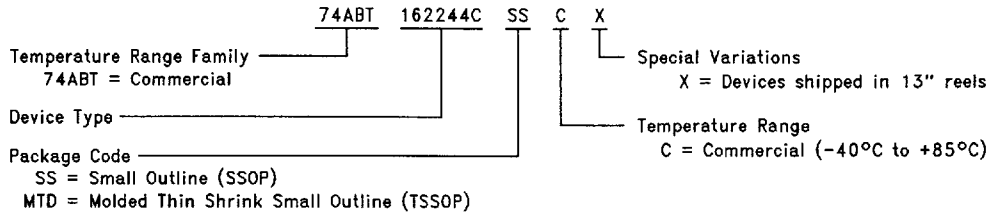
FIGURE 6. Setup Time, Hold Time and Recovery Time Waveforms

Ordering Information

The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:



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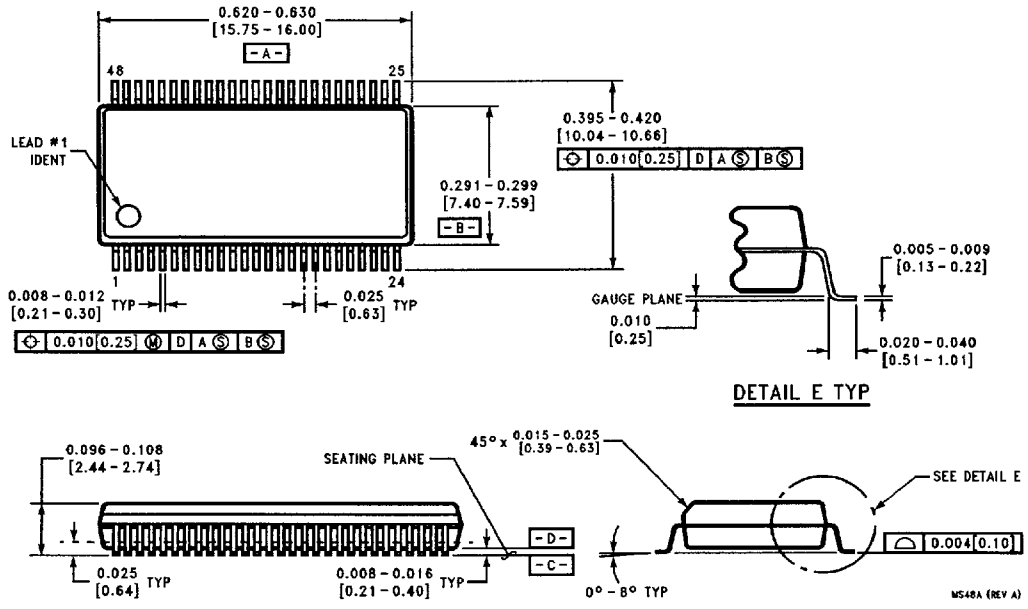
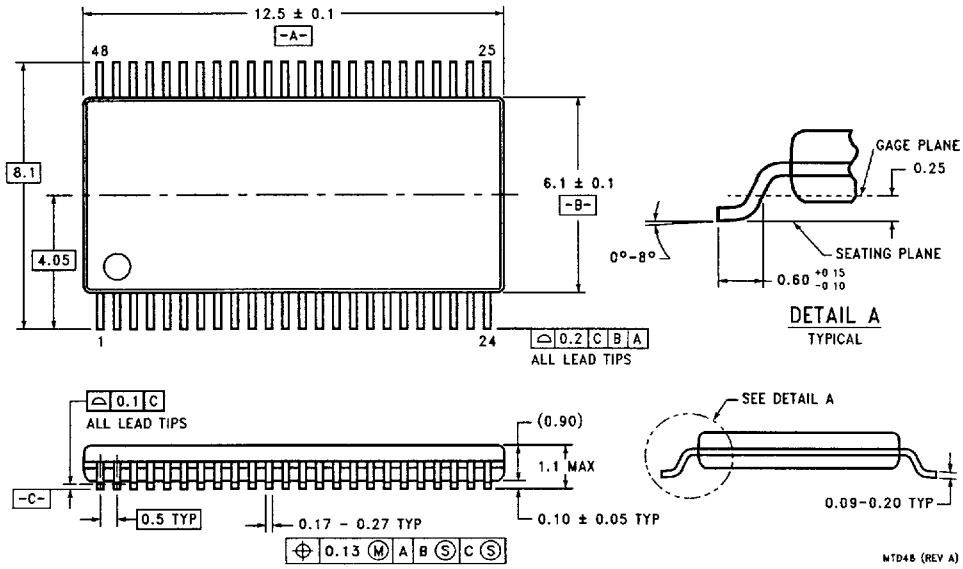
Physical Dimensions inches (millimeters)



48-Lead SSOP (0.300" Wide) (SS)
NS Package Number MS48A

Physical Dimensions millimeters (Continued)



48-Lead Molded Thin Shrink Small Outline Package, JEDEC
NS Package Number MTD48

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National Semiconductor Corporation
1111 West Bardin Road
Arlington, TX 76017
Tel. 1(800) 272-9959
Fax 1(800) 737-7018

National Semiconductor Europe
Fax (+49) 0-180-530 85 86
Email cnjwge@tevm2.nsc.com
Deutsch Tel (+49) 0-180-530 85 85
English Tel (+49) 0-180-532 78 32
Français Tel (+49) 0-180-532 93 58
Italiano Tel (+49) 0-180-534 16 80

National Semiconductor Hong Kong Ltd.
13th Floor, Straight Block,
Ocean Centre, 5 Canton Rd
Tsimshatsui, Kowloon
Hong Kong
Tel (852) 2737-1600
Fax (852) 2736-9960

National Semiconductor Japan Ltd.
Tel 81-043-299-2309
Fax 81-043 299-2408