Octal transceiver with parity generator/checker (3-State)

74ABT657

FEATURES

- Combinational functions in one package
- Low static and dynamic power dissipation with high speed and high output drive
- Output capability: +64mA/–32mA
- Power-up 3-State
- Latch-up protection exceeds 500mA per Jedec Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model

DESCRIPTION

The 74ABT657 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT657 is an octal transceiver featuring non-inverting buffers with 3-State outputs and an 8-bit parity generator/checker, and is intended for bus-oriented applications. The buffers have a guaranteed current sinking capability of 64mA. The Transmit/Receive (T/$\overline{R}$) input determines the direction of the data flow through the bidirectional transceivers. Transmit (active-High) enables data from A ports to B ports; Receive (active-Low) enables data from B ports to A ports.

The Output Enable ($\overline{OE}$) input disables both the A and B ports by placing them in a high impedance condition when the $\overline{OE}$ input is High. The parity select (ODD/$\overline{EVEN}$) input gives the user the option of odd or even parity systems. The parity (PARITY) pin is an output from the generator/checker when transmitting from the port A to B (T/$\overline{R}$ = High) and an input when receiving from port B to A port (T/$\overline{R}$ = Low). When transmitting (T/$\overline{R}$ = High) the parity select (ODD/$\overline{EVEN}$) input is set, then the A port data is polled to determine the number of High bits. The parity (PARITY) output then goes to the logic state determined by the parity select (ODD/$\overline{EVEN}$) setting and by the number of High bits on port A. For example, if the parity select (ODD/$\overline{EVEN}$) is set Low (even parity), and the number of High bits on port A is odd, then the parity (PARITY) output will be High, transmitting even parity. If the number of High bits on port A is even, then the parity (PARITY) output will be Low, keeping even parity. When in receive mode (T/$\overline{R}$ = Low) the B port is polled to determine the number of High bits. If parity select (ODD/$\overline{EVEN}$) is Low (even parity) and the number of Highs on port B is:

(1) odd and the parity (PARITY) input is High, then $\overline{ERROR}$ will be High, signifying no error.

(2) even and the parity (PARITY) input is High, then $\overline{ERROR}$ will be asserted Low, indicating an error.

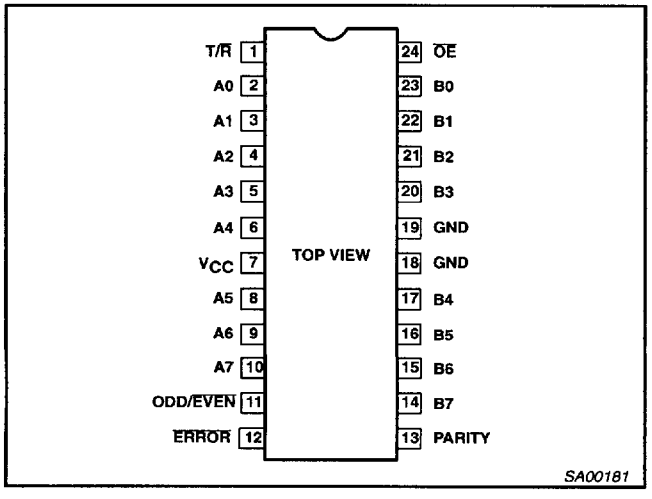
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T_{amb} = 25°C; GND = 0V	TYPICAL	UNIT
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	C_L = 50pF; V_{CC} = 5V	3.3	ns
C_{IN}	Input capacitance	V_I = 0V or V_{CC}	4	pF
$C_{I/O}$	I/O capacitance	Outputs disabled; V_O = 0V or V_{CC}	7	pF
I_{CCZ}	Total supply current	Outputs disabled; V_{CC} =5.5V	500	nA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
24-Pin Plastic DIP	–40°C to +85°C	74ABT657 N	74ABT657 N	SOT222-1
24-Pin plastic SO	–40°C to +85°C	74ABT657 D	74ABT657 D	SOT137-1
24-Pin Plastic SSOP Type II	–40°C to +85°C	74ABT657 DB	74ABT657 DB	SOT340-1
24-Pin Plastic TSSOP Type I	–40°C to +85°C	74ABT657 PW	74ABT657PW DH	SOT355-1

PIN CONFIGURATION



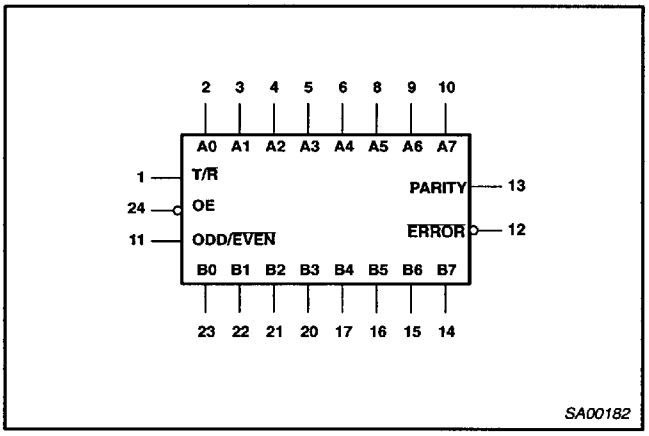
PIN DESCRIPTION

SYMBOL	PIN NUMBER	NAME AND FUNCTION
13	PARITY	Parity output
11	ODD/$\overline{EVEN}$	Parity select input
12	$\overline{ERROR}$	Error output
1	T/$\overline{R}$	Transmit/receive input
2, 3, 4, 5, 6, 8, 9, 10	A0 - A7	A port 3-State outputs
23, 22, 21, 20, 17, 16, 15, 14	B0 - B7	B port 3-State outputs
24	$\overline{OE}$	Output enable input (active-Low)
18, 19	GND	Ground (0V)
7	V_{CC}	Positive supply voltage

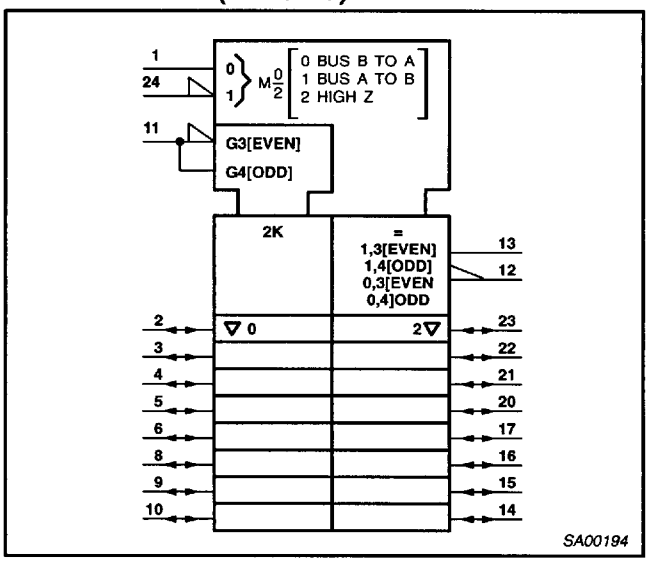
Octal transceiver with parity generator/checker (3-State)

74ABT657

LOGIC SYMBOL



LOGIC SYMBOL (IEEE/IEC)

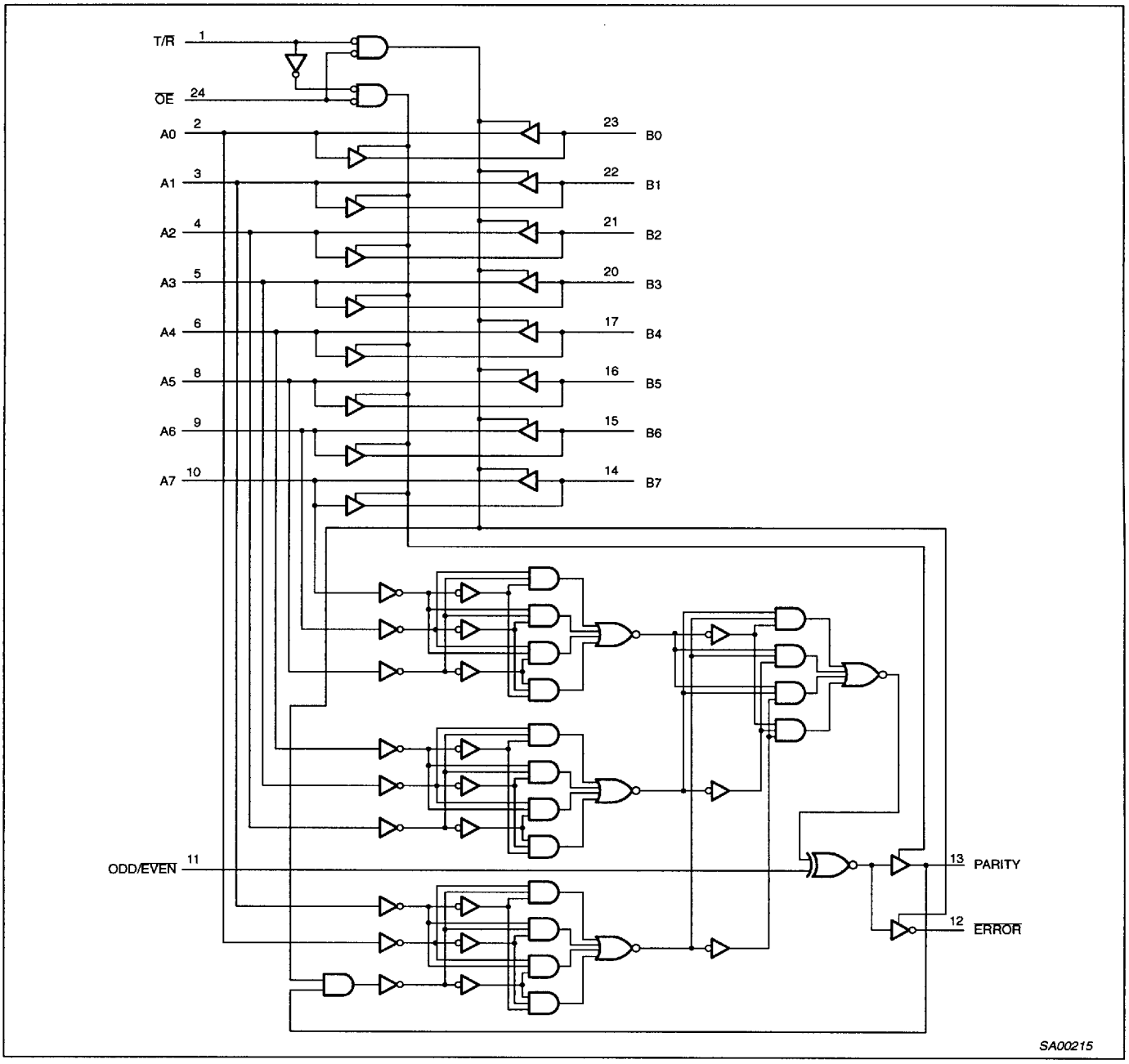


FUNCTION TABLE

NUMBER OF HIGH INPUTS	INPUTS			INPUT/ OUTPUT	OUTPUTS	
	$\overline{OE}$	T/$\overline{R}$	ODD/$\overline{EVEN}$	PARITY	$\overline{ERROR}$	OUTPUTS MODE
0, 2, 4, 6, 8	L	H	H	H	Z	Transmit
	L	H	L	L	Z	Transmit
	L	L	H	H	H	Receive
	L	L	H	L	L	Receive
	L	L	L	H	L	Receive
	L	L	L	L	H	Receive
1, 3, 5, 7	L	H	H	L	Z	Transmit
	L	H	L	H	Z	Transmit
	L	L	H	H	L	Receive
	L	L	H	L	H	Receive
	L	L	L	H	H	Receive
	L	L	L	L	L	Receive
Don't care	H	X	X	Z	Z	3-State

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1, 2]

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		–0.5 to +7.0	V
I_{IK}	DC input diode current	$V_I < 0$	–18	mA
V_I	DC input voltage[3]		–1.2 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	–50	mA
V_{OUT}	DC output voltage[3]	output in Off or High state	–0.5 to +5.5	V
I_{OUT}	DC output current	output in Low state	128	mA
T_{stg}	Storage temperature range		–65 to 150	°C

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V_{CC}	DC supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2.0		V
V_{IL}	Low-level input voltage		0.8	V
I_{OH}	High-level output current		–32	mA
I_{OL}	Low-level output current		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0	5	ns/V
T_{amb}	Operating free-air temperature range	–40	+85	°C

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITIONS	LIMITS					UNIT
				T_{amb} = +25°C			T_{amb} = –40°C to +85°C		
				Min	Typ	Max	Min	Max	
V_{IK}	Input clamp voltage		V_{CC} = 4.5V; I_{IK} = –18mA		–0.9	–1.2		–1.2	V
V_{OH}	High-level output voltage		V_{CC} = 4.5V; I_{OH} = –3mA; V_I = V_{IL} or V_{IH}	2.5	3.5		2.5		V
			V_{CC} = 5.0V; I_{OH} = –3mA; V_I = V_{IL} or V_{IH}	3.0	4.0		3.0		V
			V_{CC} = 4.5V; I_{OH} = –32mA; V_I = V_{IL} or V_{IH}	2.0	2.6		2.0		V
V_{OL}	Low-level output voltage		V_{CC} = 4.5V; I_{OL} = 64mA; V_I = V_{IL} or V_{IH}		0.42	0.55		0.55	V
I_I	Input leakage current	Control pins	V_{CC} = 5.5V; V_I = GND or 5.5V		±0.01	±1.0		±1.0	µA
		Data pins	V_{CC} = 5.5V; V_I = GND or 5.5V		±5	±100		±100	µA
I_{OFF}	Power-off leakage current		V_{CC} 0.0V; V_O or $V_I \leq$ 4.5V		±5.0	±100		±100	µA
I_{PU}/I_{PD}	Power-up/down 3-State output current[3]		V_{CC} 2.0V; V_O = 0.5V; V_I = GND or V_{CC}; V_{OE} = V_{CC}		±5.0	±50		±50	µA
$I_{IH} + I_{OZH}$	3-State output High current		V_{CC} = 5.5V; V_O = 2.7V; V_I = V_{IL} or V_{IH}		5.0	50		50	µA
$I_{IL} + I_{OZL}$	3-State output Low current		V_{CC} = 5.5V; V_O = 0.5V; V_I = V_{IL} or V_{IH}		–5.0	–50		–50	µA
I_{CEX}	Output High leakage current		V_{CC} = 5.5V; V_O = 5.5V; V_I = GND or V_{CC}		5.0	50		50	µA
I_O	Output current[1]		V_{CC} = 5.5V; V_O = 2.5V	–50	–80	–180	–50	–180	mA
I_{CCH}	Quiescent supply current		V_{CC} = 5.5V; Outputs High, V_I = GND or V_{CC}		0.5	250		250	µA
I_{CCL}			V_{CC} = 5.5V; Outputs Low, V_I = GND or V_{CC}		20	30		30	mA
I_{CCZ}			V_{CC} = 5.5V; Outputs 3-State; V_I = GND or V_{CC}		0.5	250		250	µA
ΔI_{CC}	Additional supply current per input pin[2]		Outputs enabled, one data input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.5	1.5		1.5	mA
			Outputs 3-State, one data input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		50	250		250	µA
			Outputs 3-State, one enable input at 3.4V, other inputs at V_{CC} or GND; V_{CC} = 5.5V		0.5	1.5		1.5	mA

NOTES:
1. Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
2. This is the increase in supply current for each input at 3.4V.
3. This parameter is valid for any V_{CC} between 0V and 2.1V with a transition time of up to 10msec. For V_{CC} = 2.1V to V_{CC} = 5V ± 10%, a transition time of up to 100µsec is permitted.

AC CHARACTERISTICS

GND = 0V; $t_R = t_F = 2.5ns$; $C_L = 50pF$, $R_L = 500\Omega$

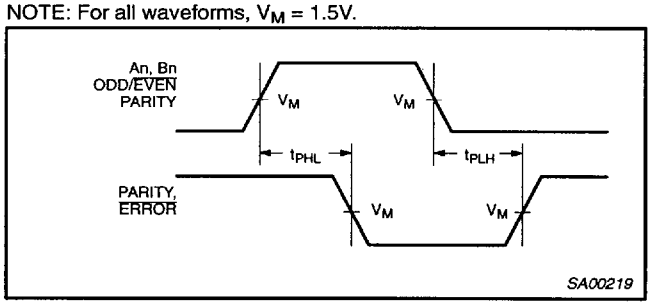
SYMBOL	PARAMETER	WAVEFORMS	LIMITS					UNIT
			T_{amb} = +25°C, V_{CC} = +5.0V			T_{amb} = −40 to +85°C, V_{CC} = +5.0V ±10%		
			Min	Typ	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay An to Bn or Bn to An	2	1.1 1.2	3.3 3.0	5.0 4.3	1.1 1.2	5.5 4.8	ns
t_{PLH} t_{PHL}	Propagation delay An to PARITY	1, 2	2.5 2.8	6.5 7.0	8.7 9.1	2.5 2.8	10.1 10.6	ns
t_{PLH} t_{PHL}	Propagation delay ODD/$\overline{EVEN}$ to PARITY, $\overline{ERROR}$	1, 2	1.7 1.9	5.0 5.0	6.6 6.6	1.7 1.9	7.3 7.3	ns
t_{PLH} t_{PHL}	Propagation delay Bn to $\overline{ERROR}$	1, 2	3.9 4.0	9.2 9.6	11.7 12.1	3.9 4.0	13.8 14.5	ns
t_{PLH} t_{PHL}	Propagation delay PARITY to $\overline{ERROR}$	1, 2	2.7 3.2	6.0 6.4	7.6 8.0	2.7 3.2	9.4 9.4	ns
t_{PZH} t_{PZL}	Output enable time[1] to High or Low level	3, 4	1.3 1.9	3.8 4.4	5.6 7.0	1.3 1.9	6.6 8.2	ns
t_{PHZ} t_{PLZ}	Output disable time from High or Low level	3, 4	2.4 2.7	5.1 5.4	7.0 7.6	2.4 2.7	7.6 8.1	ns

NOTES:

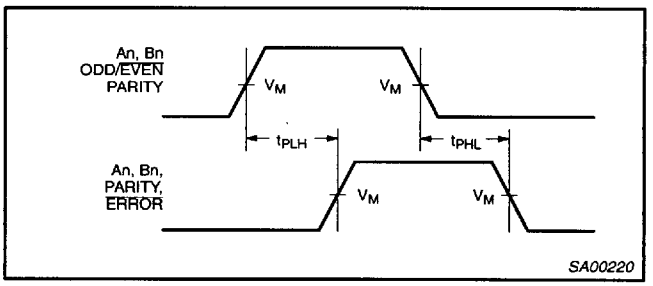
1. These delay times reflect the 3-State recovery time only and do not include the delay through the buffers and the parity check circuitry which affect the $\overline{ERROR}$ output. To assure *valid* information at the $\overline{ERROR}$ pin, time must be allowed for the signal to propagate through the drivers (B to A), through the parity check circuitry (same as A to PARITY), and to the $\overline{ERROR}$ output. *Valid* data at the $\overline{ERROR}$ pin ≥ (B to A) + (A to PARITY).

AC WAVEFORMS

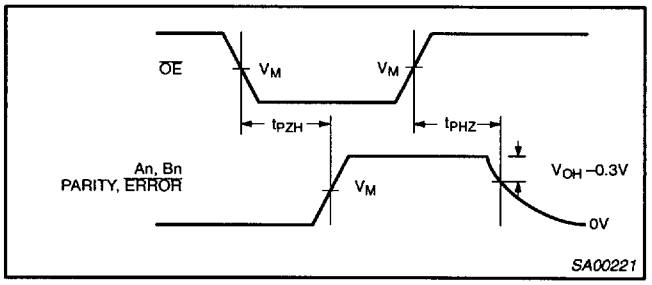
NOTE: For all waveforms, $V_M = 1.5V$.



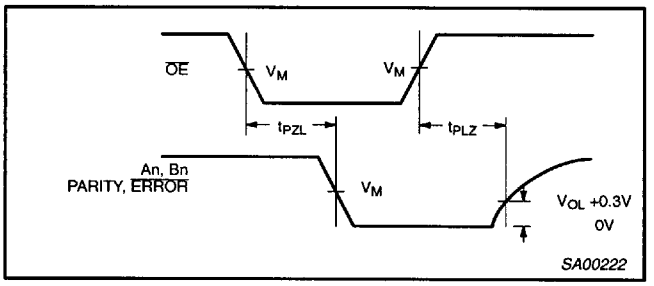
Waveform 1. Propagation Delay For Inverting Output



Waveform 2. Propagation Delay For Non-Inverting Output

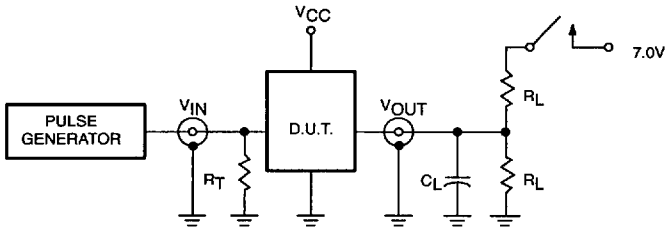


Waveform 3. 3-State Output Enable Time to High Level and Output Disable Time from High Level

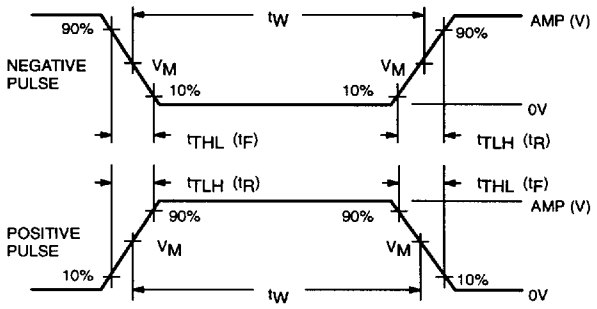


Waveform 4. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

TEST CIRCUIT AND WAVEFORM



Test Circuit for 3-State Outputs



V_M = 1.5V

Input Pulse Definition

SWITCH POSITION

TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

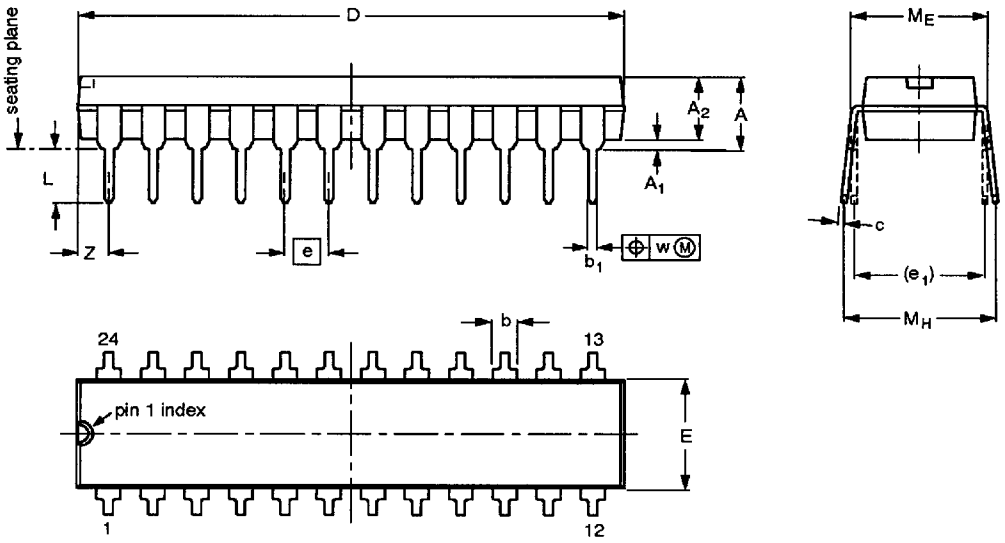
C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

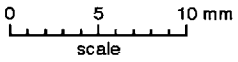
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ABT	3.0V	1MHz	500ns	2.5ns	2.5ns

SA00012

DIP24: plastic dual in-line package; 24 leads (300 mil) SOT222-1





DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

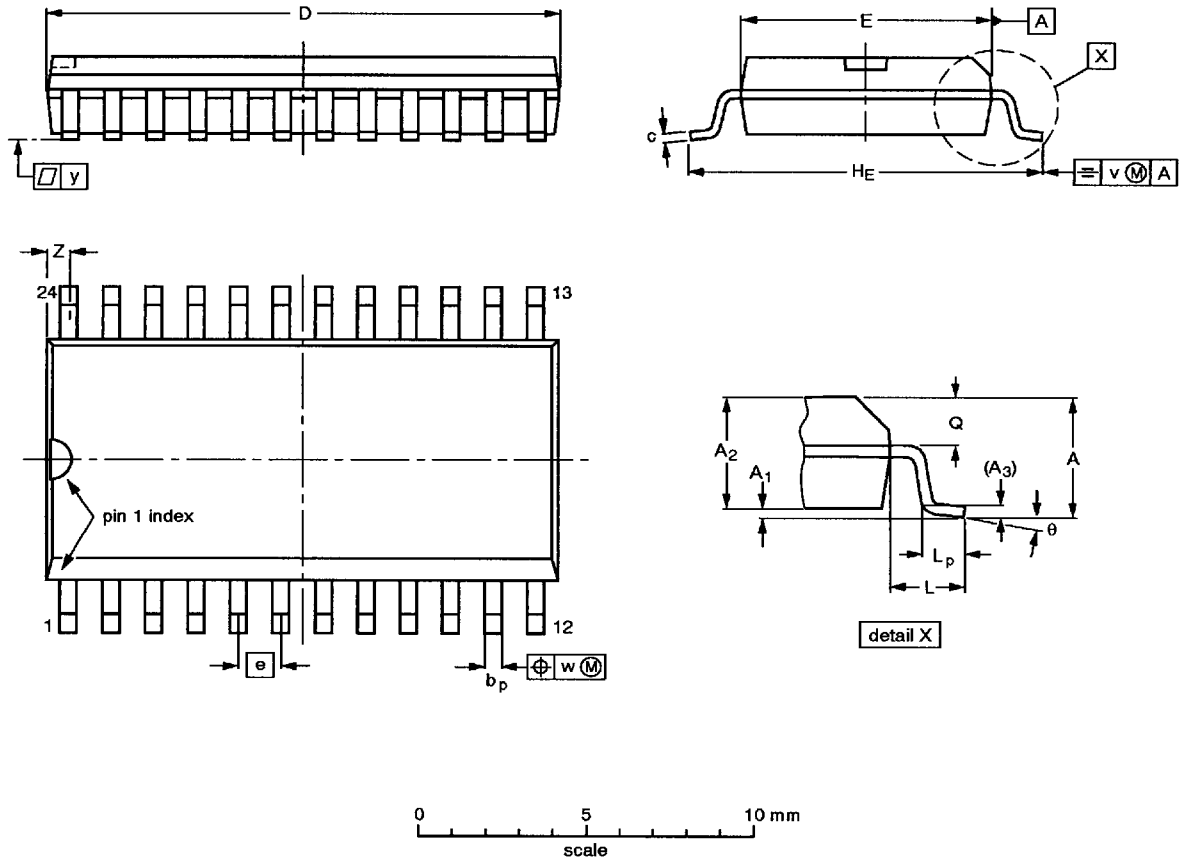
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	$D^{(1)}$	$E^{(1)}$	e	e_1	L	M_E	M_H	w	$Z^{(1)}$ max.
mm	4.70	0.38	3.94	1.63 1.14	0.56 0.43	0.36 0.25	31.9 31.5	6.73 6.48	2.54	7.62	3.51 3.05	8.13 7.62	10.03 7.62	0.25	2.05
inches	0.185	0.015	0.155	0.064 0.045	0.022 0.017	0.014 0.010	1.256 1.240	0.265 0.255	0.100	0.300	0.138 0.120	0.32 0.30	0.395 0.300	0.01	0.081

Note

1. Plastic or metal protrusions of 0.01 inches maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT222-1		MS-001AF				95-03-11

SO24: plastic small outline package; 24 leads; body width 7.5 mm — SOT137-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

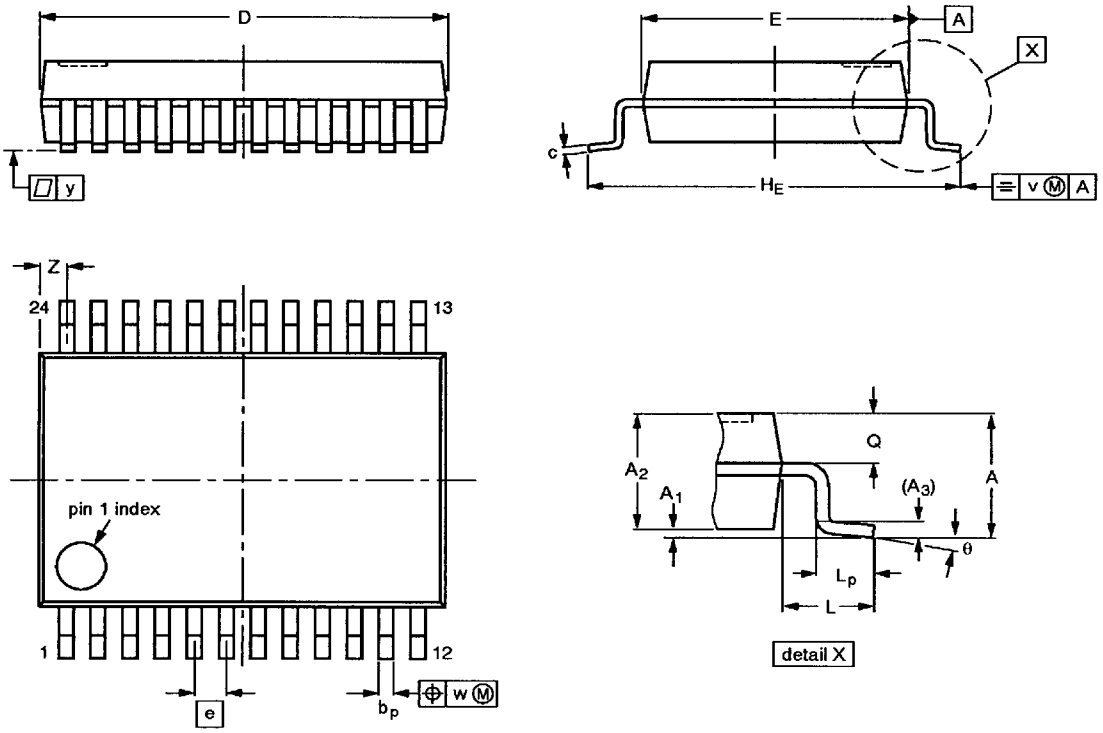
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	15.6 15.2	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.61 0.60	0.30 0.29	0.050	0.42 0.39	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

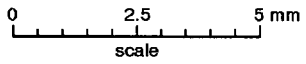
Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT137-1	075E05	MS-013AD				~~92-11-17~~ 95-01-24

SSOP24: plastic shrink small outline package; 24 leads; body width 5.3 mm **SOT340-1**





DIMENSIONS (mm are the original dimensions)

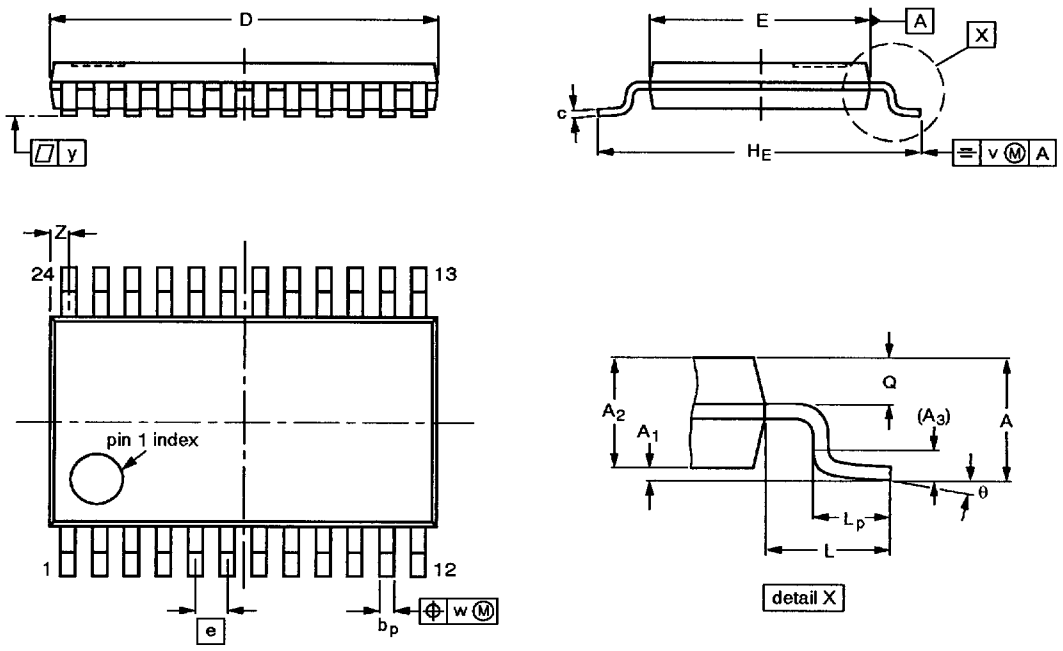
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	8.4 8.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.8 0.4	8° 0°

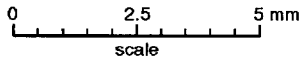
Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT340-1		MO-150AG				~~93-09-08~~ 95-02-04

TSSOP24: plastic thin shrink small outline package; 24 leads; body width 4.4 mm **SOT355-1**





DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	7.9 7.7	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT355-1		MO-153AD				~~93-06-16~~ 95-02-04