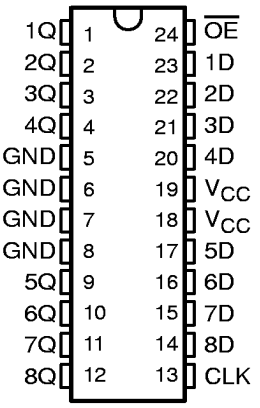
74AC11374
OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOP WITH 3-STATE OUTPUTS

SCAS214A – JULY 1987 – REVISED APRIL 1996

- **Eight D-Type Flip-Flops in a Single Package**
- **3-State Bus-Driving True Outputs**
- **Full Parallel Access for Loading**
- **Flow-Through Architecture Optimizes PCB Layout**
- **Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise**
- ***EPIC*™ (Enhanced-Performance Implanted CMOS) 1-μm Process**
- **500-mA Typical Latch-Up Immunity at 125°C**
- **Package Options Include Plastic Small-Outline (DW) and Shrink Small-Outline (DB) Packages, and Standard Plastic 300-mil DIPs (NT)**

DB, DW, OR NT PACKAGE
(TOP VIEW)



description

This 8-bit flip-flop features 3-state outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. It is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

The eight flip-flops of the 74AC11374 are edge-triggered D-type flip-flops. On the positive transition of the clock, the Q outputs are set to the logic levels set up at the D inputs.

The output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines signigicantly. The high-impedance third state provides the capability to drive the bus lines in a bus-organized system without need for interface or pullup components.

$\overline{OE}$ does not affect the internal operation of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The 74AC11374 is characterized for operation from –40°C to 85°C.

FUNCTION TABLE
(each flip-flop)

INPUTS			OUTPUT
$\overline{OE}$	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
L	H	X	Q_0
L	↓	X	Q_0
H	X	X	Z

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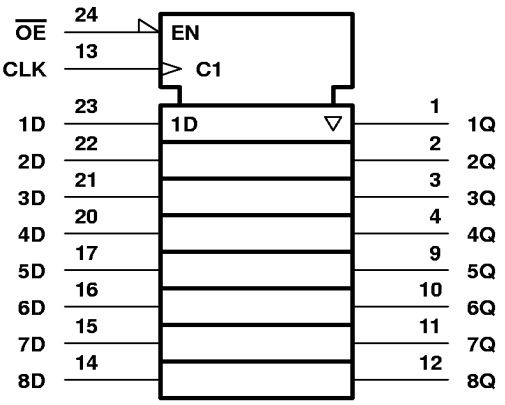
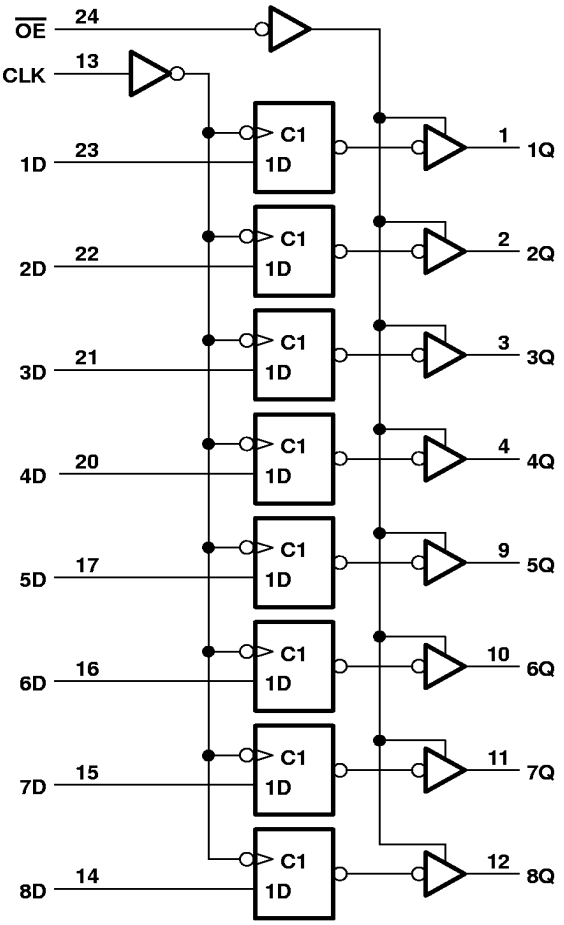
logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . . –0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (see Note 1) . . . . . –0.5 V to V_{CC} + 0.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) . . . . . ±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) . . . . . ±50 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) . . . . . ±50 mA
Continuous current through V_{CC} or GND . . . . . ±200 mA
Maximum power dissipation at T_A = 55°C (in still air) (see Note 2): DB package . . . . . 0.65 W
DW package . . . . . 1.7 W
NT package . . . . . 1.3 W
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils, except for the NT package, which has a trace length of zero.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		3	5	5.5	V
V_{IH}	High-level input voltage	V_{CC} = 3 V	2.1			V
		V_{CC} = 4.5 V	3.15			
		V_{CC} = 5.5 V	3.85			
V_{IL}	Low-level input voltage	V_{CC} = 3 V			0.9	V
		V_{CC} = 4.5 V			1.35	
		V_{CC} = 5.5 V			1.65	
V_I	Input voltage		0		V_{CC}	V
V_O	Output voltage		0		V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 3 V			–4	mA
		V_{CC} = 4.5 V			–24	
		V_{CC} = 5.5 V			–24	
I_{OL}	Low-level output current	V_{CC} = 3 V			12	mA
		V_{CC} = 4.5 V			24	
		V_{CC} = 5.5 V			24	
$\Delta t/\Delta v$	Input transition rise or fall rate	Data	0		10	ns/V
		$\overline{OE}$	0		5	
T_A	Operating free-air temperature		–40		85	°C

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
V_{OH}	I_{OH} = –50 μA	3 V	2.9			2.9		V
		4.5 V	4.4			4.4		
		5.5 V	5.4			5.4		
	I_{OH} = –4 mA	3 V	2.58			2.48		
	I_{OH} = –24 mA	4.5 V	3.94			3.8		
		5.5 V	4.94			4.8		
	I_{OH} = –75 mA†	5.5 V				3.85		
V_{OL}	I_{OL} = 50 μA	3 V			0.1		0.1	V
		4.5 V			0.1		0.1	
		5.5 V			0.1		0.1	
	I_{OL} = 12 mA	3 V			0.36		0.44	
	I_{OL} = 24 mA	4.5 V			0.36		0.44	
		5.5 V			0.36		0.44	
	I_{OL} = 75 mA†	5.5 V					1.65	
I_{OZ}	V_O = V_{CC} or GND	5.5 V			±0.5		±5	μA
I_I	V_I = V_{CC} or GND	5.5 V			±0.1		±1	μA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	5.5 V			8		80	μA
C_i	V_I = V_{CC} or GND	5 V		4				pF
C_o	V_O = V_{CC} or GND	5 V		10				pF

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

timing requirements over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

			T_A = 25°C		MIN	MAX	UNIT
			MIN	MAX			
f_{clock}	Clock frequency		0	75	0	75	MHz
t_w	Pulse duration	CLK low or high	6.5		6.5		ns
t_{su}	Setup time, data before CLK↑		2.5		2.5		ns
t_h	Hold time, data after CLK↑		4.5		4.5		ns

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

			T_A = 25°C		MIN	MAX	UNIT
			MIN	MAX			
f_{clock}	Clock frequency		0	95	0	95	MHz
t_w	Pulse duration	CLK low or high	5		5		ns
t_{su}	Setup time, data before CLK↑		2.5		2.5		ns
t_h	Hold time, data after CLK↑		3.5		3.5		ns

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switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
f_{max}			75	90		75		MHz
t_{PLH}	CLK	Any Q	1.5	9.5	12.5	1.5	14.2	ns
t_{PHL}			1.5	9	12.6	1.5	14	
t_{PZH}	$\overline{OE}$	Any Q	1.5	8	10.9	1.5	12.3	ns
t_{PZL}			1.5	8	11.1	1.5	12.3	
t_{PHZ}	$\overline{OE}$	Any Q	1.5	10	12.1	1.5	12.5	ns
t_{PLZ}			1.5	8	10.7	1.5	11.6	

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	T_A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
f_{max}			95	110		95		MHz
t_{PLH}	CLK	Any Q	1.5	6.5	9	1.5	10.2	ns
t_{PHL}			1.5	5.5	9.1	1.5	10.1	
t_{PZH}	$\overline{OE}$	Any Q	1.5	5.5	8	1.5	9.1	ns
t_{PZL}			1.5	5.5	8.4	1.5	9.4	
t_{PHZ}	$\overline{OE}$	Any Q	1.5	9	11	1.5	11.2	ns
t_{PLZ}			1.5	6	8.6	1.5	9.2	

operating characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER			TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance per flip-flop	Outputs enabled	C_L = 50 pF	f =1 MHz	75	pF
		Outputs disabled			66	

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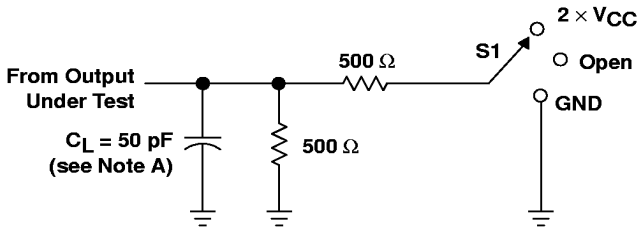
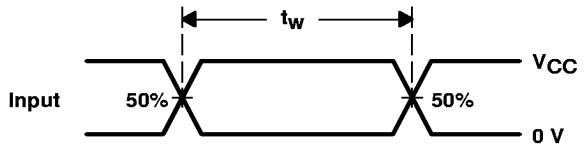
PARAMETER MEASUREMENT INFORMATION

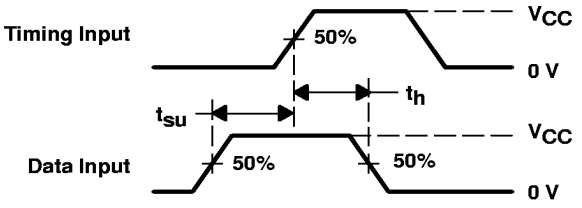


LOAD CIRCUIT

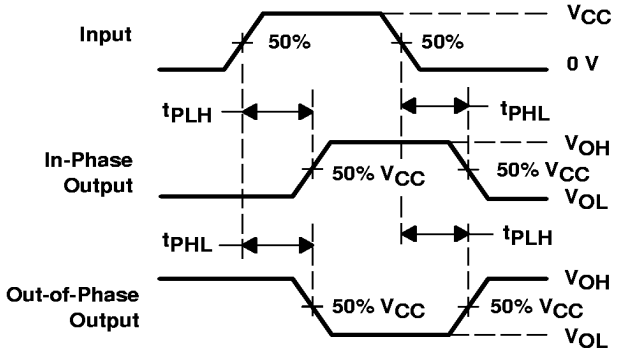
TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND



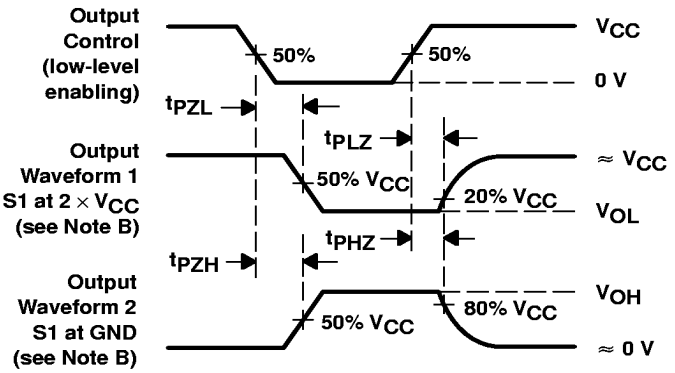
VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 3 ns, t_f = 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

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