

**54AC11827, 74AC11827**

TI0155—D3379, NOVEMBER 1989—REVISED MARCH 1990

- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
  - Flow-Through Architecture to Optimize PCB Layout
  - Center-Pin V<sub>CC</sub> and GND Configurations to Minimize High-Speed Switching Noise
  - EPIC™ (Enhanced-Performance Implanted CMOS) 1-µm Process
  - 500-mA Typical Latch-Up Immunity at 125°C
  - Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs

### **description**

These 10-bit buffers/bus drivers provide high-performance bus interface for wide data paths or buses carrying parity.

The 3-state control gate is a 2-input NOR such that if either  $\overline{G_1}$  or  $\overline{G_2}$  is high, all ten outputs are in the high-impedance state.

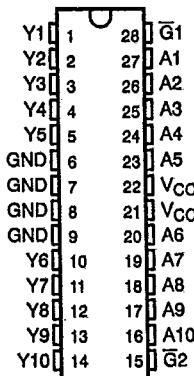
The 'AC11827 provides true data.

The 54AC11827 is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The 74AC11827 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

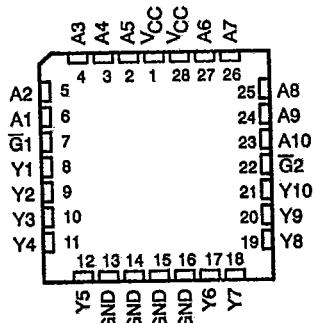
FUNCTION TABLE

INPUTS			OUTPUT
G1	G2	A	
L	L	H	H
L	L	L	L
X	H	X	Z
H	X	X	Z

**54AC11827 ... JT PACKAGE  
74AC11827 ... DW OR NT PACKAGE  
(TOP VIEW)**



54AC11827 ... FK PACKAGE  
(TOP VIEW)



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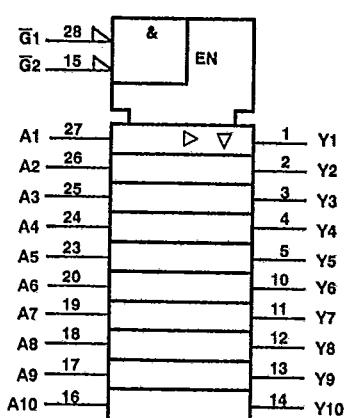
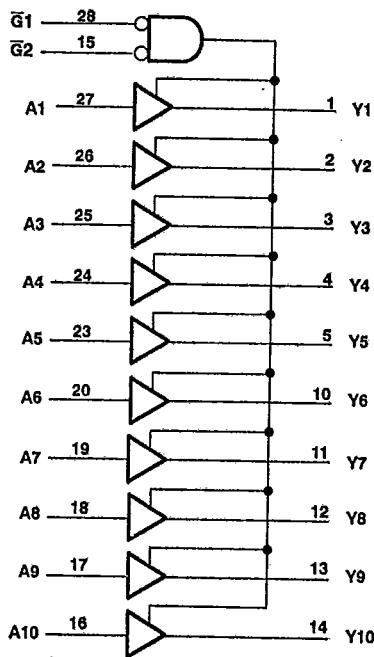
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**54AC11827, 74AC11827**  
**10-BIT BUFFERS/BUS DRIVERS WITH 3-STATE OUTPUTS**

T-52-09

D3379, NOVEMBER 1989—REVISED MARCH 1990—TI0155

**logic symbol†****logic diagram (positive logic)**

† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.  
Pin numbers shown are for DW, JT, and NT packages.

**absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡**

Supply voltage range, $V_{CC}$ .....	-0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) .....	-0.5 V to $V_{CC} + 0.5$ V
Output voltage range, $V_O$ (see Note 1).....	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ ) .....	$\pm 20$ mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ ).....	$\pm 50$ mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ ) .....	$\pm 50$ mA
Continuous current through $V_{CC}$ or GND pins .....	$\pm 250$ mA
Storage temperature range .....	-65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

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**recommended operating conditions****T-52-09**

		54AC11827			74AC11827			UNIT
VCC	Supply voltage	MIN	NOM	MAX	MIN	NOM	MAX	
VIH	VCC = 3 V	2.1			2.1			V
	VCC = 4.5 V	3.15			3.15			
	VCC = 5.5 V	3.85			3.85			
VIL	VCC = 3 V		0.9			0.9		V
	VCC = 4.5 V		1.35			1.35		
	VCC = 5.5 V		1.65			1.65		
VI	Input voltage	0	VCC	0	VCC	VCC	V	
VO	Output voltage	0	VCC	0	VCC	VCC	V	
IOH	VCC = 3 V		-4			-4		mA
	VCC = 4.5 V		-24			-24		
	VCC = 5.5 V		-24			-24		
IOL	VCC = 3 V		12			12		mA
	VCC = 4.5 V		24			24		
	VCC = 5.5 V		24			24		
Δt/Δv	Input transition rise or fall rate	0	10	0	10	ns/V		
TA	Operating free-air temperature	-55	125	-40	85	°C		

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	VCC	TA = 25°C			54AC11827		74AC11827		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
VOH	IOH = -50 μA	3 V	2.9			2.9		2.9		V
		4.5 V	4.4			4.4		4.4		
		5.5 V	5.4			5.4		5.4		
	IOH = -4 mA	3 V	2.58			2.4		2.48		
		4.5 V	3.94			3.7		3.8		
		5.5 V	4.94			4.7		4.8		
VOL	IOL = -50 mA†	5.5 V				3.85				V
		5.5 V						3.85		
		5.5 V								
	IOL = 50 μA	3 V		0.1		0.1		0.1		V
		4.5 V		0.1		0.1		0.1		
		5.5 V		0.1		0.1		0.1		
IOL	IOL = 12 mA	3 V		0.36		0.5		0.44		V
		4.5 V		0.36		0.5		0.44		
		5.5 V		0.36		0.5		0.44		
	IOL = 24 mA	5.5 V				1.65				
		5.5 V						1.65		
		5.5 V								
IOL	IOL = 50 mA†	5.5 V								V
		5.5 V								
		5.5 V								
	IOL = 75 mA†	5.5 V								
		5.5 V								
		5.5 V								
Ioz	VO = VCC or GND	5.5 V		±0.5		±10		±5	μA	
Ii	Vi = VCC or GND	5.5 V		±0.1		±1		±1	μA	
Icc	Vi = VCC or GND, IO = 0	5.5 V		8		160		80	μA	
Ci	Vi = VCC or GND	5 V		4.5					pF	
Co	VO = VCC or GND	5 V		12					pF	

† Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.

PRODUCT PREVIEW Information concerns products in the formative or early phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.

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**54AC11827, 74AC11827  
10-BIT BUFFERS/BUS DRIVERS WITH 3-STATE OUTPUTS**

T-52-09

D9379, NOVEMBER 1989—REVISED MARCH 1990—TI0165

switching characteristics over recommended operating free-air temperature range,  
 $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25^\circ\text{C}$			54AC11827		74AC11827		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$t_{PLH}$	A	Y	4.8	8.4	10.8	4.8	13.5	4.8	12.4	ns
			6.8	10.4	12.6	6.8	14.1	6.8	13.4	
$t_{PHL}$	$\overline{G}_1$ or $\overline{G}_2$	Y	6.3	10.2	12.7	6.3	15.9	6.3	14.5	ns
			10	16	19.2	10	22.3	10	21.7	
$t_{PZH}$	$\overline{G}_1$ or $\overline{G}_2$	Y	5.9	8.5	10.4	5.9	11.6	5.9	11.1	ns
			5.4	8	10	5.4	10.9	5.4	10.5	
$t_{PZL}$	$\overline{G}_1$ or $\overline{G}_2$	Y								

switching characteristics over recommended operating free-air temperature range,  
 $V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$T_A = 25^\circ\text{C}$			54AC11827		74AC11827		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$t_{PLH}$	A	Y	2.1	5.3	7.5	2.1	9.2	2.1	8.7	ns
			2.9	6.2	8.4	2.9	10.2	2.9	9.7	
$t_{PHL}$	$\overline{G}_1$ or $\overline{G}_2$	Y	3.1	5.9	8.2	3.1	10.5	3.1	9.7	ns
			4.1	7.7	10.6	4.1	14	4.1	13	
$t_{PZH}$	$\overline{G}_1$ or $\overline{G}_2$	Y	3.9	6.6	8.4	3.9	9.6	3.9	9.1	ns
			4	6.3	7.9	4	9.2	4	8.8	
$t_{PZL}$	$\overline{G}_1$ or $\overline{G}_2$	Y								

operating characteristics,  $V_{CC} = 5 \text{ V}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS		TYP	UNIT
	Outputs enabled	Outputs disabled		
Cpd Power dissipation capacitance		$C_L = 50 \text{ pF}, f = 1 \text{ MHz}$	35 9	pF

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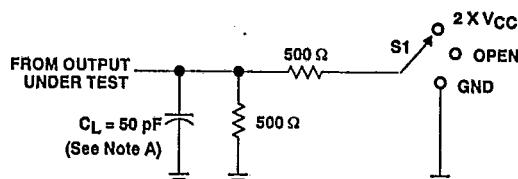
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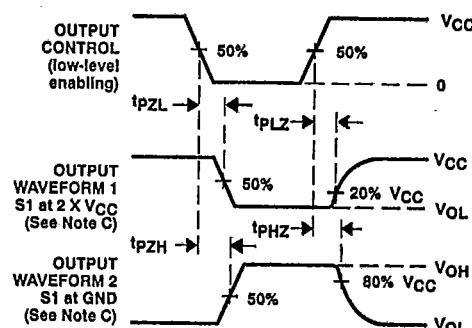
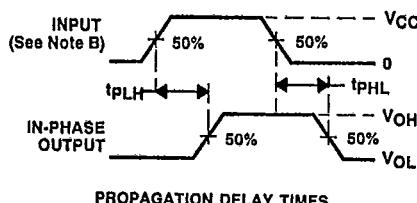
## PARAMETER MEASUREMENT INFORMATION

T-52-09



TEST	S1
tPLH/tPHL	Open
tPLZ/tPZL	2 x VCC
tPHZ/tPZH	GND

LOAD CIRCUIT FOR OUTPUTS



- NOTES:
- A.  $C_L$  includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - C. All input pulses are supplied by the generators having the following characteristics: PRR  $\leq 10 \text{ MHz}$ ,  $Z_0 = 50 \Omega$ ,  $t_f \leq 2.5 \text{ ns}$ .
  - D. The outputs are measured one at a time with one transition per measurement.

FIGURE 1. LOAD CIRCUIT AND VOLTAGE WAVEFORMS