16-BIT REGISTERED BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

TI0246--- D3569, JUNE 1990

- Members of Texas Instruments Widebus™ **Family**
- Packaged in Shrink Small-Outline 300-mil Packages (SSOP) and 380-mil Fine-Pitch Ceramic Flat Packages Using 25-mil Center-to-Center Pin Spacings
- Inputs are TTL- or CMOS-Voltage Compatible
- 3-State Outputs Drive Bus Lines Directly
- Flow-Through Architecture Optimizes PCB Layout
- Distributed VCC and GND Pin Configuration Minimizes High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1-µm Process
- 500-mA Typical Latch-Up Immunity at 125°C

description

The 'AC16470 and 'ACT16470 are noninverting 16-bit registered bus transceivers composed of two 8-bit sections with separate control signals. For either 8-bit transceiver section, data flow in the A-to-B mode is controlled by output enable (10EAB or 20EAB), direction enable (1DEAB or 2DEAB), and clock (1CLKAB or 2CLKAB)

54AC16470, 54ACT16470 ... WD PACKAGE 74AC18470, 74ACT16470 ... DL PACKAGE (TOP VIEW)

10EAB [, 0	56	10EBA
1CLKAB			1 CLKBA
1DEAB			1DEBA
GND		53	GND
TA1		52	191
1A2 🗍		51	182
V _{cc} 🗍	7	50	ĪVcc
1Ă3 🛘		49	183
184	9	48	184
1A5 🗌	10	47]185
GND [11	48	GND
1A6 🛚]186
1A7 🗌	13		187
1A8 🛚]1B8
2A1 [2B1
2A2 🗌			282
2A3 🗌			283
GND [GND
2A4] 2B4
2A5 🗌			285
2A6			2B6
V ₀₀ [⊒v _{cc}
2A7 [287
2A8 [288
GND			GND
2DEAB			20EBA
2CLKAB			2CLKB
20EAB	28	29] 20EBA

When 1DEAB (or 2DEAB) is high, storage of the current A-bus data is inhibited and the corresponding B outputs are in the high-impedance state. When 1DEAB (or 2DEAB) is low, the register contents and the output buffers are controlled by 1CLKAB (or 2CLKAB) and 1OEAB (or 2OEAB). A low level on 1CLKAB (or 2CLKAB) inhibits register loading; a low-to-high transition on 1CLKAB (or 2CLKAB) causes loading of the corresponding registers with the current A-bus data. If 10EAB (or 20EAB) is low, the corresponding B outputs reflect the contents of the registers. A high level on 10EAB (or 20EAB) causes the B outputs to be in the high-impedance state.

FUNCTION TABLE, EACH SECTION[†]

INPUTS			LATOURATA	B OUTPUTS
DEAB	· CLKAB	ÖEAB	LATCH DATA	BOUIPUIS
Н	X	Х	Previous A Data	Z
L	L	Н	Previous A Data	Z
L	L	L	Previous A Data	Previous A Data
Ĺ	<u>↑</u>	Н	Current A Data	Z
L	<u> </u>	L	Current A Data	Current A Data

† A-to-B data flow is shown. B-to-A data flow is controlled analogously by DEBA, CLKBA, and OEBA.

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PRODUCT PREVIE

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54AC16470, 54ACT16470 74AC16470, 74ACT16470 16-BIT REGISTERED BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

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Data flow from B to A is similar, but uses 10EBA and/or 20EBA, 1DEBA and/or 2DEBA, and 1CLKBA and/or 2CLKBA.

The 74AC16470 and 74ACT16470 are packaged in TI's shrink small-outline package (SSOP) with 25-mil center-to-center pin spacings. This package provides twice the I/O pin count and functionality of a standard small-outline package in the same printed-circuit-board area.

The 'AC16470 has CMOS-compatible input thresholds. The 'ACT16470 has TTL-compatible input thresholds.

The 54AC16470 and 54ACT16470 are characterized over the full military temperature range of -55°C to 125°C. The 74AC16470 and 74ACT16470 are characterized for operation from -40°C to 85°C.

