NATIONAL SEMICOND {LOGIC} 02E D 6501122 0062588 5

54AC/74AC564 • 54ACT/74ACT564

T-46-07-11

Octal D-Type Latch With 3-State Outputs

Description

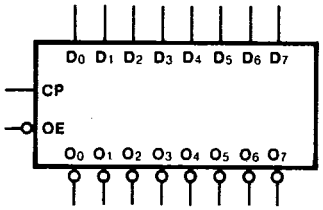
The 'AC/'ACT564 is a high-speed, low power octal flip-flop with a buffered common Clock (CP) and a buffered common Output Enable ($\overline{OE}$). The information presented to the D inputs is stored in the flip-flops on the LOW-to-HIGH Clock (CP) transition.

The 'AC/'ACT564 device is functionally identical to the 'AC/'ACT574, but with inverted outputs.

- **Inputs and Outputs on Opposite Sides of Package Allowing Easy Interface with Microprocessors**
- **Useful as Input or Output Port for Microprocessors**
- **Functionally Identical to 'AC/'ACT574 but with Inverted Outputs**
- **3-State Outputs for Bus-Oriented Applications**
- **Outputs Source/Sink 24 mA**
- **'ACT564 has TTL-Compatible Inputs**

Ordering Code: See Section 6

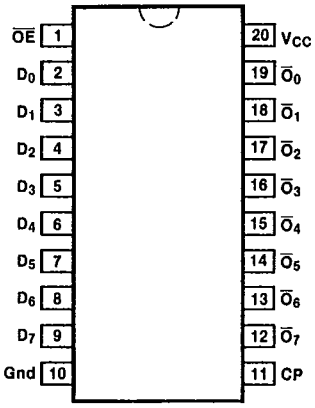
Logic Symbol



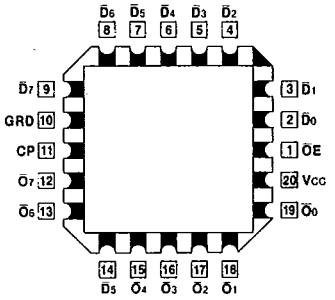
Pin Names

D_0 - D_7	Data Inputs
CP	Clock Pulse Input
$\overline{OE}$	3-State Output Enable Input
$\overline{O}_0$ - $\overline{O}_7$	3-State Outputs

Connection Diagrams



Pin Assignment for DIP, Flatpak and SOIC



Pin Assignment for LCC

Functional Description

The 'AC/'ACT564 consists of eight edge-triggered flip-flops with individual D-type inputs and 3-state complementary outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold times requirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable ($\overline{OE}$) LOW, the contents of the eight flip-flops are available at the outputs. When $\overline{OE}$ is HIGH, the outputs go to the high impedance state. Operation of the $\overline{OE}$ input does not affect the state of the flip-flops.

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Function Table

Inputs			Internal	Outputs	Function
$\overline{OE}$	CP	D	Q	O	
H	H	L	NC	Z	Hold
H	H	H	NC	Z	Hold
H	⌐	L	H	Z	Load
H	⌐	H	L	Z	Load
L	⌐	L	H	H	Data Available
L	⌐	H	L	L	Data Available
L	H	L	NC	NC	No Change in Data
L	H	H	NC	NC	No Change in Data

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance
⌐ = LOW-to-HIGH Transition
NC = No Change

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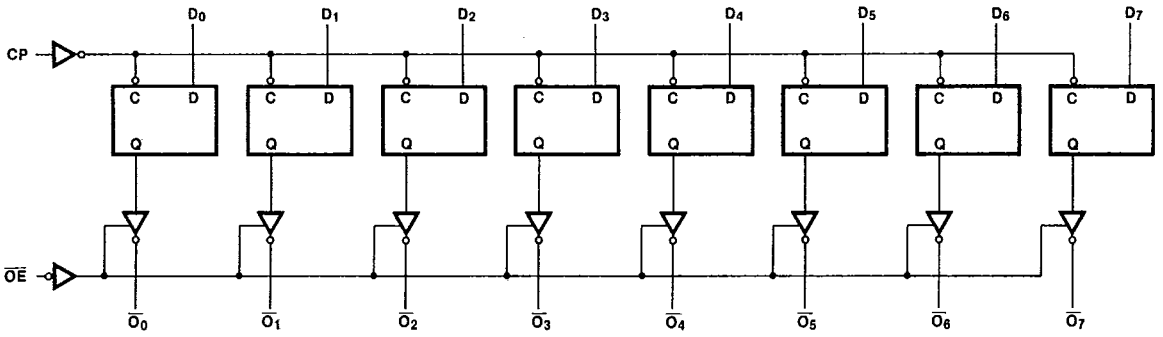
Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics (unless otherwise specified)

Symbol	Parameter	54AC/ACT	74AC/ACT	Units	Conditions
I_{CC}	Maximum Quiescent Supply Current	160	80	μA	V_{IN} = Vcc or Ground, Vcc = 5.5 V, T_A = Worst Case
I_{CC}	Maximum Quiescent Supply Current	8.0	8.0	μA	V_{IN} = Vcc or Ground, Vcc = 5.5 V, T_A = 25°C
I_{CCT}	Maximum Additional Icc/Input ('ACT564)	1.6	1.5	mA	V_{IN} = Vcc − 2.1 V Vcc = 5.5 V, T_A = Worst Case

AC Characteristics

Symbol	Parameter	Vcc* (V)	74AC T_A = +25°C C_L = 50 pF			54AC T_A = −55°C to +125°C C_L = 50 pF		74AC T_A = −40°C to +85°C C_L = 50 pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	3.3 5.0		110 150						MHz	3-3
t_{PLH}	Propagation Delay CP to $\overline{O}_n$	3.3 5.0		10.5 7.0						ns	3-6
t_{PHL}	Propagation Delay CP to $\overline{O}_n$	3.3 5.0		9.5 6.0						ns	3-6
t_{PZH}	Output Enable Time	3.3 5.0		8.5 6.5						ns	3-7
t_{PZL}	Output Enable Time	3.3 5.0		8.0 5.5						ns	3-8
t_{PHZ}	Output Disable Time	3.3 5.0		9.5 7.0						ns	3-7
t_{PLZ}	Output Disable Time	3.3 5.0		7.5 5.5						ns	3-8

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

AC Operating Requirements

Symbol	Parameter	Vcc* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF	54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum			
t_s	Setup Time, HIGH or LOW D_n to CP	3.3 5.0	2.0 1.0			ns	3-9
t_h	Hold Time, HIGH or LOW D_n to CP	3.3 5.0	−1.0 −0.5			ns	3-9
t_w	CP Pulse Width, HIGH or LOW	3.3 5.0	3.5 2.5			ns	3-6

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

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AC Characteristics

Symbol	Parameter	Vcc* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Clock Frequency	5.0	85	90		65		75		MHz	3-3
t_{PLH}	Propagation Delay CP to $\overline{O}_n$	5.0	1.0	6.5	10.5	1.0	12.5	1.0	11.5	ns	3-6
t_{PHL}	Propagation Delay CP to $\overline{O}_n$	5.0	1.0	6.0	9.5	1.0	11.5	1.0	10.5	ns	3-6
t_{PZH}	Output Enable Time	5.0	1.0	5.5	9.0	1.0	10.5	1.0	9.5	ns	3-7
t_{PZL}	Output Enable Time	5.0	1.0	5.5	8.5	1.0	10.5	1.0	9.5	ns	3-8
t_{PHZ}	Output Disable Time	5.0	1.0	7.0	10.5	1.0	12.5	1.0	11.5	ns	3-7
t_{PLZ}	Output Disable Time	5.0	1.0	5.0	8.0	1.0	9.0	1.0	8.5	ns	3-8

*Voltage Range 5.0 is 5.0 V ± 0.5 V

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AC Operating Requirements

Symbol	Parameter	Vcc* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF		54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Setup Time, HIGH or LOW D_n to CP	5.0	1.0	2.5	3.0	3.0	ns	3-9
t_h	Hold Time, HIGH or LOW D_n to CP	5.0	−0.5	1.0	1.0	1.0	ns	3-9
t_w	LE Pulse Width, HIGH or LOW	5.0	2.5	3.0	5.0	3.5	ns	3-6

*Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

Capacitance

Symbol	Parameter	54/74AC/ACT Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.5$ V
C_{PD}	Power Dissipation Capacitance	50.0	pF	$V_{CC} = 5.5$ V