



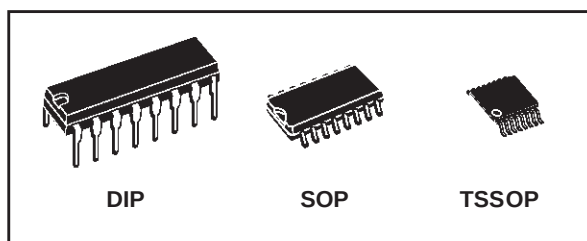
74ACT174

HEX D-TYPE FLIP FLOP WITH CLEAR

- HIGH SPEED:
 $f_{MAX} = 200\text{MHz}$ (TYP.) at $V_{CC} = 5\text{V}$
- LOW POWER DISSIPATION:
 $I_{CC} = 4\mu\text{A}$ (MAX.) at $T_A = 25^\circ\text{C}$
- COMPATIBLE WITH TTL OUTPUTS
 $V_{IH} = 2\text{V}$ (MIN.), $V_{IL} = 0.8\text{V}$ (MAX.)
- 50Ω TRANSMISSION LINE DRIVING CAPABILITY
- SYMMETRICAL OUTPUT IMPEDANCE:
 $|I_{OH}| = I_{OL} = 24\text{mA}$ (MIN)
- BALANCED PROPAGATION DELAYS:
 $t_{PLH} \approx t_{PHL}$
- OPERATING VOLTAGE RANGE:
 V_{CC} (OPR) = 4.5V to 5.5V
- PIN AND FUNCTION COMPATIBLE WITH 74 SERIES 174
- IMPROVED LATCH-UP IMMUNITY

DESCRIPTION

The 74ACT174 is an advanced high-speed CMOS HEX D-TYPE FLIP FLOP WITH CLEAR fabricated with sub-micron silicon gate and double-layer metal wiring C²MOS technology. Information signals applied to D inputs are transferred to the Q output on the positive going edge of the clock pulse.

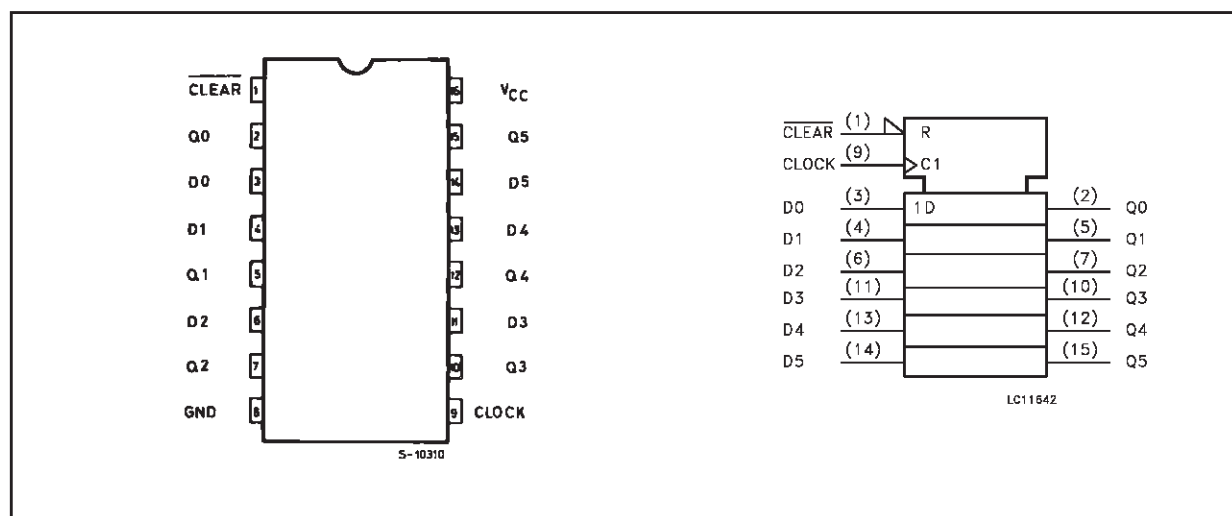


ORDER CODES

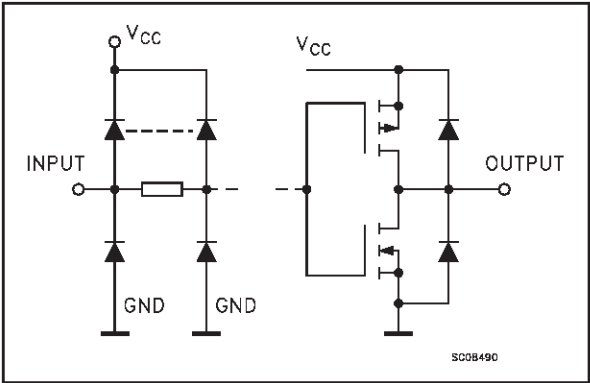
PACKAGE	TUBE	T & R
DIP	74ACT174B	
SOP	74ACT174M	74ACT174MTR
TSSOP		74ACT174TTR

When the CLEAR input is held low, the Q outputs are held low independently of the other inputs. The device is designed to interface directly High Speed CMOS systems with TTL, NMOS and CMOS output voltage levels. All inputs and outputs are equipped with protection circuits against static discharge, giving them 2KV ESD immunity and transient excess voltage.

PIN CONNECTION AND IEC LOGIC SYMBOLS



INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

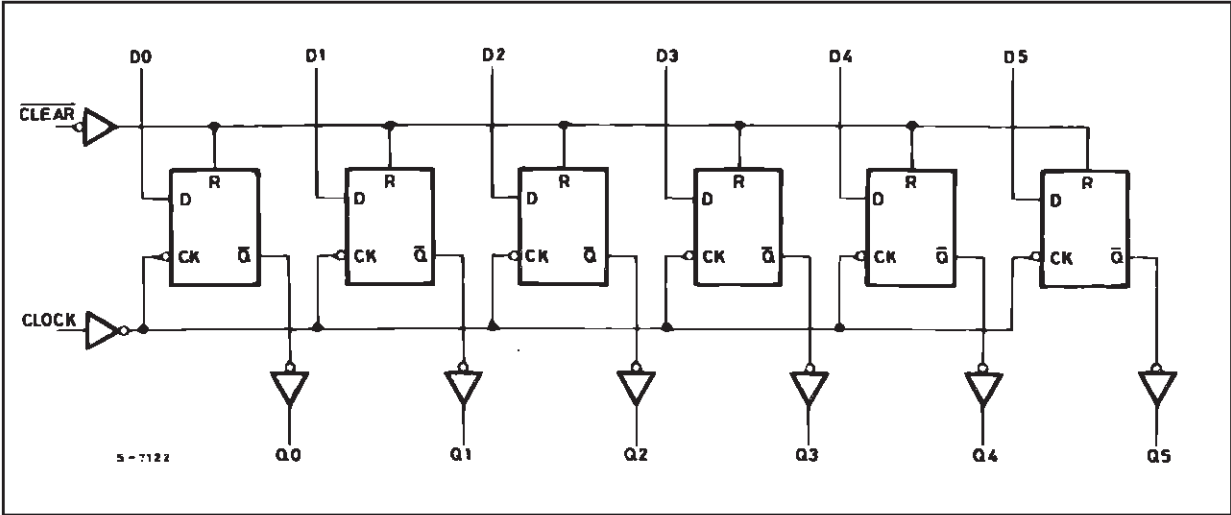
PIN No	SYMBOL	NAME AND FUNCTION
1	$\overline{\text{CLEAR}}$	Asynchronous Master Reset (Active LOW)
2, 5, 7, 10, 12, 15	Q0 to Q5	Flip-Flop Outputs
3, 4, 6, 11, 13, 14	D0 to D5	Data Inputs
9	CLOCK	Clock Input (LOW-to-HIGH, Edge Trigger)
8	GND	Ground (0V)
16	V _{CC}	Positive Supply Voltage

TRUTH TABLE

INPUTS			OUTPUT	FUNCTION
$\overline{\text{CLEAR}}$	D	CLOCK	Q	
L	X	X	L	CLEAR
H	L		L	
H	H		H	
H	X		Q _n	NO CHANGE

X : Don't Care

LOGIC DIAGRAM



This logic diagram has not to be used to estimate propagation delays

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to $V_{CC} + 0.5$	V
V_O	DC Output Voltage	-0.5 to $V_{CC} + 0.5$	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Current	± 50	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 300	mA
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	4.5 to 5.5	V
V_I	Input Voltage	0 to V_{CC}	V
V_O	Output Voltage	0 to V_{CC}	V
T_{op}	Operating Temperature	-55 to 125	°C
dt/dv	Input Rise and Fall Time $V_{CC} = 4.5$ to $5.5V$ (note 1)	8	ns/V

1) V_{IN} from 0.8V to 2.0V

DC SPECIFICATIONS

Symbol	Parameter	Test Condition		Value						Unit	
		V _{CC} (V)		T _A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
V _{IH}	High Level Input Voltage	4.5	V _O = 0.1 V or V _{CC} -0.1V	2.0	1.5		2.0		2.0		V
		5.5		2.0	1.5		2.0		2.0		
V _{IL}	Low Level Input Voltage	4.5	V _O = 0.1 V or V _{CC} -0.1V		1.5	0.8		0.8		0.8	V
		5.5			1.5	0.8		0.8		0.8	
V _{OH}	High Level Output Voltage	4.5	I _O =-50 μA	4.4	4.49		4.4		4.4		V
		5.5	I _O =-50 μA	5.4	5.49		5.4		5.4		
		4.5	I _O =-24 mA	3.86			3.76		3.7		V
		5.5	I _O =-24 mA	4.86			4.76		4.7		
V _{OL}	Low Level Output Voltage	4.5	I _O =50 μA		0.001	0.1		0.1		0.1	V
		5.5	I _O =50 μA		0.001	0.1		0.1		0.1	
		4.5	I _O =24 mA			0.36		0.44		0.5	
		5.5	I _O =24 mA			0.36		0.44		0.5	
I _I	Input Leakage Cur- rent	5.5	V _I = V _{CC} or GND			± 0.1		± 1		± 1	μA
I _{CCT}	Max I _{CC} /Input	5.5	V _I = V _{CC} - 2.1V		0.6			1.5		1.6	mA
I _{CC}	Quiescent Supply Current	5.5	V _I = V _{CC} or GND			4		40		80	μA
I _{OLD}	Dynamic Output	5.5	V _{OLD} = 1.65 V max					75		50	mA
I _{OHD}	Current (note 1, 2)		V _{OHD} = 3.85 V min					-75		-50	mA

1) Maximum test duration 2ms, one output loaded at a time

2) Incident wave switching is guaranteed on transmission lines with impedances as low as 50Ω

AC ELECTRICAL CHARACTERISTICS (C_L = 50 pF, R_L = 500 Ω, Input t_r = t_f = 3ns)

Symbol	Parameter	Test Condition		Value						Unit	
		V _{CC} (V)		T _A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
t _{PLH} t _{PHL}	Propagation Delay Time CLOCK to Y	5.0(*)		1.5	6.0	10.5		11.5		11.5	ns
t _{PLH} t _{PHL}	Propagation Delay Time CLEAR to Y	5.0(*)		1.5	7.0	9.5		11.0		11.0	ns
t _{WL}	CLEAR Pulse Width, LOW	5.0(*)			3.0	4.5		5.0		5.0	ns
t _W	CLOCK Pulse Width	5.0(*)			3.0	4.5		5.0		5.0	ns
t _s	Setup Time D to CLOCK, HIGH or LOW	5.0(*)			0.5	1.5		1.5		1.5	ns
t _h	Hold Time D to CLOCK, HIGH or LOW	5.0(*)			1.0	2.0		2.0		2.0	ns
t _{REM}	Recovery Time CLEAR to CLOCK	5.0(*)			0.0	0.5		0.5		0.5	ns
f _{MAX}	Maximum CLOCK Frequency	5.0(*)		165	200		140		140		MHz

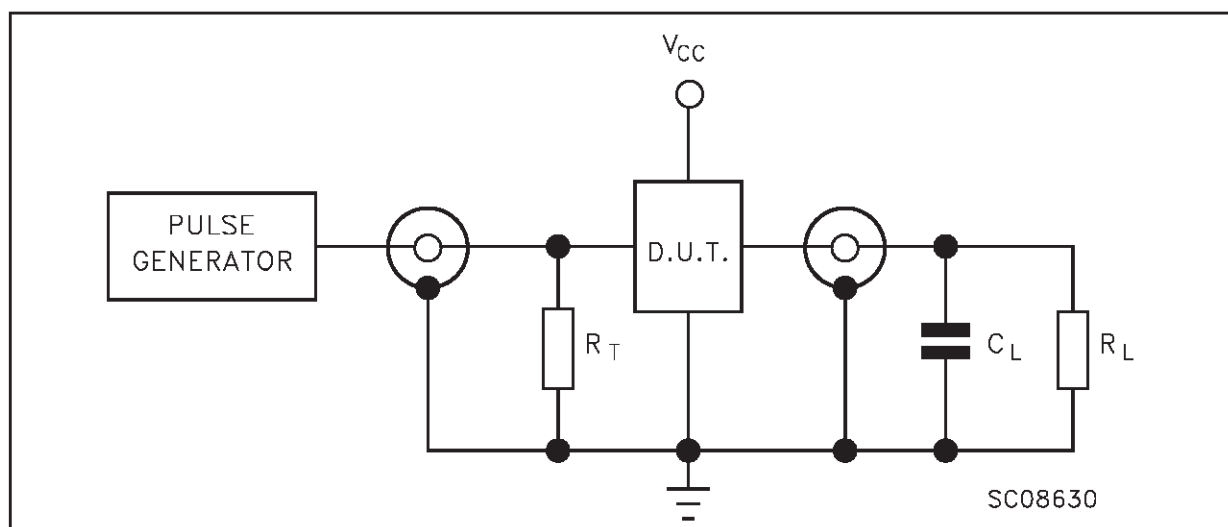
(*) Voltage range is 5.0V ± 0.5V

CAPACITIVE CHARACTERISTICS

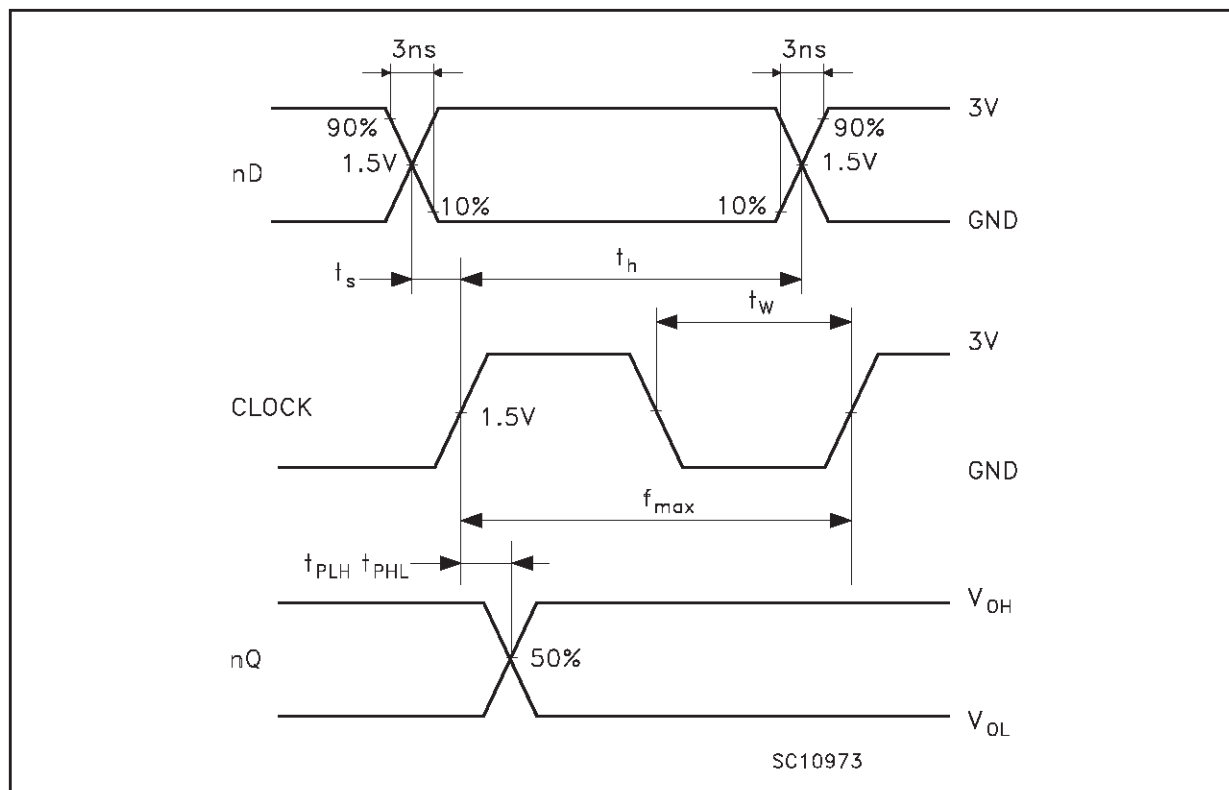
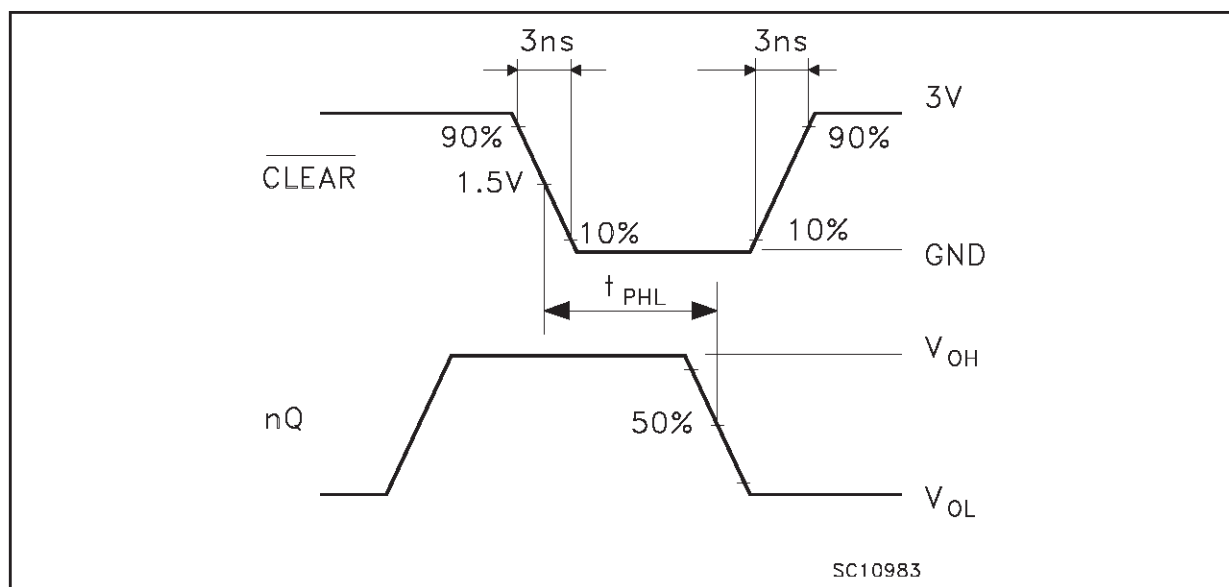
Symbol	Parameter	Test Condition		Value						Unit	
		V _{CC} (V)		T _A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
C _{IN}	Input Capacitance	5.0			4						pF
C _{PD}	Power Dissipation Capacitance (note 1)	5.0	f _{IN} = 10MHz		35						pF

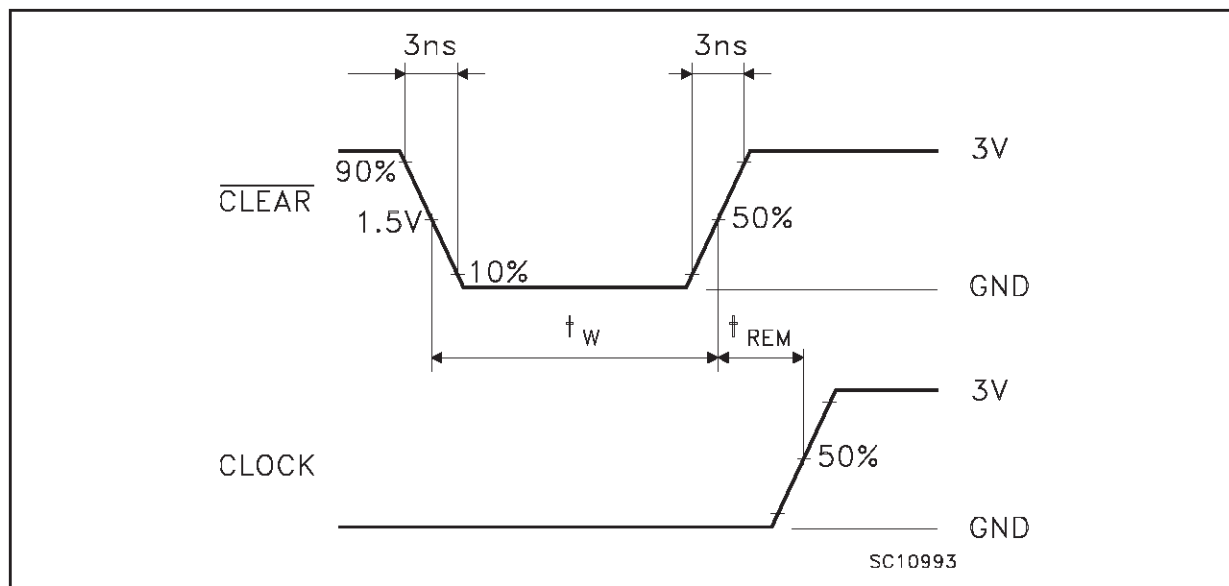
1) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation. $I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}/n$ (per circuit)

TEST CIRCUIT



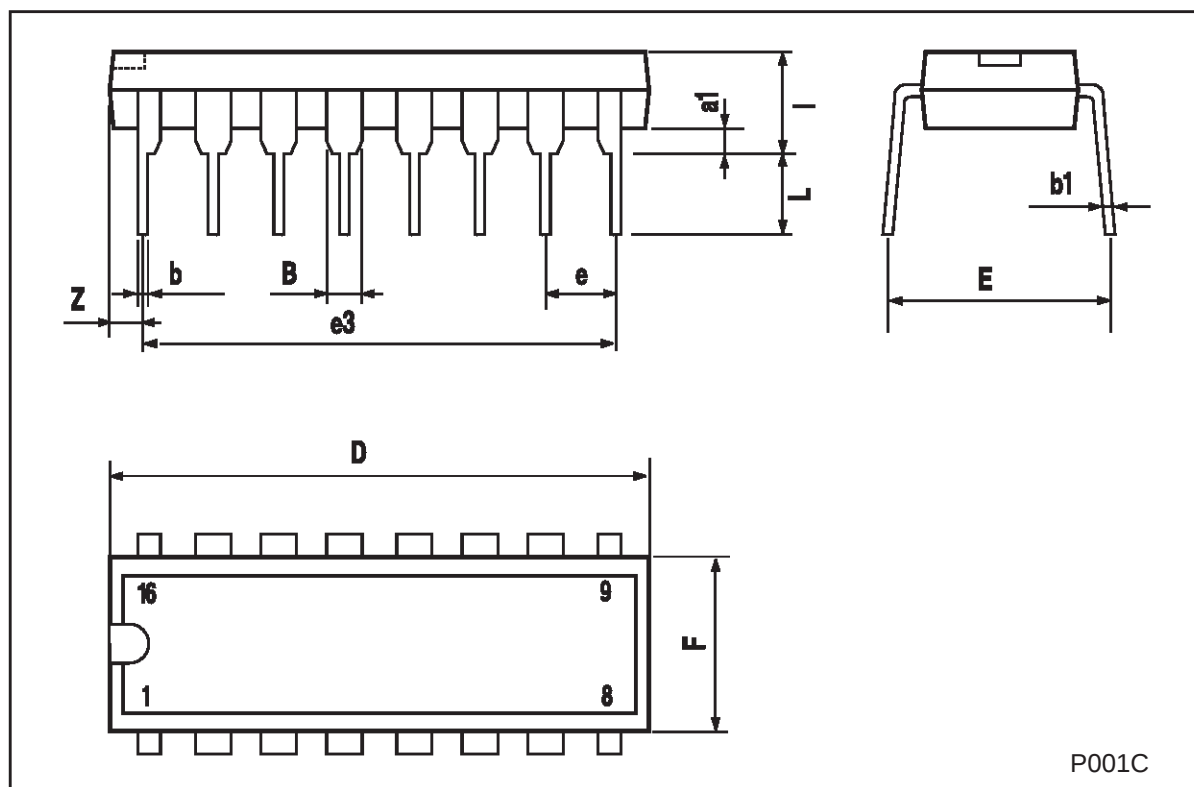
C_L = 50pF or equivalent (includes jig and probe capacitance)
R_L = R₁ = 500Ω or equivalent
R_T = Z_{OUT} of pulse generator (typically 50Ω)

WAVEFORM 1: PROPAGATION DELAYS, SETUP AND HOLD TIMES ($f=1\text{MHz}$; 50% duty cycle)**WAVEFORM 2: PROPAGATION DELAYS ($f=1\text{MHz}$; 50% duty cycle)**

WAVEFORM 3: RECOVERY TIME ($f=1\text{MHz}$; 50% duty cycle)

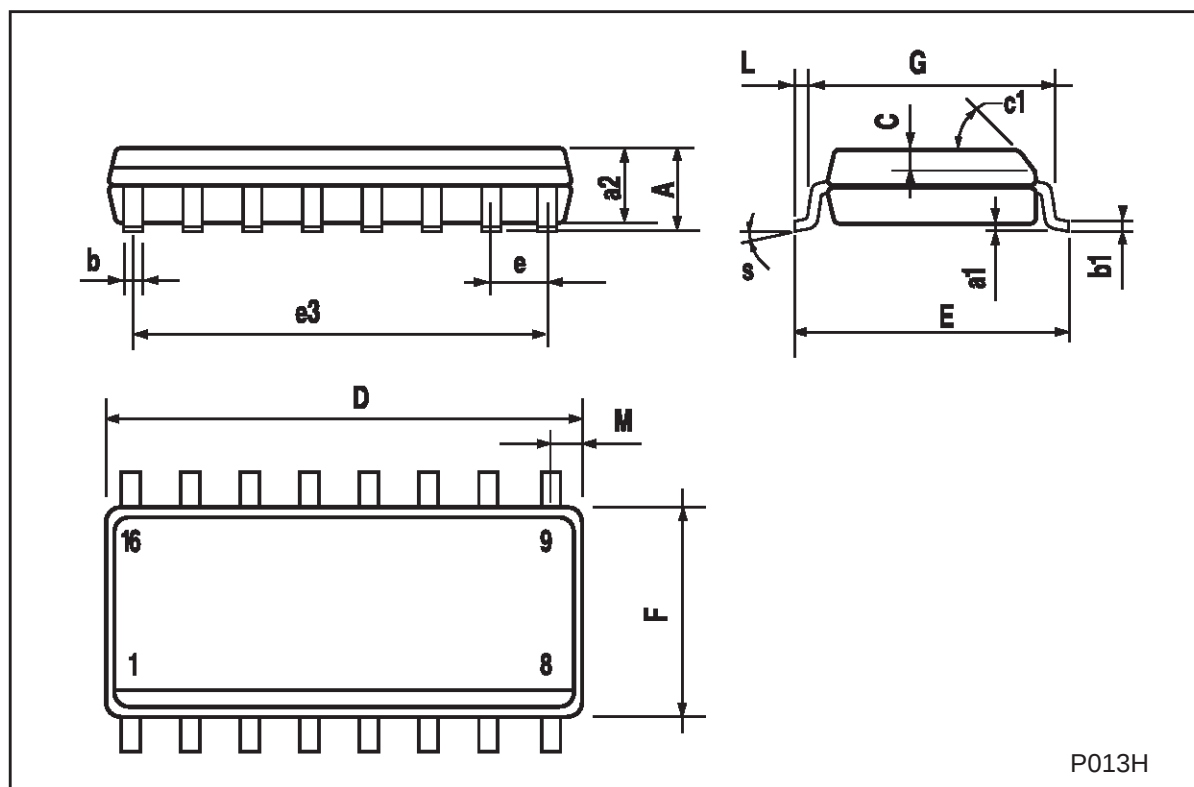
Plastic DIP-16 (0.25) MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.77		1.65	0.030		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		17.78			0.700	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050



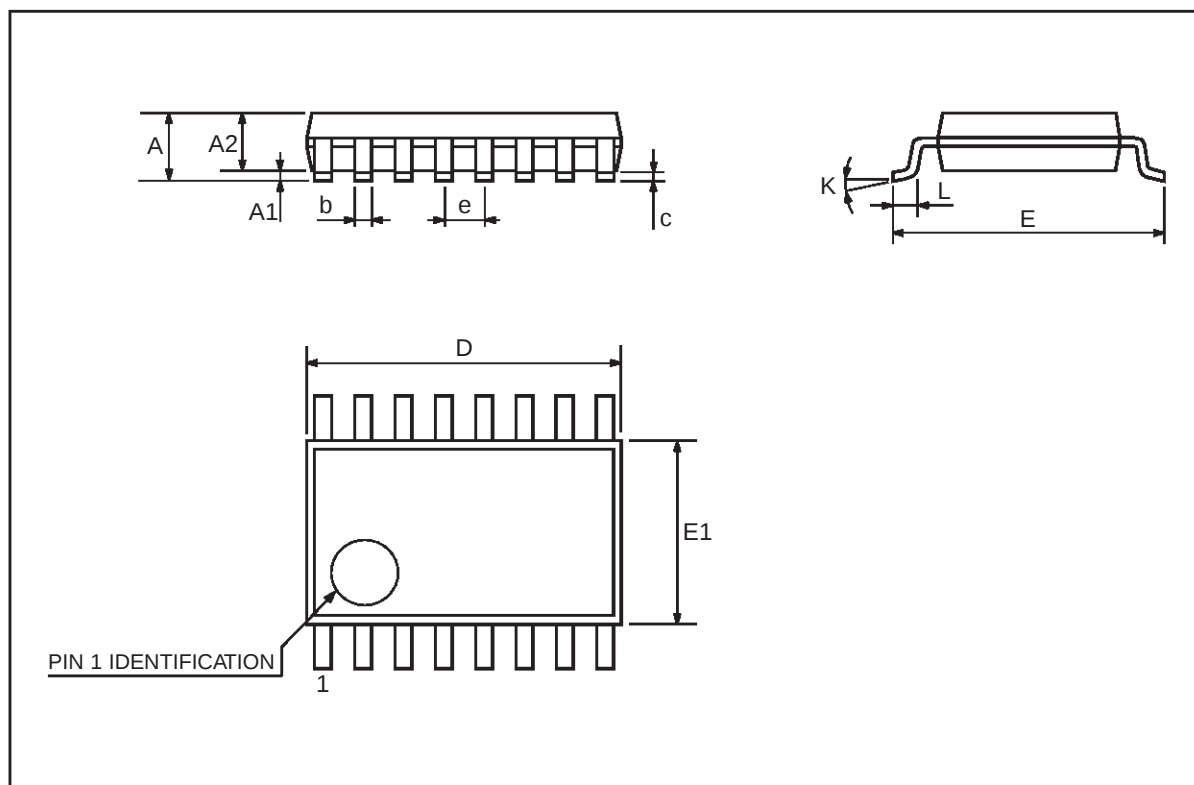
SO-16 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.2	0.004		0.007
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45 (typ.)					
D	9.8		10	0.385		0.393
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		8.89			0.350	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.62			0.024
S	8 (max.)					



TSSOP16 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.1			0.433
A1	0.05	0.10	0.15	0.002	0.004	0.006
A2	0.85	0.9	0.95	0.335	0.354	0.374
b	0.19		0.30	0.0075		0.0118
c	0.09		0.20	0.0035		0.0079
D	4.9	5	5.1	0.193	0.197	0.201
E	6.25	6.4	6.5	0.246	0.252	0.256
E1	4.3	4.4	4.48	0.169	0.173	0.176
e		0.65 BSC			0.0256 BSC	
K	0°	4°	8°	0°	4°	8°
L	0.50	0.60	0.70	0.020	0.024	0.028



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