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54AC/74AC843 • 54ACT/74ACT843
54AC/74AC844 • 54ACT/74ACT844

T-46-07-12

9-Bit Transparent Latch

Description

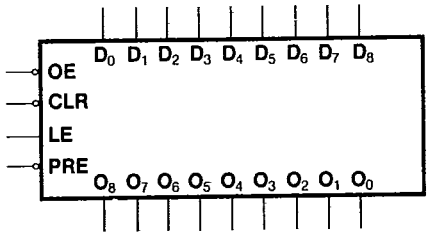
The 'AC/'ACT843 and 'AC/'ACT844 bus interface latch is designed to eliminate the extra packages required to buffer existing latches and provide extra data width for wider address/data paths or buses carrying parity.

The 'AC/'ACT843 is functionally and pin compatible with AMD's AM29843.

- **'ACT843 and 'ACT844 have TTL-Compatible Inputs**

Ordering Code: See Section 6

Logic Symbol ('AC/'ACT843)*

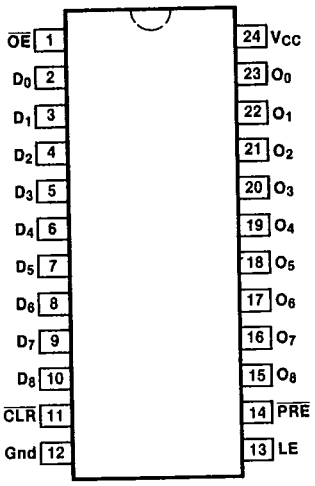


*The 'AC/'ACT844 has inverting outputs.

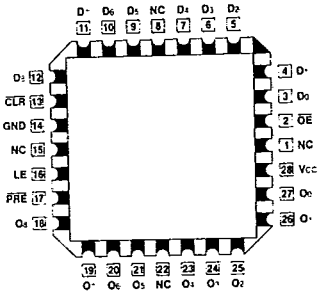
Pin Names

D_0 - D_8	Data Inputs
O_0 - O_8	Data Outputs ('AC/'ACT843)
$\overline{O}_0$ - $\overline{O}_8$	Data Outputs ('AC/'ACT844)
$\overline{OE}$	Output Enable
LE	Latch Enable
$\overline{CLR}$	Clear
$\overline{PRE}$	Preset

Connection Diagrams



Pin Assignment for DIP, Flatpak and SOIC



Pin Assignment for LCC

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Functional Description

The 'AC/'ACT843 and 'AC/'ACT844 consist of nine D-type latches with 3-state outputs. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. This allows asynchronous operation, as the output transition follows the data in transition. On the LE HIGH-to-LOW transition, the data that meets the setup times is latched. Data appears on the bus when the Output Enable ($\overline{OE}$) is LOW. When $\overline{OE}$ is HIGH, the bus output is in the high impedance state. In addition to the LE and $\overline{OE}$ pins, the 'AC/'ACT843 and 'AC/'ACT844 have a Clear ($\overline{CLR}$) pin and a Preset ($\overline{PRE}$) pin. These pins are ideal for parity bus interfacing in high performance systems. When $\overline{CLR}$ is LOW, the outputs are LOW if $\overline{OE}$ is LOW. When $\overline{CLR}$ is HIGH, data can be entered into the latch. When $\overline{PRE}$ is LOW, the outputs are HIGH if $\overline{OE}$ is LOW. Preset overides $\overline{CLR}$.

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Function Tables

Inputs					Internal	Outputs		Function
$\overline{CLR}$	$\overline{PRE}$	$\overline{OE}$	LE	D	Q	O ('843)	$\overline{O}$ ('844)	
H	H	H	H	L	L	Z	Z	High Z
H	H	H	H	H	H	Z	Z	High Z
H	H	H	L	X	NC	Z	Z	Latched
H	H	L	H	L	L	L	H	Transparent
H	H	L	H	H	H	H	L	Transparent
H	H	L	L	X	NC	NC	NC	Latched
H	L	L	X	X	H	H	L	Preset
L	H	L	X	X	L	L	H	Clear
L	L	L	X	X	H	H	L	Preset
L	H	H	L	X	L	Z	Z	Clear/High Z
H	L	H	L	X	H	Z	Z	Preset/High Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance
NC = No Change

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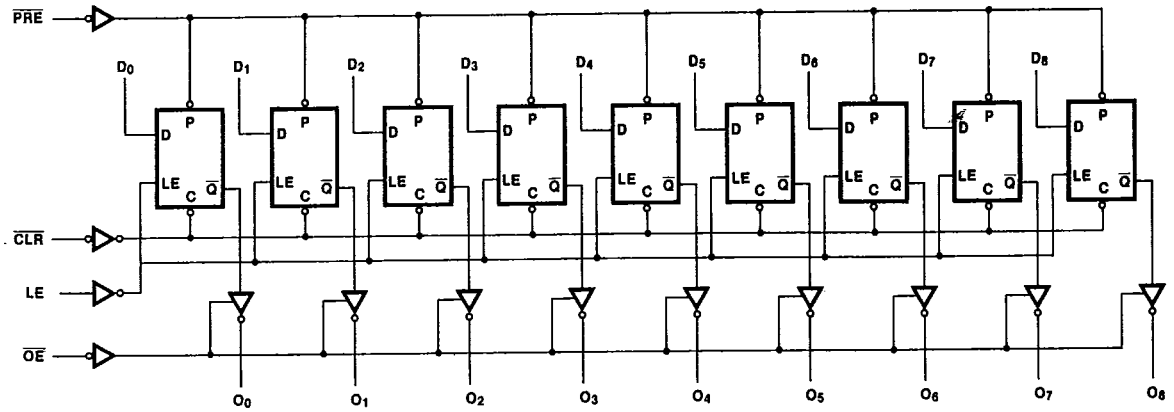
Logic Diagram ('AC/'ACT843)



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays. The 'AC/'ACT844 has the same logic diagram with inverting outputs.

DC Characteristics (unless otherwise specified)

Symbol	Parameter	54AC/ACT	74AC/ACT	Units	Conditions
I_{CC}	Maximum Quiescent Supply Current	160	80	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, T_A = Worst Case
I_{CC}	Maximum Quiescent Supply Current	8.0	8.0	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, $T_A = 25°C$
I_{CCT}	Maximum Additional Icc/Input ('ACT843/844)	1.6	1.5	mA	$V_{IN} = V_{CC} - 2.1$ V, $V_{CC} = 5.5$ V, T_A = Worst Case

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AC Characteristics

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Symbol	Parameter	Vcc* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay D_n to O_n	3.3 5.0		17.0 12.0						ns	3-5
t_{PHL}	Propagation Delay D_n to O_n	3.3 5.0		16.5 11.0						ns	3-5
t_{PLH}	Propagation Delay LE to O_n	3.3 5.0		18.5 13.0						ns	3-6
t_{PHL}	Propagation Delay LE to O_n	3.3 5.0		17.0 12.0						ns	3-6
t_{PLH}	Propagation Delay $\overline{PRE}$ to O_n	3.3 5.0		17.0 12.0						ns	3-6
t_{PHL}	Propagation Delay $\overline{CLR}$ to O_n	3.3 5.0		17.0 12.0						ns	3-6
t_{PZH}	Output Enable Time $\overline{OE}$ to O_n	3.3 5.0		14.5 10.0						ns	3-7
t_{PZL}	Output Enable Time $\overline{OE}$ to O_n	3.3 5.0		11.5 8.0						ns	3-8
t_{PHZ}	Output Disable Time $\overline{OE}$ to O_n	3.3 5.0		13.0 9.0						ns	3-7
t_{PLZ}	Output Disable Time $\overline{OE}$ to O_n	3.3 5.0		13.0 9.0						ns	3-8

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

PRELIMINARY

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AC Operating Requirements

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Symbol	Parameter	Vcc* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF		54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Setup Time, HIGH or LOW D_n to LE	3.3 5.0	4.0 2.5				ns	3-9
t_h	Hold Time, HIGH or LOW D_n to LE	3.3 5.0	0 0				ns	3-9
t_w	LE Pulse Width, HIGH	3.3 5.0	4.0 2.5				ns	3-6
t_w	$\overline{PRE}$ Pulse Width, LOW	3.3 5.0	4.0 2.5				ns	3-6
t_w	$\overline{CLR}$ Pulse Width, LOW	3.3 5.0	4.0 2.5				ns	3-6
t_{rec}	$\overline{PRE}$ Recovery Time	3.3 5.0	5.0 4.0				ns	3-9
t_{rec}	$\overline{CLR}$ Recovery Time	3.3 5.0	5.0 4.0				ns	3-9

PRELIMINARY

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

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AC Characteristics

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Symbol	Parameter	Vcc* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay D_n to O_n	5.0		12.0						ns	3-5
t_{PHL}	Propagation Delay D_n to O_n	5.0		11.0						ns	3-5
t_{PLH}	Propagation Delay LE to O_n	5.0		13.0						ns	3-6
t_{PHL}	Propagation Delay LE to O_n	5.0		12.0						ns	3-6
t_{PLH}	Propagation Delay $\overline{PRE}$ to O_n	5.0		12.0						ns	3-6
t_{PHL}	Propagation Delay $\overline{CLR}$ to O_n	5.0		12.0						ns	3-6
t_{PZH}	Output Enable Time $\overline{OE}$ to O_n	5.0		10.0						ns	3-7
t_{PZL}	Output Enable Time $\overline{OE}$ to O_n	5.0		8.0						ns	3-8
t_{PHZ}	Output Disable Time $\overline{OE}$ to O_n	5.0		9.0						ns	3-7
t_{PLZ}	Output Disable Time $\overline{OE}$ to O_n	5.0		9.0						ns	3-8

*Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

PRELIMINARY

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AC Operating Requirements

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Symbol	Parameter	Vcc* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF		54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF	74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF	Units	Fig. No.
			Typ	Guaranteed Minimum				
t_s	Setup Time, HIGH or LOW D_n to LE	5.0	2.5				ns	3-9
t_h	Hold Time, HIGH or LOW D_n to LE	5.0	0				ns	3-9
t_w	LE Pulse Width, HIGH	5.0	2.5				ns	3-6
t_w	$\overline{PRE}$ Pulse Width, LOW	5.0	2.5				ns	3-6
t_w	$\overline{CLR}$ Pulse Width, LOW	5.0	2.5				ns	3-6
t_{rec}	$\overline{PRE}$ Recovery Time	5.0	5.0				ns	3-9
t_{rec}	$\overline{CLR}$ Recovery Time	5.0	5.0				ns	3-9

*Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

Capacitance

Symbol	Parameter	54/74AC/ACT Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.5$ V
C_{PD}	Power Dissipation Capacitance		pF	$V_{CC} = 5.5$ V

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