

2.5V/3.3V 18-bit bus-interface D-type flip-flop with reset and enable with 30Ω termination resistors (3-State)

74ALVT162823

FEATURES

- Two sets of high speed parallel registers with positive edge-triggered D-type flip-flops
- 5V I/O Compatible
- Ideal where high speed, light loading, or increased fan-in are required with MOS microprocessors
- Live insertion/extraction permitted
- Power-up 3-State
- Power-up Reset
- Output capability: +12mA/−12mA
- Latch-up protection exceeds 500mA per Jedec Std 17
- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model
- Bus hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Outputs include series resistance of 30Ω making external termination resistors unnecessary

DESCRIPTION

The 74ALVT162823 18-bit bus interface register is designed to eliminate the extra packages required to buffer existing registers and provide extra data width for wider data/address paths of buses carrying parity.

The 74ALVT162823 has two 9-bit wide buffered registers with Clock Enable ($\overline{nCE}$) and Master Reset ($\overline{nMR}$) which are ideal for parity bus interfacing in high microprogrammed systems.

The registers are fully edge-triggered. The state of each D input, one set-up time before the Low-to-High clock transition is transferred to the corresponding flip-flop's Q output.

The 74ALVT162823 is designed with 30Ω series resistance in both the pull-up and pull-down output structures. This design reduces line noise in applications such as memory address drivers, clock drivers, and bus receivers/transmitters.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS $T_{amb} = 25^{\circ}\text{C}$; GND = 0V	TYPICAL		UNIT
			2.5V	3.3V	
t_{PLH} t_{PHL}	Propagation delay nCP to nQx	$C_L = 50\text{pF}$	4.2 3.4	3.0 2.8	ns
C_{IN}	Input capacitance	$V_I = 0\text{V}$ or V_{CC}	3	3	pF
C_{OUT}	Output capacitance	$V_{I/O} = 0\text{V}$ or 3.0V	9	9	pF
I_{CCZ}	Total supply current	Outputs disabled	40	70	μA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
56-Pin Plastic SSOP Type III	−40°C to +85°C	74ALVT162823 DL	AV162823 DL	SOT371-1
56-Pin Plastic TSSOP Type II	−40°C to +85°C	74ALVT162823 DGG	AV162823 DGG	SOT364-1

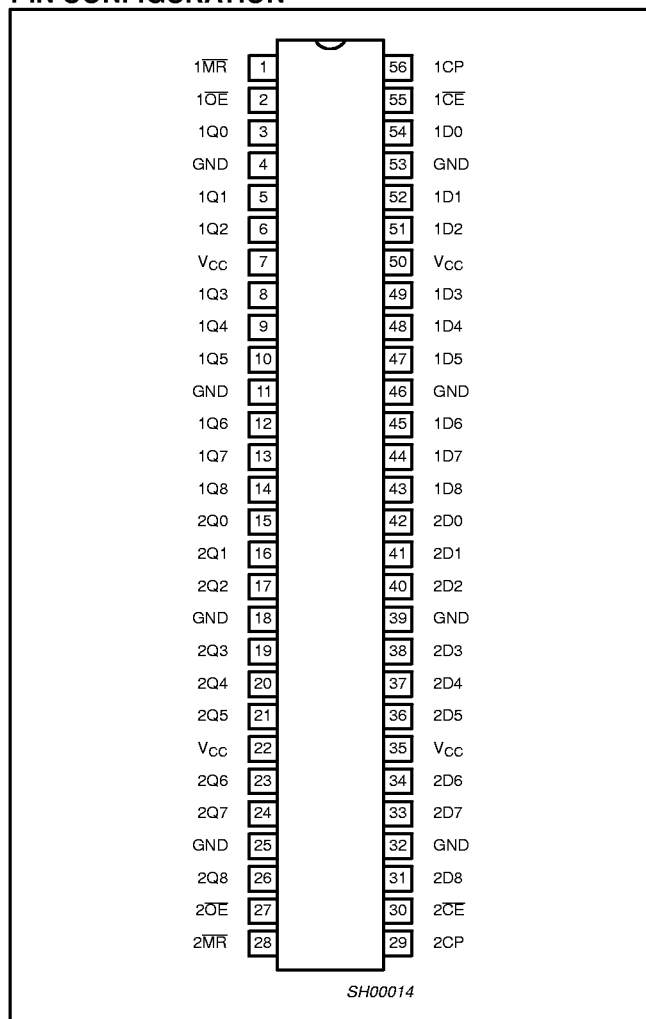
PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
2, 27	$1\overline{OE}$, $2\overline{OE}$	Output enable input (active-Low)
54, 52, 51, 49, 48, 47, 45, 44, 43 42, 41, 40, 38, 37, 36, 34, 33, 31	$1D0-1D8$ $2D0-2D8$	Data inputs
3, 5, 6, 8, 9, 10, 12, 13, 14 15, 16, 17, 19, 20, 21, 23, 24, 26	$1Q0-1Q8$ $2Q0-2Q8$	Data outputs
56, 29	$1CP$, $2CP$	Clock pulse input (active rising edge)
55, 30	$1\overline{CE}$, $2\overline{CE}$	Clock enable input (active-Low)
1, 28	$1\overline{MR}$, $2\overline{MR}$	Master reset input (active-Low)
4, 11, 18, 25, 32, 39, 46, 53	GND	Ground (0V)
7, 22, 35, 50	V_{CC}	Positive supply voltage

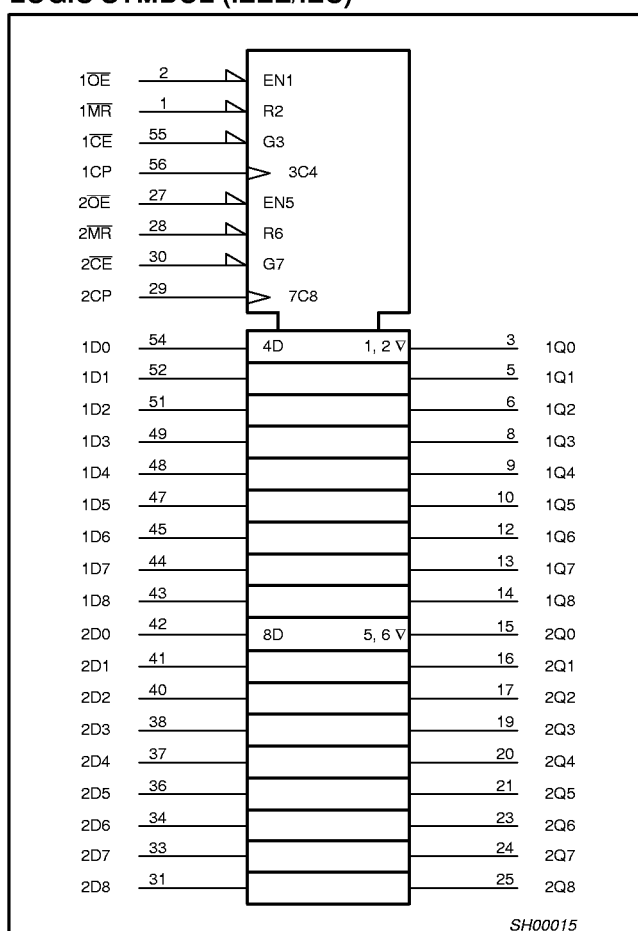
2.5V/3.3V 18-bit bus-interface D-type flip-flop with reset and enable with 30Ω termination resistors (3-State)

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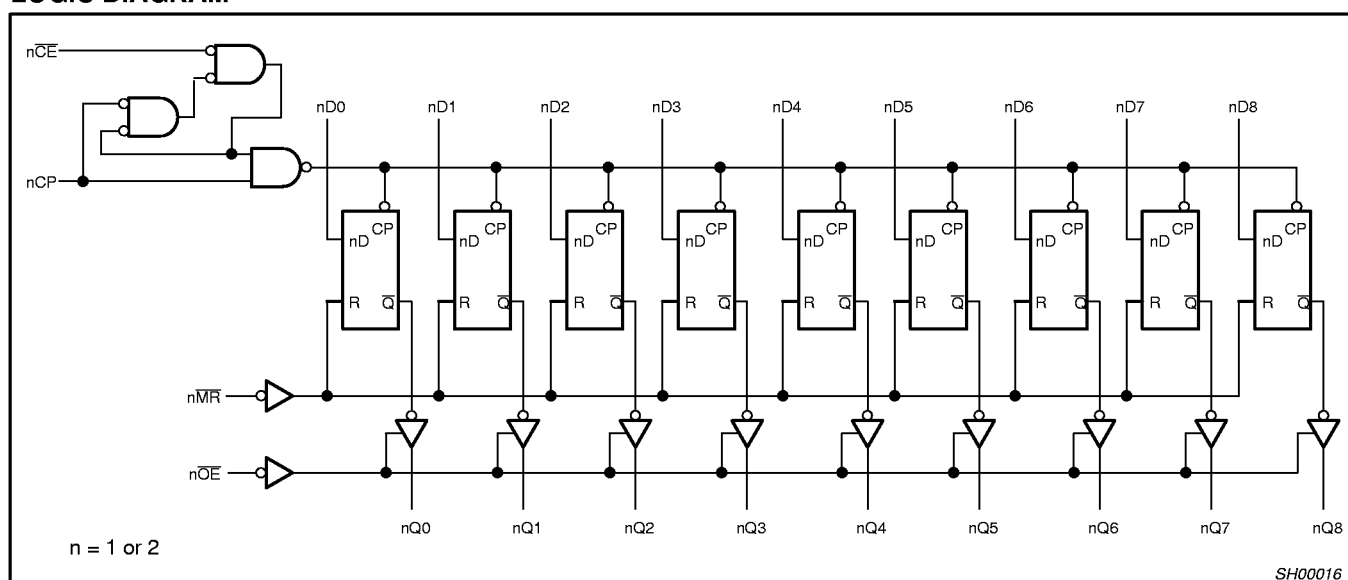
PIN CONFIGURATION



LOGIC SYMBOL (IEEE/IEC)



LOGIC DIAGRAM



2.5V/3.3V 18-bit bus-interface D-type flip-flop with reset and enable with 30Ω termination resistors (3-State)

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FUNCTION TABLE

INPUTS					OUTPUTS	OPERATING MODE
nOE	nMR	nCE	nCP	nDx	nQ0 – nQ8	
L	L	X	X	X	L	Clear
L	H	L	↑	h	H	Load and read data
L	H	L	↑	l	L	
L	H	H	↑	X	NC	Hold
H	X	X	X	X	Z	High impedance

H = High voltage level

h = High voltage level one set-up time prior to the Low-to-High clock transition

L = Low voltage level

l = Low voltage level one set-up time prior to the Low-to-High clock transition

NC = No change

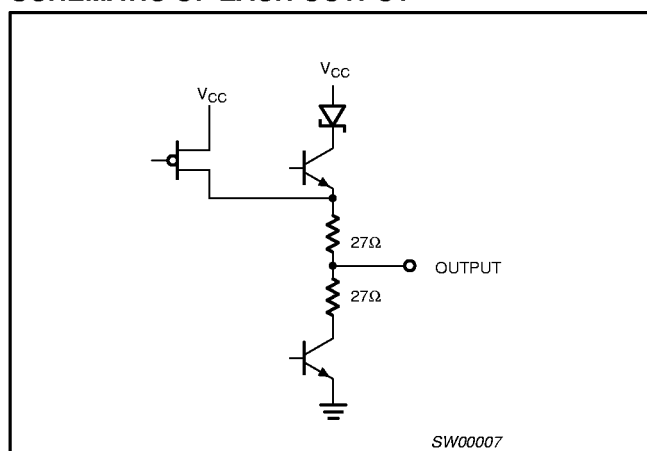
X = Don't care

Z = High impedance "off" state

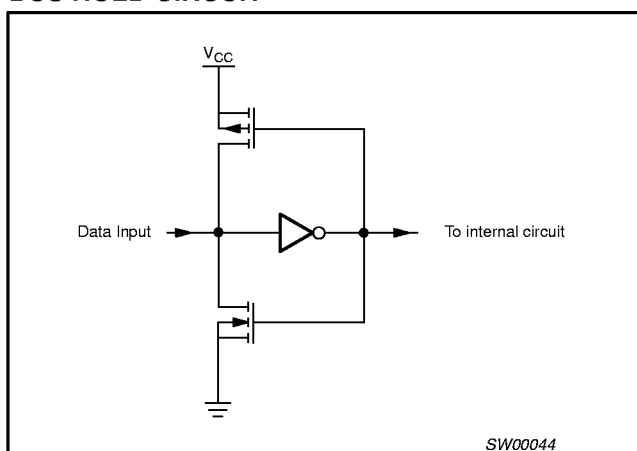
↑ = Low to High clock transition

↑ = Not a Low-to-High clock transition

SCHEMATIC OF EACH OUTPUT



BUS HOLD CIRCUIT



ABSOLUTE MAXIMUM RATINGS^{1, 2}

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V _{CC}	DC supply voltage		-0.5 to +4.6	V
I _{IK}	DC input diode current	V _I < 0	-50	mA
V _I	DC input voltage ³		-0.5 to +7.0	V
I _{OK}	DC output diode current	V _O < 0	-50	mA
V _{OUT}	DC output voltage ³	Output in Off or High state	-0.5 to +7.0	V
I _{OUT}	DC output current	Output in Low state	128	mA
		Output in High state	-64	
T _{stg}	Storage temperature range		-65 to +150	°C

NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
- The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

2.5V/3.3V 18-bit bus-interface D-type flip-flop with reset and enable with 30Ω termination resistors (3-State)

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RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	2.5V RANGE LIMITS		3.3V RANGE LIMITS		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	DC supply voltage	2.3	2.7	3.0	3.6	V
V_I	Input voltage	0	5.5	0	5.5	V
V_{IH}	High-level input voltage	1.7		2.0		V
V_{IL}	Input voltage		0.7		0.8	V
I_{OH}	High-level output current		-8		-12	mA
I_{OL}	Low-level output current		12		12	mA
$\Delta t/\Delta v$	Input transition rise or fall rate; Outputs enabled		10		10	ns/V
T_{amb}	Operating free-air temperature range	-40	+85	-40	+85	°C

DC ELECTRICAL CHARACTERISTICS (3.3V ± 0.3V RANGE)

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS			UNIT
				Temp = -40°C to +85°C			
				MIN	TYP ¹	MAX	
V _{IK}	Input clamp voltage	V _{CC} = 3.0V; I _{IK} = -18mA			-0.85	-1.2	V
V _{OH}	High-level output voltage	V _{CC} = 3.0V; I _{OH} = -12mA		2.0	2.3		V
V _{OL}	Low-level output voltage	V _{CC} = 3.0V; I _{OL} = 12mA			0.5	0.8	V
V _{RST}	Power-up output low voltage ⁶	V _{CC} = 3.6V; I _O = 1mA; V _I = V _{CC} or GND				0.55	V
I _I	Input leakage current	V _{CC} = 3.6V; V _I = V _{CC} or GND	Control pins		0.1	±1	μA
		V _{CC} = 0 or 3.6V; V _I = 5.5V			0.1	10	
		V _{CC} = 3.6V; V _I = 5.5V	Data pins ⁴		0.1	10	μA
		V _{CC} = 3.6V; V _I = V _{CC}			0.5	1	
		V _{CC} = 3.6V; V _I = 0			0.1	-5	
I _{OFF}	Off current	V _{CC} = 0V; V _I or V _O = 0 to 4.5V			0.1	±100	μA
I _{HOLD}	Bus Hold current D inputs ⁷	V _{CC} = 3V; V _I = 0.8V		75	130		μA
		V _{CC} = 3V; V _I = 2.0V		-75	-140		
		V _{CC} = 0V to 3.6V; V _{CC} = 3.6V		±500			
I _{EX}	Current into an output in the High state when V _O > V _{CC}	V _O = 5.5V; V _{CC} = 3.0V			10	125	μA
I _{PU/PD}	Power up/down 3-State output current ³	V _{CC} ≤ 1.2V; V _O = 0.5V to V _{CC} ; V _I = GND or V _{CC} OE/OE = Don't care			1	±100	μA
I _{OZH}	3-State output High current	V _{CC} = 3.6V; V _O = 3.0V; V _I = V _{IL} or V _{IH}			0.5	5	μA
I _{OZL}	3-State output Low current	V _{CC} = 3.6V; V _O = 0.5V; V _I = V _{IL} or V _{IH}			0.5	-5	μA
I _{CCH}	Quiescent supply current	V _{CC} = 3.6V; Outputs High, V _I = GND or V _{CC} , I _O = 0			0.05	0.1	mA
I _{CCL}		V _{CC} = 3.6V; Outputs Low, V _I = GND or V _{CC} , I _O = 0			3.9	5.5	
I _{CCZ}		V _{CC} = 3.6V; Outputs Disabled; V _I = GND or V _{CC} , I _O = 0 ⁵			0.06	0.1	
ΔI _{CC}	Additional supply current per input pin ²	V _{CC} = 3V to 3.6V; One input at V _{CC} -0.6V, Other inputs at V _{CC} or GND			0.04	0.4	mA

NOTES:

- All typical values are at $V_{CC} = 3.3V$ and $T_{amb} = 25^\circ C$.
- This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND
- This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From $V_{CC} = 1.2V$ to $V_{CC} = 3.3V \pm 0.3V$ a transition time of 100μsec is permitted. This parameter is valid for $T_{amb} = 25^\circ C$ only.
- Unused pins at V_{CC} or GND.
- I_{CCZ} is measured with outputs pulled up to V_{CC} or pulled down to ground.
- For valid test results, data must not be loaded into the flip-flops (or latches) after applying power.
- This is the bus hold overdrive current required to force the input to the opposite logic state.

2.5V/3.3V 18-bit bus-interface D-type flip-flop with reset and enable with 30Ω termination resistors (3-State)

74ALVT162823

AC CHARACTERISTICS (3.3V ± 0.3V RANGE)

GND = 0V, $t_R = t_F = 2.5\text{ns}$, $C_L = 50\text{pF}$, $R_L = 500\Omega$

SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			T _{amb} = −40°C to +85°C V _{CC} = +3.3V ±0.3V			
			MIN	TYP	MAX	
f _{MAX}	Maximum clock frequency	1				MHz
t _{PLH} t _{PHL}	Propagation delay nCP to nQx	1	1.8 1.8	3.0 2.8	4.7 4.0	ns
t _{PHL}	Propagation delay nMR to nQx	2	1.8	2.8	4.0	ns
t _{PZH} t _{PZL}	Output enable time to High and Low level	4 5	1.9 1.6	3.5 2.6	5.7 3.8	ns
t _{PHZ} t _{PLZ}	Output disable time from High and Low level	4 5	1.9 1.5	3.4 2.5	5.2 3.8	ns

AC SETUP REQUIREMENTS (3.3V ± 0.3V RANGE)

GND = 0V, $t_R = t_F = 2.5\text{ns}$, $C_L = 50\text{pF}$, $R_L = 500\Omega$

SYMBOL	PARAMETER	WAVEFORM	LIMITS		UNIT
			$T_{\text{amb}} = -40 \text{ to } +85^{\circ}\text{C}$ $V_{\text{CC}} = +3.3\text{V} \pm 0.3\text{V}$		
			MIN	TYP	
$t_{\text{S}}(\text{H})$ $t_{\text{S}}(\text{L})$	Setup time, High or Low nDx to nCP	3	1.0 1.2	0.6 0.7	ns
$t_{\text{h}}(\text{H})$ $t_{\text{h}}(\text{L})$	Hold time, High or Low nDx to nCP	3	0.1 0.1	−0.8 −0.6	ns
$t_{\text{w}}(\text{H})$ $t_{\text{w}}(\text{L})$	nCP pulse width High or Low	1	1.5 2.5	0.7 1.7	ns
$t_{\text{S}}(\text{H})$ $t_{\text{S}}(\text{L})$	Setup time, High or Low nCE to nCP	3	1.0 0.5	0.2 −0.5	ns
$t_{\text{h}}(\text{H})$ $t_{\text{h}}(\text{L})$	Hold time, High or Low nCE to nCP	3	1.0 1.0	0.5 −0.1	ns
$t_{\text{w}}(\text{L})$	nMR pulse width, Low	2	2.0	1.5	ns
t_{rec}	Recovery time nMR to nCP	2	2.0	1.4	ns

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DC ELECTRICAL CHARACTERISTICS (2.5V ± 0.2V RANGE)

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS			UNIT
				Temp = -40°C to +85°C			
				MIN	TYP ¹	MAX	
V _{IK}	Input clamp voltage	V _{CC} = 2.3V; I _{IK} = -18mA			-0.85	-1.2	V
V _{OH}	High-level output voltage	V _{CC} = 2.3V; I _{OH} = -8mA		1.7	2.5		V
V _{OL}	Low-level output voltage	V _{CC} = 2.3V; I _{OL} = 12mA			0.3	0.5	V
V _{RST}	Power-up output low voltage ⁷	V _{CC} = 2.7V; I _O = 1mA; V _I = V _{CC} or GND			0.2	0.55	V
I _I	Input leakage current	V _{CC} = 2.7V; V _I = GND	Control pins		0.1	±1	μA
		V _{CC} = 2.7V; V _I = 5.5V			0.1	10	
		V _{CC} = 3.6V; V _I = 5.5V	Data pins ⁴		0.1	10	μA
		V _{CC} = 3.6V; V _I = V _{CC}			0.5	1	
		V _{CC} = 3.6V; V _I = 0			0.1	-5	
I _{OFF}	Off current	V _{CC} = 0V; V _I or V _O = 0 to 4.5V			0.1	±100	μA
I _{HOLD}	Bus Hold current D inputs ⁶	V _{CC} = 2.5V; V _I = 0.7V			100		μA
		V _{CC} = 2.5V; V _I = 1.7V			-70		μA
I _{EX}	Current into an output in the High state when V _O > V _{CC}	V _O = 5.5V; V _{CC} = 2.5V			10	125	μA
I _{PU/PD}	Power up/down 3-State output current ³	V _{CC} ≤ 1.2V; V _O = 0.5V to V _{CC} ; V _I = GND or V _{CC} ; OE/OE = Don't care			1	±100	μA
I _{OZH}	3-State output High current	V _{CC} = 2.7V; V _O = 2.3V; V _I = V _{IL} or V _{IH}			0.5	5	μA
I _{OZL}	3-State output Low current	V _{CC} = 2.7V; V _O = 0.5V; V _I = V _{IL} or V _{IH}			0.5	-5	μA
I _{CCH}	Quiescent supply current	V _{CC} = 2.7V; Outputs High, V _I = GND or V _{CC} , I _O = 0			0.04	0.1	mA
I _{CCL}		V _{CC} = 2.7V; Outputs Low, V _I = GND or V _{CC} , I _O = 0			2.7	4.5	
I _{CCZ}		V _{CC} = 2.7V; Outputs Disabled; V _I = GND or V _{CC} , I _O = 0 ⁵			0.04	0.1	
ΔI _{CC}	Additional supply current per input pin ²	V _{CC} = 2.3V to 2.7V; One input at V _{CC} -0.6V, Other inputs at V _{CC} or GND			0.04	0.4	mA

NOTES:

- All typical values are at V_{CC} = 2.5V and T_{amb} = 25°C.
- This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND.
- This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From V_{CC} = 1.2V to V_{CC} = 2.5V ± 0.2V a transition time of 100μsec is permitted. This parameter is valid for T_{amb} = 25°C only.
- Unused pins at V_{CC} or GND.
- I_{CCZ} is measured with outputs pulled up to V_{CC} or pulled down to ground.
- Not guaranteed.
- For valid test results, data must not be loaded into the flip-flops (or latches) after applying power.

2.5V/3.3V 18-bit bus-interface D-type flip-flop with reset and enable with 30Ω termination resistors (3-State)

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AC CHARACTERISTICS (2.5V ± 0.2V RANGE)

GND = 0V, $t_R = t_F = 2.5\text{ns}$, $C_L = 50\text{pF}$, $R_L = 500\Omega$

SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			T _{amb} = −40°C to +85°C V _{CC} = +2.5V ±0.2V			
			MIN	TYP	MAX	
f _{MAX}	Maximum clock frequency	1				MHz
t _{PLH} t _{PHL}	Propagation delay nCP to nQx	1	2.5 2.0	4.2 3.4	6.3 5.0	ns
t _{PHL}	Propagation delay nMR to nQx	2	2.0	3.4	4.6	ns
t _{PZH} t _{PZL}	Output enable time to High and Low level	4 5	3.0 2.0	4.8 3.2	7.6 5.2	ns
t _{PHZ} t _{PLZ}	Output disable time from High and Low level	4 5	2.5 2.0	4.4 3.3	6.7 5.2	ns

AC SETUP REQUIREMENTS (2.5V ± 0.2V RANGE)

GND = 0V, $t_R = t_F = 2.5\text{ns}$, $C_L = 50\text{pF}$, $R_L = 500\Omega$

SYMBOL	PARAMETER	WAVEFORM	LIMITS		UNIT
			$T_{\text{amb}} = -40 \text{ to } +85^{\circ}\text{C}$ $V_{\text{CC}} = +2.5\text{V} \pm 0.2\text{V}$		
			MIN	TYP	
$t_{\text{S}}(\text{H})$ $t_{\text{S}}(\text{L})$	Setup time, High or Low nDx to nCP	3	1.0 2.0	0.6 1.4	ns
$t_{\text{h}}(\text{H})$ $t_{\text{h}}(\text{L})$	Hold time, High or Low nDx to nCP	3	0.1 0.1	−1.5 −0.6	ns
$t_{\text{w}}(\text{H})$ $t_{\text{w}}(\text{L})$	nCP pulse width High or Low	1	2.0 3.0	0.8 2.1	ns
$t_{\text{S}}(\text{H})$ $t_{\text{S}}(\text{L})$	Setup time, High or Low nCE to nCP	3	1.0 0.5	0.2 −0.2	ns
$t_{\text{h}}(\text{H})$ $t_{\text{h}}(\text{L})$	Hold time, High or Low nCE to nCP	3	1.0 1.0	0.2 −0.1	ns
$t_{\text{w}}(\text{L})$	nMR pulse width, Low	2	2.5	1.6	ns
t_{rec}	Recovery time nMR to nCP	2	2.3	1.7	ns

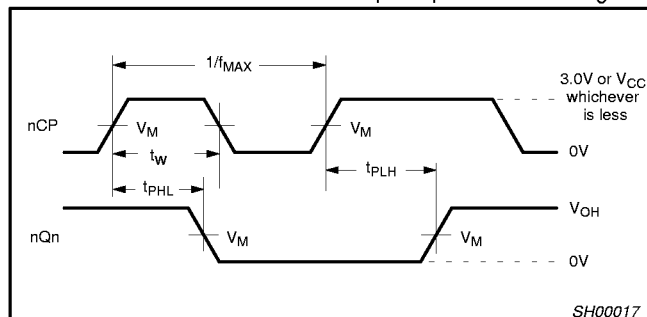
2.5V/3.3V 18-bit bus-interface D-type flip-flop with reset and enable with 30Ω termination resistors (3-State)

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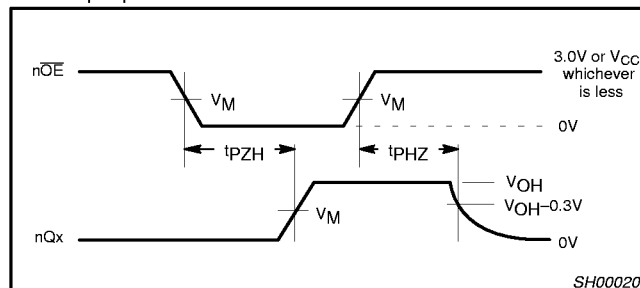
AC WAVEFORMS

For all waveforms, $V_M = 1.5V$ or $V_{CC}/2$ whichever is less

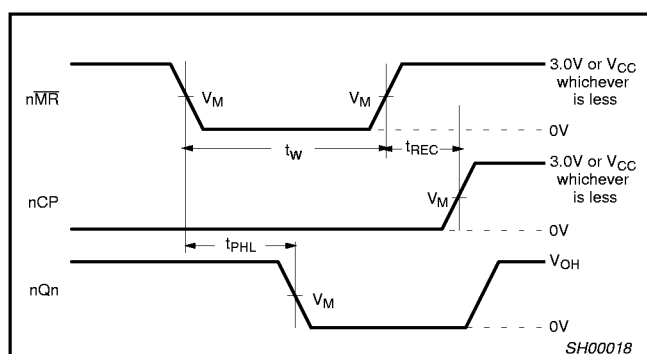
The shaded areas indicate when the input is permitted to change for predictable output performance.



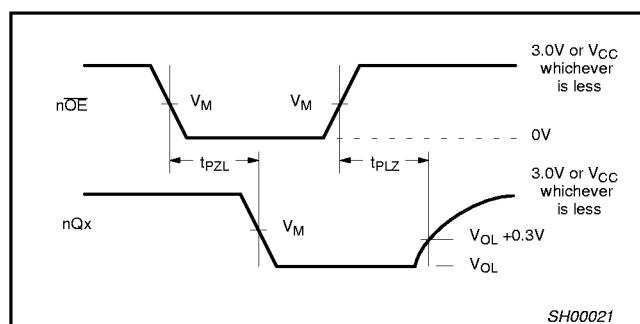
Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency



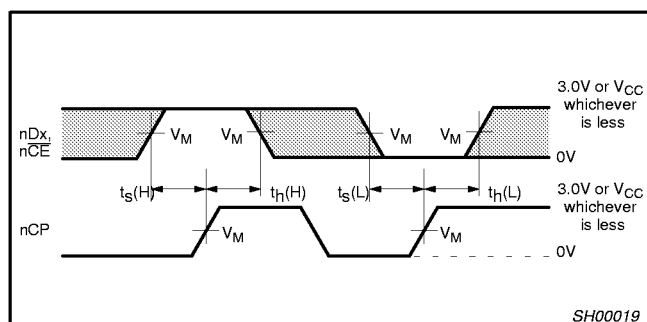
Waveform 4. 3-State Output Enable Time to High Level and Output Disable Time from High Level



Waveform 2. Master Reset Pulse Width, Master Reset to Output Delay and Master Reset to Clock Recovery Time



Waveform 5. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

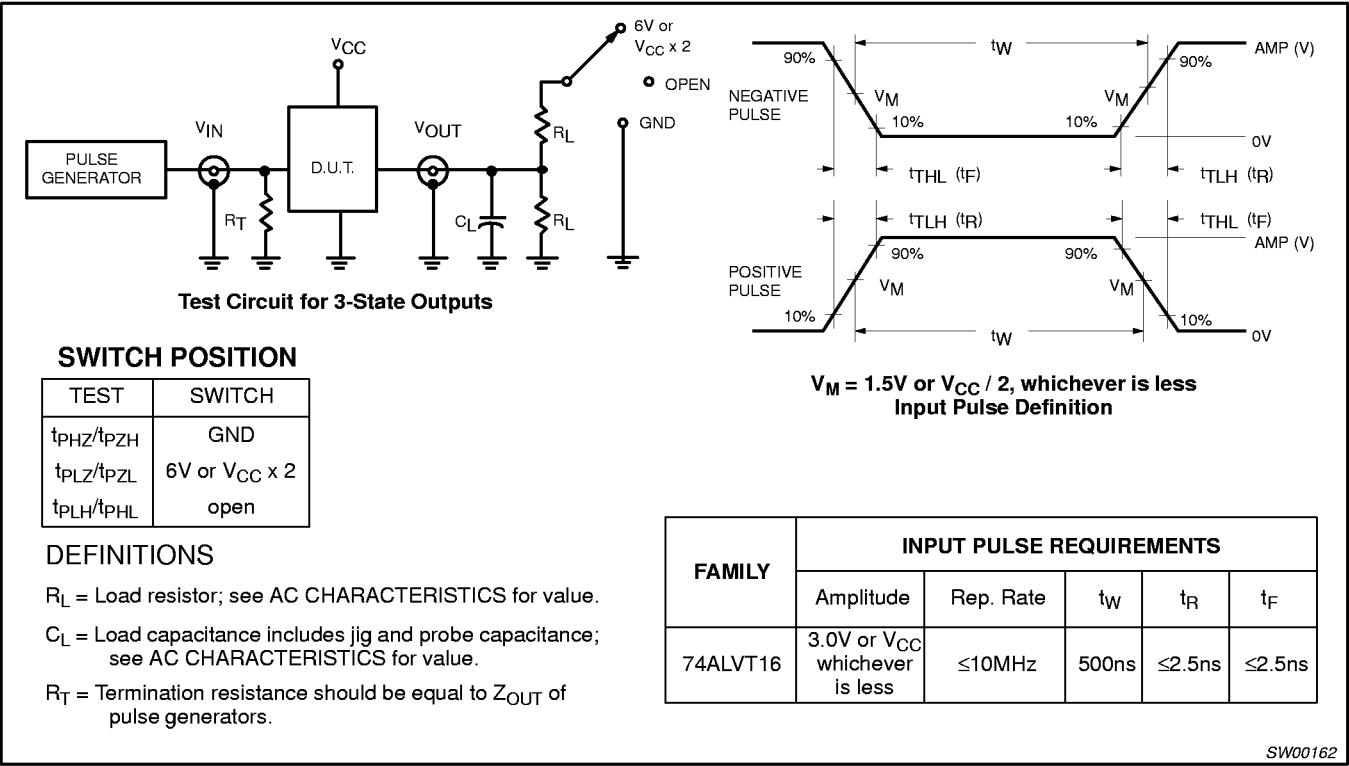


Waveform 3. Data Setup and Hold Times

2.5V/3.3V 18-bit bus-interface D-type flip-flop with reset
and enable with 30Ω termination resistors (3-State)

74ALVT162823

TEST CIRCUIT AND WAVEFORM



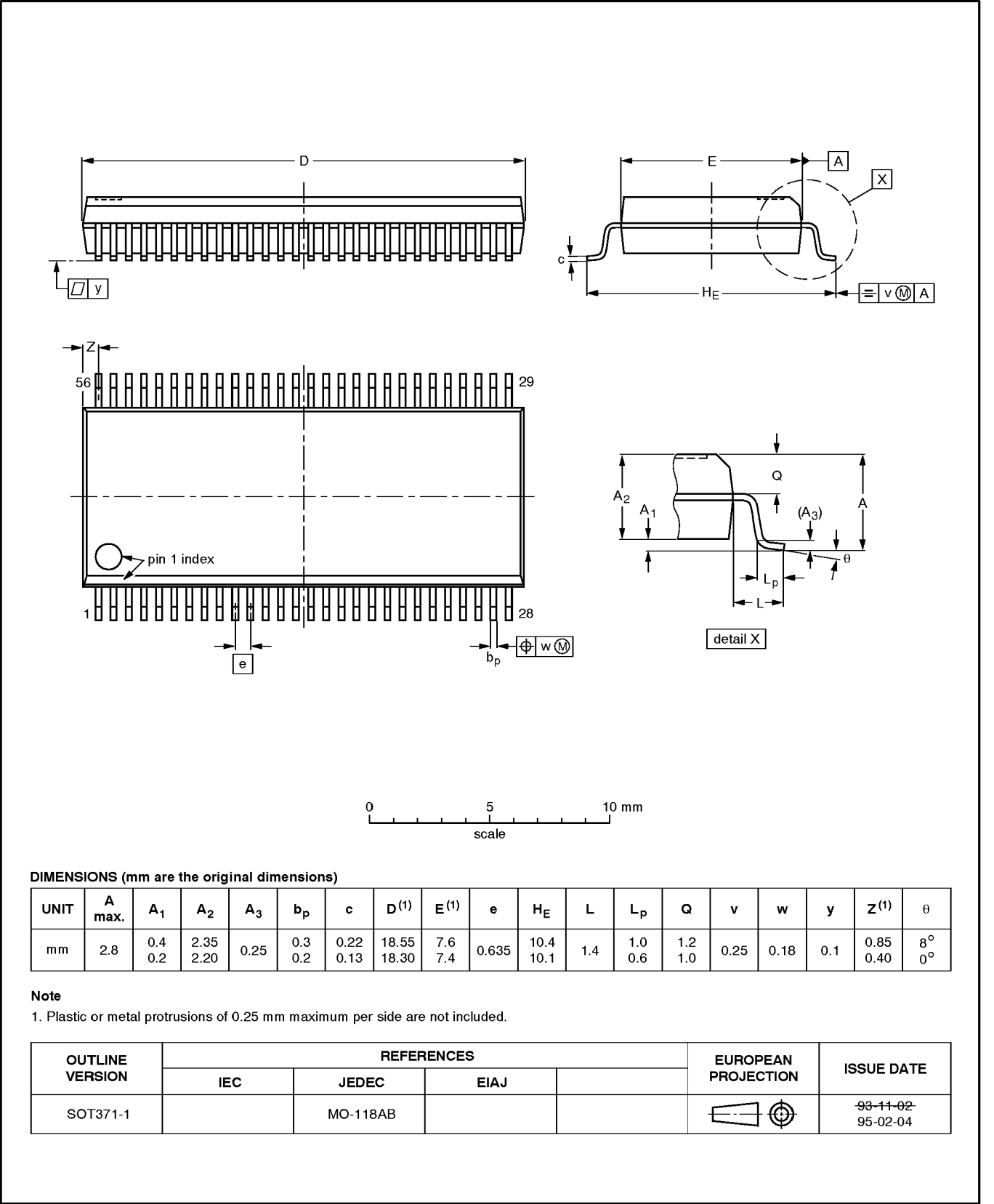
SW00162

18-bit bus-interface D-type flip-flop with reset and enable with 30Ω termination resistors (3-State)

74ALVT162823

SSOP56: plastic shrink small outline package; 56 leads; body width 7.5 mm

SOT371-1



18-bit bus-interface D-type flip-flop with reset and enable with 30Ω termination resistors (3-State)

74ALVT162823

TSSOP56: plastic thin shrink small outline package; 56 leads; body width 6.1mm

SOT364-1

