

2.5V/3.3V 16-bit registered transceiver (3-State)

74ALVT16952

FEATURES

- Two 8-bit registered transceivers
- 5V I/O Compatible
- 3-State buffers
- Output capability: +64mA/−32mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5V supply
- Bus hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power-up 3-State
- Power-up reset
- No bus current loading when output is tied to 5V bus
- Latch-up protection exceeds 500mA per JEDEC Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

DESCRIPTION

The 74ALVT16952 is a high-performance BiCMOS product designed for V_{CC} operation at 2.5V or 3.3V with I/O compatibility up to 5V.

The 74ALVT16952 is a dual octal registered transceiver. Two 8-bit registers store data flowing in both directions between two bidirectional buses. Data applied to the inputs is entered and stored on the rising edge of the Clock ($nCPXX$) provided that the Clock Enable ($nCEXX$) is Low. The data is then present at the 3-State output buffers, but is only accessible when the Output Enable ($nOEXX$) is Low. Data flow from A inputs to B outputs is the same as for B inputs to A outputs.

Active bus hold circuitry is provided to hold unused or floating data inputs at a valid logic level.

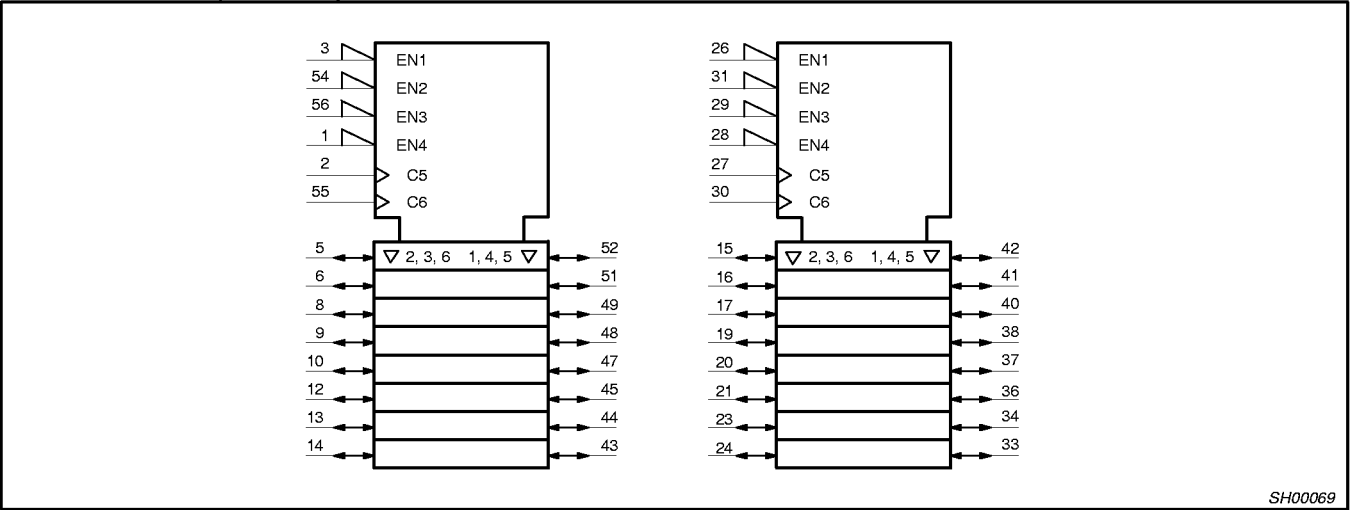
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS $T_{amb} = 25^{\circ}C$; $GND = 0V$	TYPICAL		UNIT
			2.5V	3.3V	
t_{PLH} t_{PHL}	Propagation delay $nCPBA$ to nAx or $nCPAB$ to nBx	$C_L = 50pF$;	3.0 3.0	2.3 2.3	ns
C_{IN}	Input capacitance	$V_I = 0V$ or V_{CC}	3	3	pF
$C_{I/O}$	I/O pin capacitance	$V_{I/O} = 0V$ or V_{CC} Outputs disabled	9	9	pF
I_{CCZ}	Total supply current	Outputs disabled	40	70	μA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
56-Pin Plastic SSOP Type III	−40°C to +85°C	74ALVT16952 DL	AV16952 DL	SOT371-1
56-Pin Plastic TSSOP Type II	−40°C to +85°C	74ALVT16952 DGG	AV16952 DGG	SOT364-1

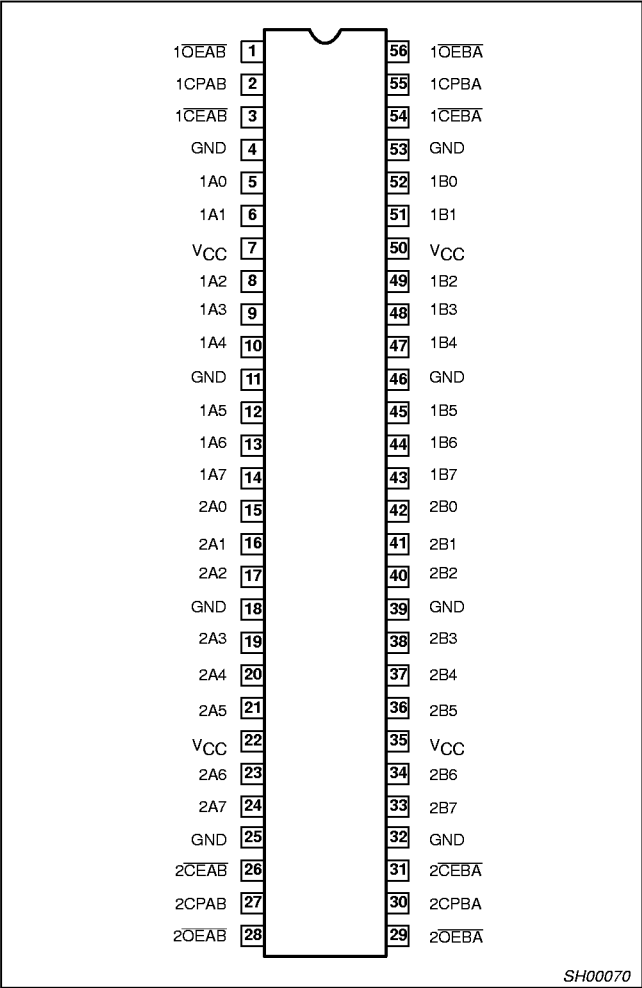
LOGIC SYMBOL (IEEE/IEC)



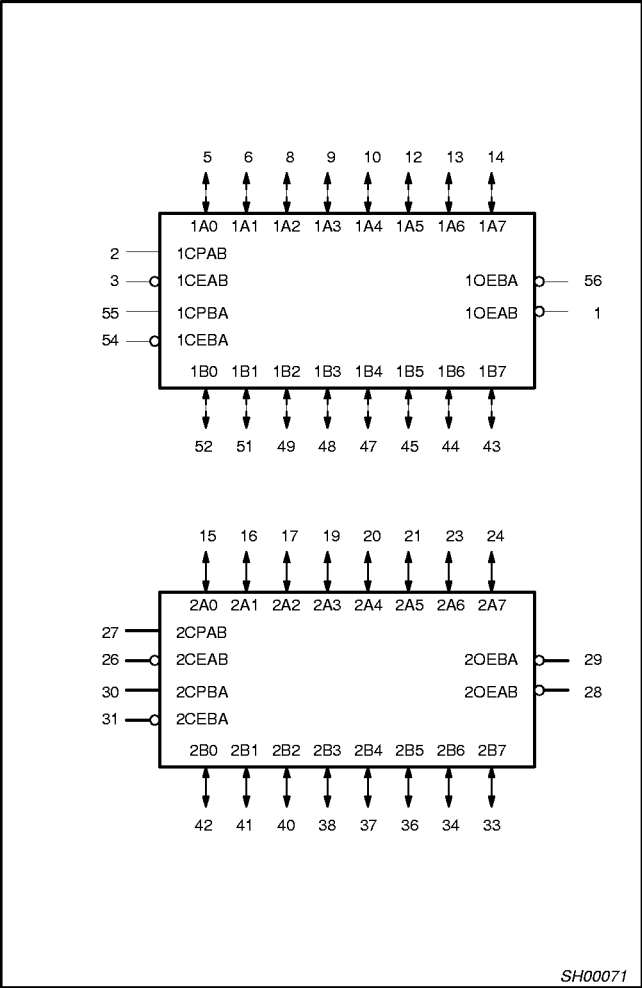
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PIN CONFIGURATION



LOGIC SYMBOL



PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
2, 55 27, 30	1CPAB / 1CPBA 2CPAB / 2CPBA	Clock input A to B / Clock input B to A
3, 54, 26, 31	1CEAB / 1CEBA 2CEAB / 2CEBA	Clock enable input A to B / Clock enable input B to A
5, 6, 8, 9, 10, 12, 13, 14, 15, 16, 17, 19, 20, 21, 23, 24	1A0 – 1A7 2A0 – 2A7	Data inputs/outputs (A side)
52, 51, 49, 48, 47, 45, 44, 43 42, 41, 40, 38, 37, 36, 34, 33	1B0 – 1B7 2B0 – 2B7	Data inputs/outputs (B side)
1, 56 28, 29	1OEAB / 1OEBA 2OEAB / 2OEBA	Output enable inputs
4, 11, 18, 25, 32, 39, 46, 53	GND	Ground (0V)
7, 22, 35, 50	VCC	Positive supply voltage

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FUNCTION TABLE for Register nAx or nBx

INPUTS			INTERNAL Q	OPERATING MODE
nAx or nBx	nCPXX	nCEXX		
X	X	H	NC	Hold data
L H	↑ ↑	L L	L H	Load data

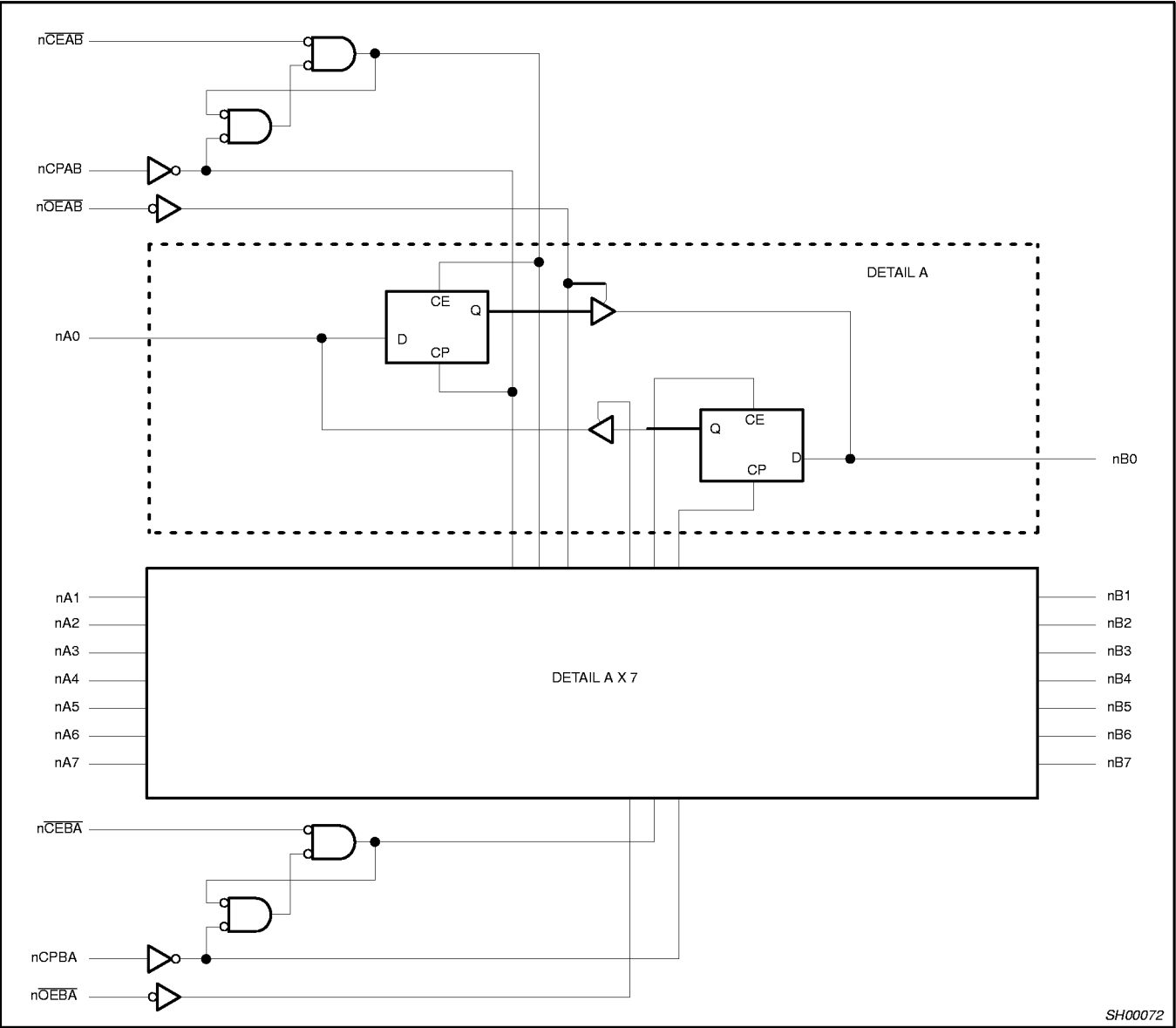
H = High voltage level
L = Low voltage level
↑ = Low-to-High transition
X = Don't care
XX = AB or BA
NC = No change

FUNCTION TABLE for Output Enable

INPUTS		INTERNAL Q	nAx or nBx OUTPUTS	OPERATING MODE
nOEXX				
H		X	Z	Disable outputs
L L		L H	L H	Enable outputs

H = High voltage level
L = Low voltage level
X = Don't care
XX = AB or BA
Z = High impedance "off" state

LOGIC DIAGRAM



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ABSOLUTE MAXIMUM RATINGS^{1, 2}

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		-0.5 to +4.6	V
I_{IK}	DC input diode current	$V_I < 0$	-50	mA
V_I	DC input voltage ³		-0.5 to +7.0	V
I_{OK}	DC output diode current	$V_O < 0$	-50	mA
V_{OUT}	DC output voltage ³	output in Off or High state	-0.5 to +7.0	V
I_{OUT}	DC output current	output in Low state output in High state	128 -64	mA
T_{stg}	Storage temperature range		-65 to +150	°C

NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	2.5V RANGE LIMITS		3.3V RANGE LIMITS		UNIT
		MIN	MAX	MIN	MAX	
V_{CC}	DC supply voltage	2.3	2.7	3.0	3.6	V
V_I	Input voltage	0	5.5	0	5.5	V
V_{IH}	High-level input voltage	1.7		2.0		V
V_{IL}	Input voltage		0.7		0.8	V
I_{OH}	High-level output current		-8		-32	mA
I_{OL}	Low-level output current		8		32	mA
	Low-level output current; current duty cycle $\leq 50\%$; $f \geq 1\text{kHz}$		24		64	
$\Delta t/\Delta v$	Input transition rise or fall rate; Outputs enabled		10		10	ns/V
T_{amb}	Operating free-air temperature range	-40	+85	-40	+85	°C

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DC ELECTRICAL CHARACTERISTICS (3.3V $\pm$ 0.3V RANGE)

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS			UNIT
				Temp = -40°C to +85°C			
				MIN	TYP ¹	MAX	
V _{IK}	Input clamp voltage	V _{CC} = 3.0V; I _{IK} = -18mA			-0.85	-1.2	V
V _{OH}	High-level output voltage	V _{CC} = 3.0 to 3.6V; I _{OH} = -100μA		V _{CC} -0.2	V _{CC}		V
		V _{CC} = 3.0V; I _{OH} = -32mA		2.0	2.3		
V _{OL}	Low-level output voltage	V _{CC} = 3.0V; I _{OL} = 100μA			0.07	0.2	V
		V _{CC} = 3.0V; I _{OL} = 16mA			0.25	0.4	
		V _{CC} = 3.0V; I _{OL} = 32mA			0.3	0.5	
		V _{CC} = 3.0V; I _{OL} = 64mA			0.4	0.55	
I _I	Input leakage current	V _{CC} = 3.6V; V _I = V _{CC} or GND	Control pins		0.1	±1	μA
		V _{CC} = 0 or 3.6V; V _I = 5.5V			0.1	10	
		V _{CC} = 3.6V; V _I = 5.5V	Data pins ⁴		0.1	10	
		V _{CC} = 3.6V; V _I = V _{CC}			0.1	1	
		V _{CC} = 3.6V; V _I = 0			0.1	-5	
I _{OFF}	Off current	V _{CC} = 0V; V _I or V _O = 0 to 4.5V			0.1	±100	μA
I _{HOLD}	Bus Hold current	V _{CC} = 3V; V _I = 0.8V		75	120		μA
	A or B inputs	V _{CC} = 3V; V _I = 2.0V		-75	-130		μA
I _{EX}	Current into an output in the High state when V _O > V _{CC}	V _O = 5.5V; V _{CC} = 3.0V			50	125	μA
I _{PU/PD}	Power up/down 3-State output current ³	V _{CC} ≤ 1.2V; V _O = 0.5V to V _{CC} ; V _I = GND or V _{CC} ; OE/OE = Don't care			40	±100	μA
I _{CCH}	Quiescent supply current	V _{CC} = 3.6V; Outputs High, V _I = GND or V _{CC} , I _O = 0			0.07	0.1	mA
I _{CCL}		V _{CC} = 3.6V; Outputs Low, V _I = GND or V _{CC} , I _O = 0			3.5	5	
I _{CCZ}		V _{CC} = 3.6V; Outputs Disabled; V _I = GND or V _{CC} , I _O = 0 ⁵			0.07	0.1	
ΔI _{CC}	Additional supply current per input pin ²	V _{CC} = 3V to 3.6V; One input at V _{CC} -0.6V, Other inputs at V _{CC} or GND			0.04	0.4	mA

NOTES:

1. All typical values are at $V_{CC} = 3.3V$ and $T_{amb} = 25^\circ C$.
2. This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND.
3. This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From $V_{CC} = 1.2V$ to $V_{CC} = 3.3V \pm 0.3V$ a transition time of 100 μsec is permitted. This parameter is valid for $T_{amb} = 25^\circ C$ only.
4. Unused pins at V_{CC} or GND.
5. I_{CCZ} is measured with outputs pulled up to V_{CC} or pulled down to ground.

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AC CHARACTERISTICS (3.3V $\pm$ 0.3V RANGE)GND = 0V; $t_R = t_F = 2.5\text{ns}$; $C_L = 50\text{pF}$; $R_L = 500\Omega$; $T_{\text{amb}} = -40^\circ\text{C}$ to $+85^\circ\text{C}$

SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			V _{CC} = 3.3V ±0.3V			
			MIN	TYP ¹	MAX	
f _{MAX}	Maximum clock frequency	1	100	142		MHz
t _{PLH} t _{PHL}	Propagation delay nCPBA to nAx, nCPAB to nBx	1	1.0 1.0	2.3 2.3	3.5 3.4	ns
t _{PZH} t _{PZL}	Output enable time nOEBA to nAx, nOEAB to nBx	3 4	1.0 0.5	2.4 1.8	3.8 3.0	ns
t _{PHZ} t _{PLZ}	Output disable time nOEBA to nAx, nOEAB to nBx	3 4	1.0 1.0	2.9 2.3	4.5 3.6	ns

NOTES:1. All typical values are at $V_{CC} = 3.3V$ and $T_{\text{amb}} = 25^\circ\text{C}$ **AC SETUP REQUIREMENTS (3.3V $\pm$ 0.3V RANGE)**GND = 0V; $t_R = t_F = 2.5\text{ns}$; $C_L = 50\text{pF}$; $R_L = 500\Omega$; $T_{\text{amb}} = -40^\circ\text{C}$ to $+85^\circ\text{C}$

SYMBOL	PARAMETER	WAVEFORM	LIMITS		UNIT
			V _{CC} = 3.3V ±0.3V		
			MIN	TYP	
t _S (H) t _S (L)	Setup time nAx to nCPAB or nBx to nCPBA	2	1.5 1.5	0.9 0.7	ns
t _H (H) t _H (L)	Hold time nAx to nCPAB or nBx to nCPBA	2	0.5 0.5	−0.6 −0.8	ns
t _S (H) t _S (L)	Setup time nCEAB to nCPAB, nCEBA to nCPBA	2	1.1 0.5	0.2 −0.6	ns
t _H (H) t _H (L)	Hold time nCEAB to nCPAB, nCEBA to nCPBA	2	1.5 1.0	0.6 −0.1	ns
t _W (H) t _W (L)	nCPAB or nCPBA pulse width, High or Low	1	3.2 3.2	2.7 2.5	ns

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DC ELECTRICAL CHARACTERISTICS (2.5V $\pm$ 0.2V RANGE)

SYMBOL	PARAMETER	TEST CONDITIONS		LIMITS			UNIT
				Temp = -40°C to +85°C			
				MIN	TYP ¹	MAX	
V _{IK}	Input clamp voltage	V _{CC} = 2.3V; I _{IK} = -18mA			-0.85	-1.2	V
V _{OH}	High-level output voltage	V _{CC} = 2.3 to 3.6V; I _{OH} = -100μA		V _{CC} -0.2	V _{CC}		V
		V _{CC} = 2.3V; I _{OH} = -8mA		1.8	2.1		
V _{OL}	Low-level output voltage	V _{CC} = 2.3V; I _{OL} = 100μA			0.07	0.2	V
		V _{CC} = 2.3V; I _{OL} = 24mA			0.3	0.5	
		V _{CC} = 2.3V; I _{OL} = 8mA			0.3	0.4	
I _I	Input leakage current	V _{CC} = 2.7V; V _I = V _{CC} or GND	Control pins		0.1	±1	μA
		V _{CC} = 0 or 2.7V; V _I = 5.5V			0.1	10	
		V _{CC} = 2.7V; V _I = 5.5V	Data pins ⁴		0.1	10	
		V _{CC} = 2.7V; V _I = V _{CC}			0.1	1	
		V _{CC} = 2.7V; V _I = 0			0.1	-5	
I _{OFF}	Off current	V _{CC} = 0V; V _I or V _O = 0 to 4.5V			0.1	±100	μA
I _{HOLD}	Bus Hold current	V _{CC} = 2.5V; V _I = 0.7V			110		μA
	A or B inputs ⁶	V _{CC} = 2.5V; V _I = 1.7V			-6		μA
I _{EX}	Current into an output in the High state when V _O > V _{CC}	V _O = 5.5V; V _{CC} = 2.3V			50	125	μA
I _{PU/PD}	Power up/down 3-State output current ³	V _{CC} ≤ 1.2V; V _O = 0.5V to V _{CC} ; V _I = GND or V _{CC} ; OE/OE = Don't care			40	100	μA
I _{CCH}	Quiescent supply current	V _{CC} = 2.7V; Outputs High, V _I = GND or V _{CC} , I _O = 0			0.04	0.1	mA
I _{CCL}		V _{CC} = 2.7V; Outputs Low, V _I = GND or V _{CC} , I _O = 0			2.5	4.5	
I _{CCZ}		V _{CC} = 2.7V; Outputs Disabled; V _I = GND or V _{CC} , I _O = 0 ⁵			0.04	0.1	
ΔI _{CC}	Additional supply current per input pin ²	V _{CC} = 2.3V to 2.7V; One input at V _{CC} -0.6V, Other inputs at V _{CC} or GND			0.01	0.4	mA

NOTES:

1. All typical values are at V_{CC} = 2.5V and T_{amb} = 25°C.
2. This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND.
3. This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From V_{CC} = 1.2V to V_{CC} = 2.5V $\pm$ 0.3V a transition time of 100 μ sec is permitted. This parameter is valid for T_{amb} = 25°C only.
4. Unused pins at V_{CC} or GND.
5. I_{CCZ} is measured with outputs pulled up to V_{CC} or pulled down to ground.
6. Bus hold current is not specified below V_{CC} =

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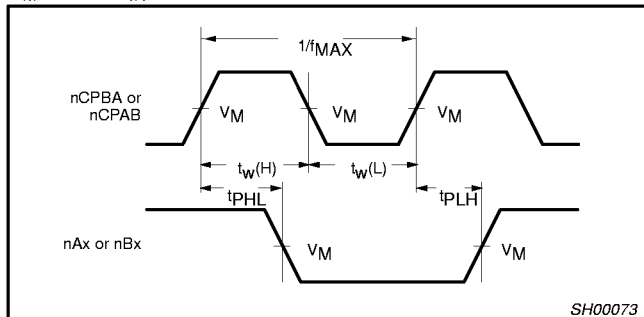
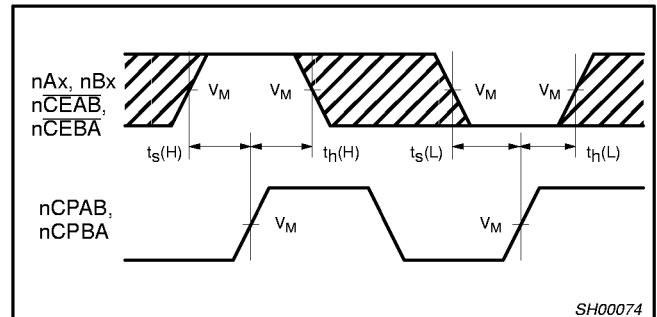
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AC CHARACTERISTICS (2.5V $\pm$ 0.2V RANGE)GND = 0V; $t_R = t_F = 2.5\text{ns}$; $C_L = 50\text{pF}$; $R_L = 500\Omega$; $T_{\text{amb}} = -40^\circ\text{C}$ to $+85^\circ\text{C}$

SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			V _{CC} = 2.5V ±0.2V			
			MIN	TYP ¹	MAX	
f _{MAX}	Maximum clock frequency	1	125	156		MHz
t _{PLH} t _{PHL}	Propagation delay nCPBA to nAx, nCPAB to nBx	1	1.0 1.0	3.0 3.0	3.8 3.9	ns
t _{PZH} t _{PZL}	Output enable time nOEBA to nAx, nOEAB to nBx	3 4	1.0 0.5	3.5 2.5	5.0 3.7	ns
t _{PHZ} t _{PLZ}	Output disable time nOEBA to nAx, nOEAB to nBx	3 4	1.0 1.0	3.9 3.1	4.8 4.1	ns

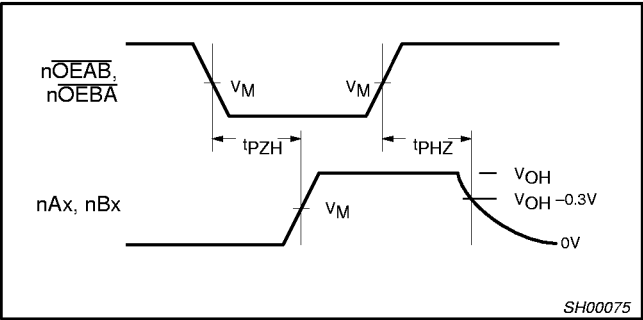
NOTES:1. All typical values are at $V_{CC} = 2.5\text{V}$ and $T_{\text{amb}} = 25^\circ\text{C}$ **AC SETUP REQUIREMENTS (2.5V $\pm$ 0.2V RANGE)**GND = 0V; $t_R = t_F = 2.5\text{ns}$; $C_L = 50\text{pF}$; $R_L = 500\Omega$; $T_{\text{amb}} = -40^\circ\text{C}$ to $+85^\circ\text{C}$

SYMBOL	PARAMETER	WAVEFORM	LIMITS		UNIT
			V _{CC} = 2.5V ±0.2V		
			MIN	TYP	
t _S (H) t _S (L)	Setup time nAx to nCPAB or nBx to nCPBA	2	1.5 2.0	0.8 1.2	ns
t _H (H) t _H (L)	Hold time nAx to nCPAB or nBx to nCPBA	2	0.5 0.5	−1.2 −0.8	ns
t _S (H) t _S (L)	Setup time nCEAB to nCPAB, nCEBA to nCPBA	2	1.0 1.0	0.0 −0.2	ns
t _H (H) t _H (L)	Hold time nCEAB to nCPAB, nCEBA to nCPBA	2	1.1 1.1	0.3 0.2	ns
t _W (H) t _W (L)	nCPAB or nCPBA pulse width, High or Low	1	3.2 2.0	2.7 1.5	ns

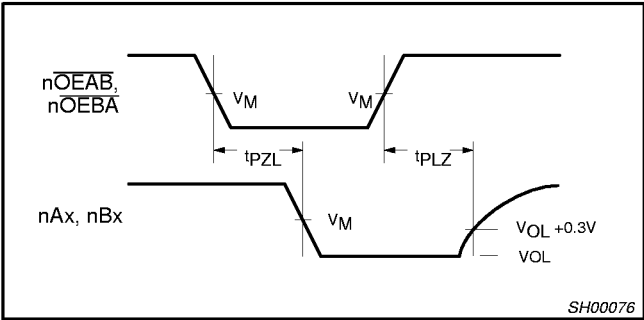
AC WAVEFORMS $V_M = 1.5\text{V}$, $V_{\text{IN}} = \text{GND to } 3.0\text{V}$ **Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency****Waveform 2. Data Setup and Hold Times**

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Waveform 3. 3-State Output Enable Time to High Level and Output Disable Time from High Level



Waveform 4. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

TEST CIRCUIT AND WAVEFORMS

Test Circuit for 3-State Outputs

SWITCH POSITION

TEST	SWITCH
t_{PLZ}/t_{PZL}	6V or $V_{CC} \times 2$
t_{PLH}/t_{PHL}	Open
t_{PHZ}/t_{PZH}	GND

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance: See AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

Input Pulse Waveforms

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74ALVT16	3.0V or V_{CC} whichever is less	$\leq 10\text{MHz}$	500ns	$\leq 2.5\text{ns}$	$\leq 2.5\text{ns}$

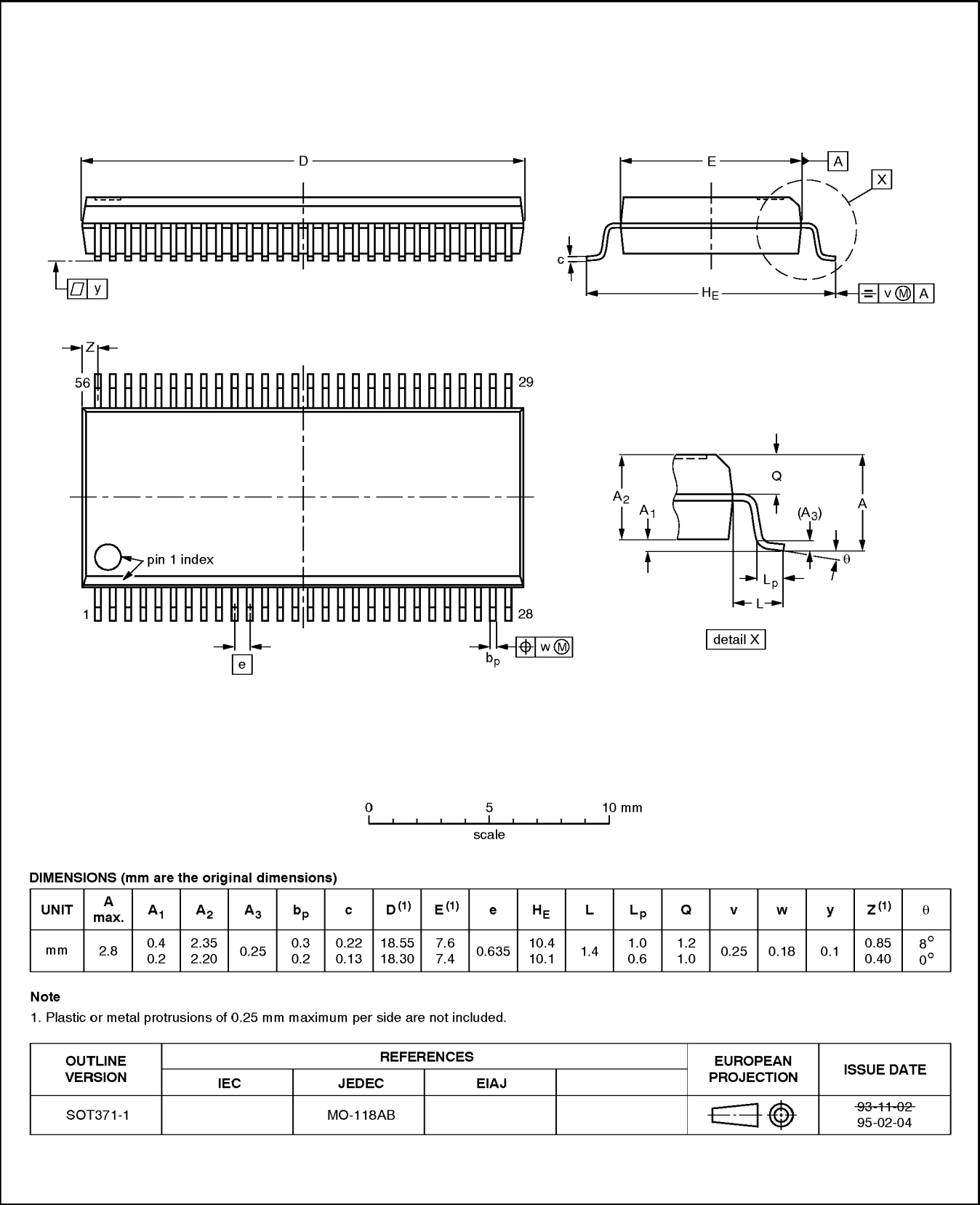
SW00025

2.5V/3.3V ALVT 16-bit registered transceiver
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SSOP56: plastic shrink small outline package; 56 leads; body width 7.5 mm

SOT371-1



2.5V/3.3V ALVT 16-bit registered transceiver (3-State)

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TSSOP56: plastic thin shrink small outline package; 56 leads; body width 6.1mm

SOT364-1

