National Semiconductor

September 1995

CGS64/74B2529
500 ps 2 to 10 Minimum Skew Clock Driver

General Description

This minimum skew clock driver is designed for Clock Generation and Support (CGS) applications operating from 33 MHz to 80 MHz. The devices guarantee minimum output skew across the outputs of a given device.

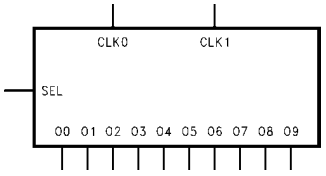
Skew parameters are also provided as a means to measure duty cycle requirements as those found in high speed clocking systems. The '2529 is a minimum skew clock driver with two selectable inputs driving ten outputs.

The SEL pin is used to determine which CLKn will have an active effect on the outputs of the circuit. When SEL = 1, the CLK1 input is selected and when SEL = 0, the CLK0 input is selected. The non-selected CLKn input will not have any effect on the logical output level of the circuit. The output pins act as a single entity and will follow the state of the CLK inputs.

Features

- Clock Generation and Support (CGS) devices
- Ideal for high frequency signal generation or clock distribution applications
- CGS74B version features National's Advanced Bipolar FAST® LSI process
- 2-to-10 low skew clock distribution
- 500 ps pin-to-pin output skew (V package)
- Specification for transition skew to meet duty cycle requirements
- 20-center pin V_{CC} and GND configuration or PLCC to minimize high speed switching noise
- Current sourcing 48 mA and current sinking of 64 mA
- Low dynamic power consumption above 20 MHz
- Guaranteed 4 kV ESD protection

Logic Symbols



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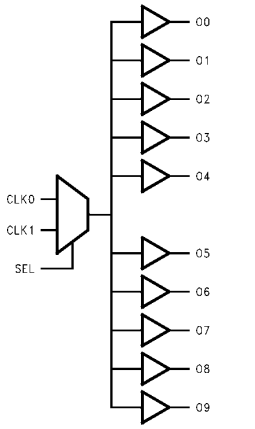

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Pin Description

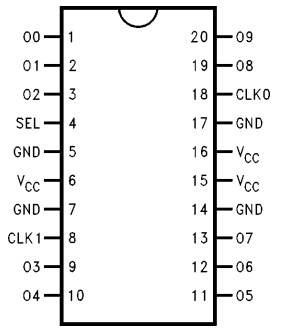
Pin Names	Description
CLK0, CLK1	Clock Input
O0–O9	Outputs
SEL	Clock Select

Inputs			Outputs
CLK0	CLK1	SEL	O0–O9
L	X	L	L
H	X	L	H
X	L	H	L
X	H	H	H

L = Low Logic Level
H = High Logic Level
X = Immaterial

Connection Diagrams

Pin Assignment SOIC



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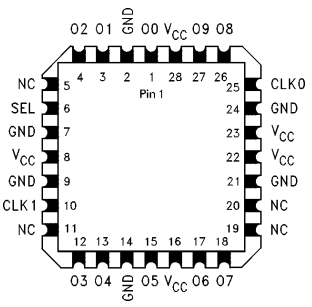
Pin Assignment for PLCC



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Absolute Maximum Ratings (Note)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage (V_{CC})	7.0V
Input Voltage (V_I)	7.0V
Operating Temperature	
64 Grade	−40°C to +85°C
74 Grade	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

Typical θ_{JA}	**Airflow**	**M**	**V**	
	0 LFM	89	64	°C/W
	225 LFM	71	52	°C/W
	500 LFM	63	45	°C/W

Recommended Operating Conditions

Supply Voltage (V_{CC})	4.5V to 5.5V
Input Rise and Fall Times (0.8V to 2.0V)	9.6 ns max
Free Air Operating Temperature (T_A)	
64 Grade	−40°C to +85°C
74 Grade	0°C to +70°C

Note: *The Absolule Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the DC and AC Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The Recommended Operating Conditions will define the conditions for actual device operation.*

DC Electrical Characteristics

Over recommended operating conditions unless specified otherwise. All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$

Symbol	Parameter	Conditions		Min	Typ	Max	Units
V_{IK}	Input Clamp Voltage	$V_{CC} = 4.5V$, $I_I = -18$ mA				−1.2	V
V_{IH}	Minimum Input High Level Voltage			2.0			V
V_{IL}	Maximum Input Low Level Voltage					0.8	V
V_{OH}	High Level Output Voltage	$I_{OH} = -3$ mA, $V_{CC} = 4.5V$		2.4			V
		$I_{OH} = 48$ mA, $V_{CC} = 4.5V$		2.0			
V_{OL}	Low Level Output Voltage	$V_{CC} = 4.5V$, $I_{OL} = 64$ mA			0.35	0.5	V
I_I	Input Current @ Max Input Voltage	$V_{CC} = 5.5V$, $V_{IH} = 7V$				0.1	mA
I_{IH}	High Level Input Current	$V_{CC} = 5.5V$, $V_{IH} = 2.7V$				20	μA
I_{IL}	Low Level Input Current	$V_{CC} = 5.5V$, $V_{IL} = 0.4V$			−0.5	−0.75	mA
I_O	Output Drive Current	$V_{CC} = 5.5V$, $V_O = 2.25V$		−50		−150	mA
I_{CC}	Supply Current '2529	$V_{CC} = 5.5V$	Outputs High		24	35	mA
			Outputs Low		45	65	mA
C_{IN}	Input Capacitance	$V_{CC} = 5.5V$			5		pF

AC Electrical Characteristics

Over recommended operating conditions unless specified otherwise. All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$

Symbol	Parameter		$V_{CC} = 4.5V$ to $5.5V$ $C_L = 50$ pF $R_L = 500\Omega$			Units
			Min	Typ	Max	
f_{MAX}	Frequency Maximum			80		MHz
t_{PLH}	Low-to-High Propagation Delay CLK0,1 to O_n	M	3.0	5.5	7.0	ns
	Low-to-High Propagation Delay CLK0,1 to O_n	V	2.5	5.5	6.0	
t_{PHL}	High-to-Low Propagation Delay CLK0,1 to O_n	M	3.0	5.5	7.0	ns
	High-to-Low Propagation Delay CLK0,1 to O_n	V	2.5	5.5	6.0	

Extended AC Electrical Characteristics

Over recommended operating conditions unless specified otherwise. All typical values are measured at $V_{CC} = 5V$, $T_A = 25°C$

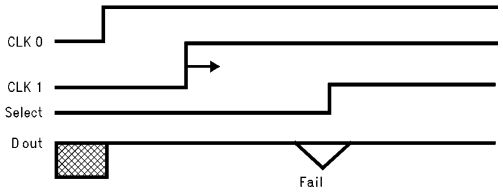
Symbol	Parameter	Package	$V_{CC} = 4.5V$ to $5.5V$ $C_L = 50$ pF $R_L = 500\Omega$			Units
			Min	Typ	Max	
t_{OSHL}	Maximum Skew Common Edge Output-to-Output Variation (Note 1)	M V			500 500	ps
t_{OSLH}	Maximum Skew Common Edge Output-to-Output Variation (Note 1)	M V			500 500	ps
t_{PS}	Maximum Skew Pin (Signal) Transition Variation (Note 1)	M V			750 850	ps
t_{Set} (Note 2)	Setup Time High Select to CLK0 or 1 Setup Time Low Select to CLK0 or 1	All	−2.0 −2.0			ns
t_{Hold} (Note 2)	Hold Time High Sel to CLK0 Hold Time High Sel to CLK1 Hold Time Low Sel to CLK0 Hold Time Low Sel to CLK1		5.0 5.0 8.0 8.0			ns
t_{rise}, t_{fail}	Rise/Fall Time (from 0.8V/2.0V to 2.0V/0.8V)	CGS74			1.5	ns
		CGS64			1.75	

Note 1: t_{OSHL} and t_{OSLH} are characterized and guaranteed by design @1 MHz.

Note 2: A negative setup time indicates that the correct logic levels may be initiated sometimes after the active transition of the timing pulse.

Timing Diagrams for the CGS64/74B2529

t_{Set}–High, CLK1



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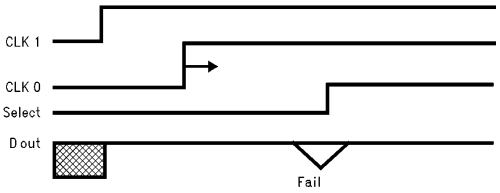
t_{Set}–High, CLK0



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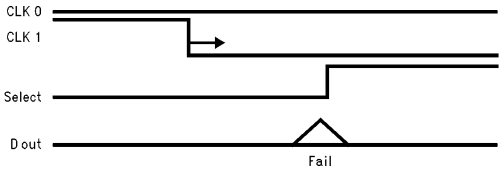
t_{Set}–Low, CLK1



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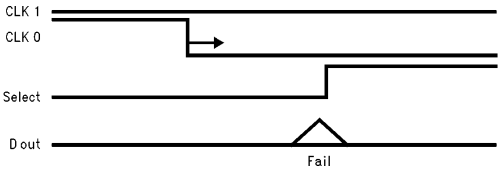
t_{Set}–Low, CLK0



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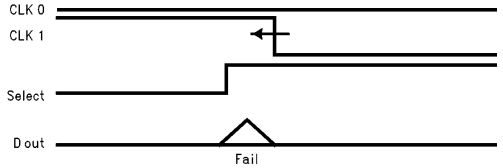
t_{Hold}–High, CLK1



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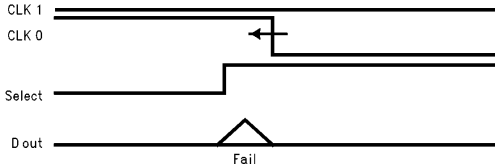
t_{Hold}–High, CLK0



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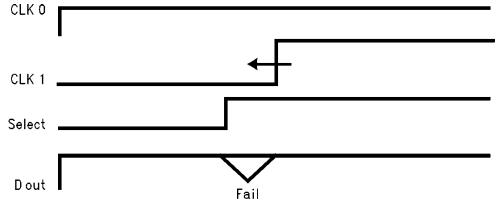
t_{Set}–Low, CLK1



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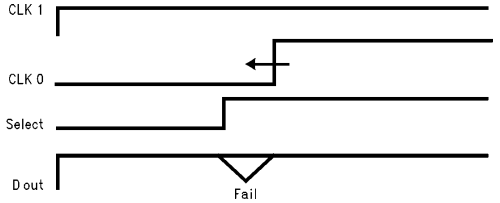
t_{Set}–Low, CLK0



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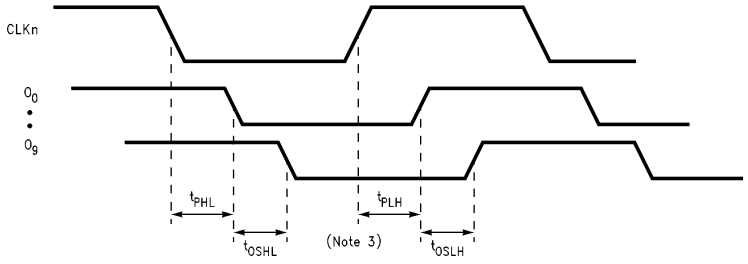
Timing Diagrams for the CGS64/74B2529 (Continued)



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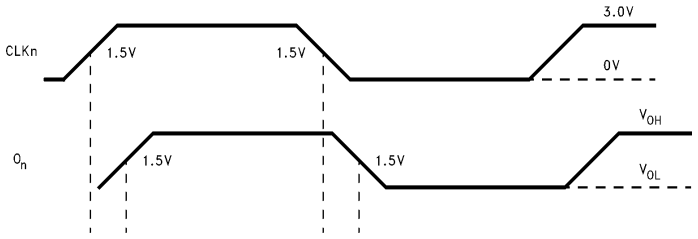

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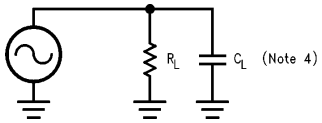
Test Circuit



R_L is 500Ω
C_L is 50 pF for all prop delays and skew measurements.

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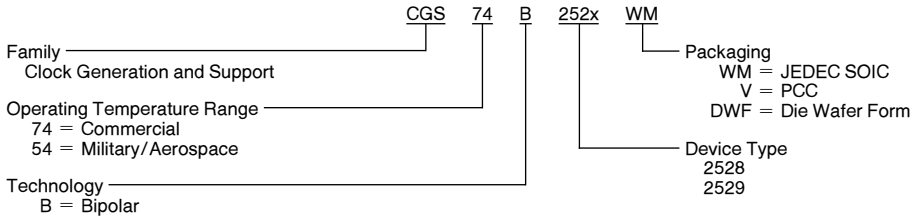
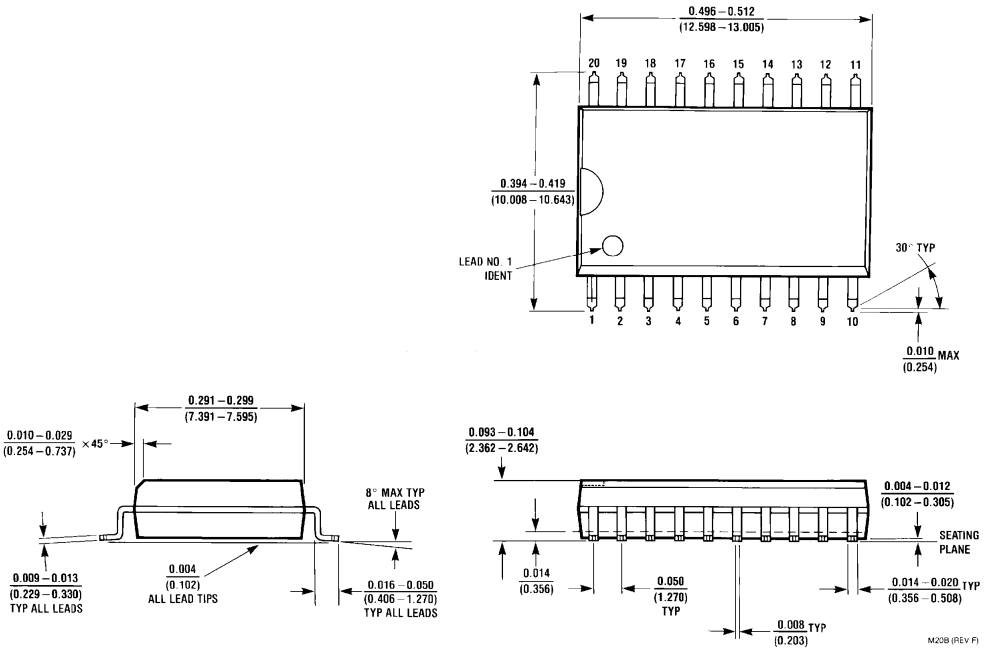
Note 3: Refer to Test Philosophy and Definitions, Minimum Skew Parameters Measurement Information for definitions of each skew specification, in section (TBD).

Note 4: Load Capacitance includes the test jig.

Ordering Information (Contact NSC Marketing for specific date of availability)

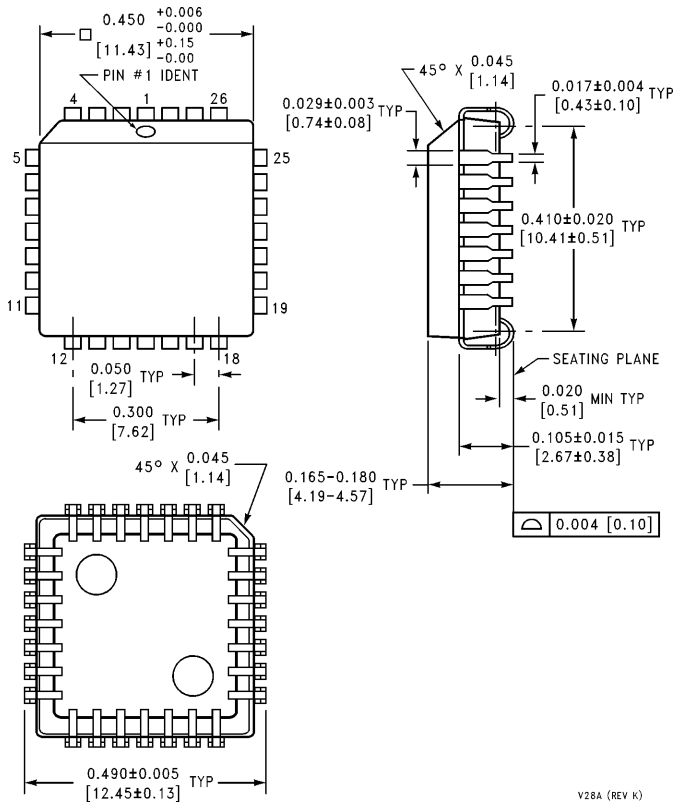


Physical Dimensions inches (millimeters) unless otherwise noted



20-Lead Molded Package (Small Outline 0.300 Wide) (WM)
NS Package Number M20B

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



28-Lead Molded Plastic Leaded Chip Carrier (PLCC)
NS Package Number V28A

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