National Semiconductor

74BCT2828A
10-Bit Buffer/Line Driver with 25Ω Series Resistors in the Outputs

General Description

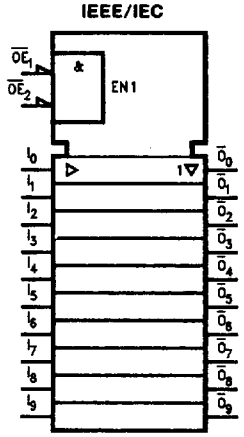
The 'BCT2828A 10-bit buffer and line driver provides high performance bus interface buffering for wide data/address paths or buses carrying parity. This device is designed to drive the capacitive inputs of MOS memory drivers, address drivers, clock drivers or bus-oriented transmitters/receivers. The 25Ω series resistors in the outputs reduce ringing and eliminate the need for external resistors.

Features

- 25Ω series resistors in outputs eliminate the need for external resistors
- Inverting buffers
- TRI-STATE® outputs drive bus lines or buffer memory address registers
- Low I_{CCZ} through BiCMOS techniques
- Guaranteed output skew
- Guaranteed multiple output switching specifications
- Guaranteed 4000V minimum ESD protection
- Guaranteed latchup protection
- Nondestructive hot insertion capability
- High impedance in power down (I_{ZZ} and V_{ID})

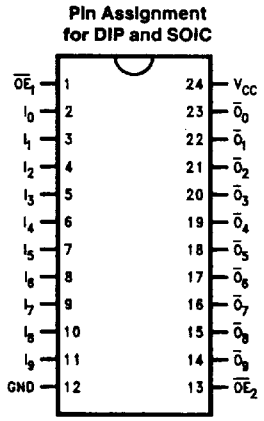
Ordering Code: See Section 11

Logic Symbol



TL/F/10917–1

Connection Diagram



TL/F/10917–2

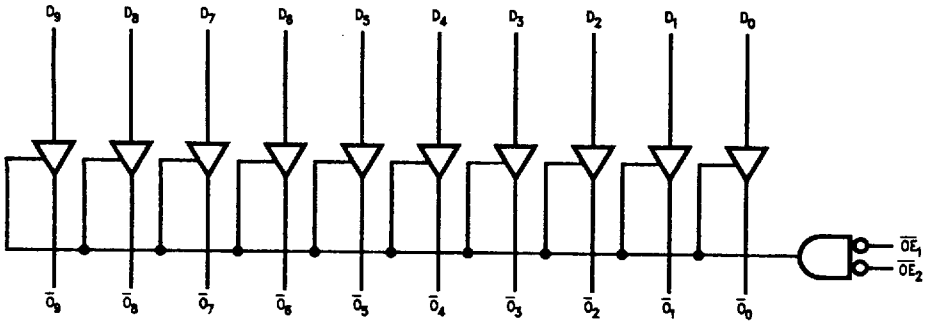
Truth Table

$\overline{OE}_n$	I_n	$\overline{O}_n$
L	H	L
L	L	H
H	X	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

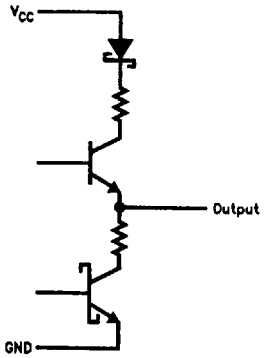
Pin Names	Description
$\overline{OE}_1$, $\overline{OE}_2$	Output Enable Input (Active LOW)
I_0–I_7	Inputs
$\overline{O}_0$–$\overline{O}_7$	Outputs

Logic Diagram



TL/F/10917–4

Schematic of Each Output



TL/F/10917–5

2828A

10

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias Plastic	−55°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Any Output in the Disable or Power-Off State in the High State	−0.5V to +5.5V −0.5V to V_{CC}
Current Applied to Output In LOW State (Max)	Twice the Rated I_{OL} (mA)
ESD Last Passing Voltage (Min)	4000V
DC Latchup Source Current	500 mA
Over Voltage Latchup	V_{CC} +4.5V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature Commercial	0°C to +70°C
Supply Voltage Commercial	+4.5V to +5.5V

DC Electrical Characteristics

Symbol	Parameter	54BCT/74BCT			Units	V_{CC}	Conditions
		Min	Typ	Max			
V_{IH}	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V_{IL}	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V_{CD}	Input Clamp Diode Voltage			−1.2	V	Min	I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	2.4 2.0			V	Min	I_{OH} = −3 mA I_{OH} = −15 mA
V_{OL}	Output LOW Voltage			0.5 0.8	V	Min	I_{OL} = 3 mA I_{OL} = 15 mA
I_{IH}	Input HIGH Current			5	μA	Max	V_{IN} = 2.7V
I_{BVI}	Input HIGH Current Breakdown Test			7	μA	Max	V_{IN} = 7.0V
I_{IL}	Input LOW Current			−200	μA	Max	V_{IN} = 0.5V
I_{OS}	Output Short-Circuit Current	−100		−225	mA	Max	V_{OUT} = 0V
I_{OZH}	Output Leakage Current			20	μA	Max	V_{OUT} = 2.7V
I_{OZL}	Output Leakage Current			−20	μA	Max	V_{OUT} = 0.5V
I_{CEX}	Output HIGH Leakage Current			50	μA	Max	V_{OUT} = V_{CC}
V_{ID}	Input Leakage Test	4.75			V	0.0	I_{ID} = 1.9 μA All Other Pins Grounded
I_{ZZ}	Bus Drainage Test			100	μA	0.0	V_{OUT} = 5.25V
I_{CCH}	Power Supply Current		5.6	10	mA	Max	V_O = HIGH
I_{CCL}	Power Supply Current		31	38	mA	Max	V_O = LOW
I_{CCZ}	Power Supply Current		4.0	6	mA	Max	V_O = HIGH Z

AC Electrical Characteristics: See Section 8 for Waveforms and Load Configurations

Symbol	Parameter	74BCT $T_A = +25°C$ $V_{CC} = +5.0V$ $C_L = 50$ pF			74BCT $T_A = Comm$ $V_{CC} = Comm$ $C_L = 50$ pF		Units	Fig. No.
		Min	Typ	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay Data to Output	1.0 1.0	2.7 2.7	7.0 7.0	1.07 1.0	8.0 8.0	ns	8-3
t_{PZH} t_{PZL}	Output Enable Time	2.5 5.0	5.4 8.0	10.0 12.0	2.5 5.0	10.5 12.5	ns	8-5
t_{PHZ} t_{PLZ}	Output Disable Time	2.0 2.0	4.2 5.0	8.5 8.5	2.0 2.0	10.0 10.0	ns	8-5
t_{OSHL} (Note 1)	Pin to Pin Skew HL Data to Output			0.5		0.6	ns	
t_{OSLH} (Note 1)	Pin to Pin Skew LH Data to Output			0.8		0.9	ns	
t_{OST} (Note 1)	Pin to Pin Skew LH/HL Data to Output			3.0		3.0	ns	
t_{PV} (Note 2)	Device to Device Skew LH/HL Data to Output			5.0		5.0	ns	

Note 1: Skew is defined as the absolute value of the difference between the actual propagation delays for any two separate outputs of the same device. The specification applies to any outputs switching HIGH to LOW (t_{OSHL}), LOW to HIGH (t_{OSLH}), or any combination switching LOW to HIGH and/or HIGH to LOW (t_{OST}). This specification is guaranteed but not tested.

Note 2: Propagation delay variation for a given set of conditions (i.e., temperature and V_{CC}) from device to device. This specification is guaranteed but not tested.

Extended AC Electrical Characteristics: See Section 8 for Waveforms and Load Configurations

Symbol	Parameter	74BCT $T_A = Comm$ $V_{CC} = Comm$ $C_L = 50$ pF 8 Outputs Switching (Note 1)		74BCT $T_A = Comm$ $V_{CC} = Comm$ $C_L = 250$ pF (Note 2)		Units	Fig. No.
		Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay Data to Output	1.5 2.5	8.5 8.5	3.0 4.0	8.5 9.0	ns	8-3

Note 1: This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase (i.e., all low-to-high, high-to-low, etc.)

Note 2: This specification is guaranteed but not tested. The limits represent propagation delays with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load.

Capacitance

Symbol	Parameter	Typ	Units	Conditions
C_{IN}	Input Capacitance	6.0	pF	$V_{CC} = 5.0V$
C_{OUT}	Output Pin Capacitance	15.0	pF	$V_{CC} = 5.0V$