

Octal bus switch with Quad Output Enables

74CBT3244

FEATURES

- Functionally equivalent to QS3244
- Standard '244-type pinout
- 5Ω switch connection between two ports
- TTL compatible control input levels
- Package options include plastic small outline (D), shrink small outline (DB), thin shrink small outline (TSSOP)

DESCRIPTION

The 74CBT3244 provides eight bits of high-speed TTL-compatible bus switching in a standard '244 device pinout. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

The 74CBT3244 device is organized as two 4-bit low-impedance switches with separate output-enable (OE) inputs. When OE is low, the switch is on and data can flow from port A to port B, or vice versa. When OE is high, the switch is open and high-impedance state exists between the two ports.

The 74CBT3244 is characterized for operation from -40°C to 85°C.

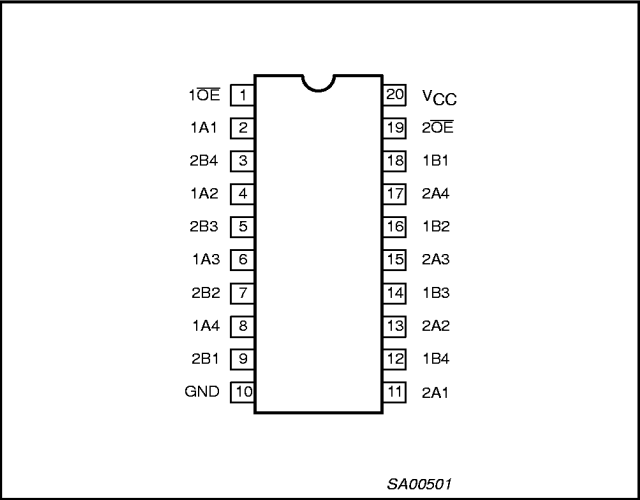
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T <sub>amb</sub> = 25°C; GND = 0V	TYPICAL	UNIT
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation delay An to Yn	C <sub>L</sub> = 50pF; V <sub>CC</sub> = 5V		ns
C <sub>IO(OFF)</sub>	Pin capacitance (OFF state)	V <sub>O</sub> = 3V or 0V	6	pF
I <sub>CCZ</sub>	Total supply current	Outputs disabled; V <sub>CC</sub> = 5.5V		μA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
20-Pin plastic SO	-40°C to 85°C	74CBT3244 D	74CBT3244 D	SOT163-1
20-Pin Plastic SSOP Type II	-40°C to 85°C	74CBT3244 DB	74CBT3244 DB	SOT339-1
20-Pin Plastic TSSOP Type I	-40°C to 85°C	74CBT3244 PW	7CBT3244PW DH	SOT360-1

PIN CONFIGURATION



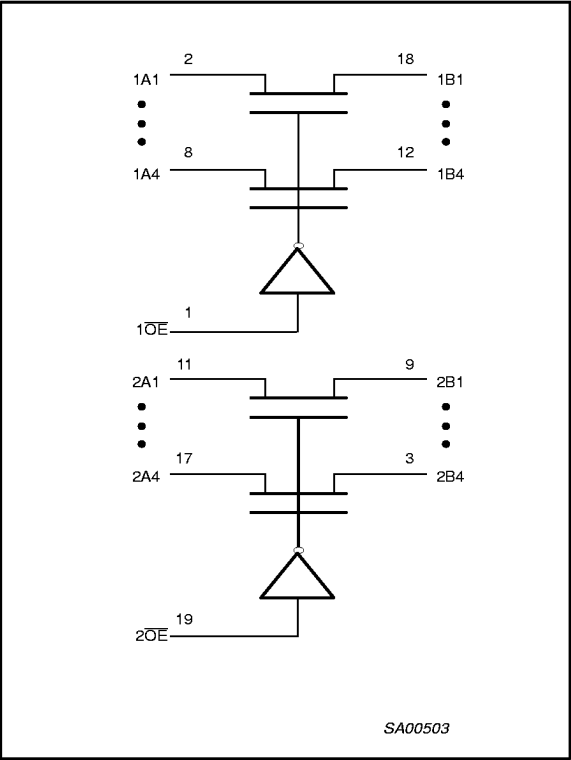
PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1, 19	1OE, 2OE	Output enable
2, 4, 6, 8	1A1-1A4	
11, 13, 15, 17	2A1-2A4	
18, 16, 14, 12	1B1-1B4	
9, 7, 5, 3	2B1-2B4	
10	GND	Ground (0V)
20	V <sub>CC</sub>	Positive supply voltage

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LOGIC SYMBOL



FUNCTION TABLE

INPUTS		OUTPUTS	
1OE	2OE	1A, 1B	2A, 2B
L	L	1A = 1B	2A = 2B
L	H	1A = 1B	Z
H	L	Z	2A = 2B
H	H	Z	Z

H = High voltage level  
L = Low voltage level  
Z = High impedance "off" state

ABSOLUTE MAXIMUM RATINGS<sup>1, 2</sup>

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V <sub>CC</sub>	DC supply voltage		−0.5 to +7.0	V
I <sub>IK</sub>	DC input diode current	V <sub>I</sub> < 0	−18	mA
V <sub>I</sub>	DC input voltage <sup>3</sup>		−1.2 to +7.0	V
I <sub>OK</sub>	DC output diode current	V <sub>O</sub> < 0	−50	mA
V <sub>OUT</sub>	DC output voltage <sup>3</sup>	output in Off or High state	−0.5 to +7	V
I <sub>OUT</sub>	DC output current	output in Low state	128	mA
T <sub>stg</sub>	Storage temperature range		−65 to 150	°C

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

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## RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
$V_{CC}$	DC supply voltage	4.5	5.5	V
$V_{IH}$	High-level input voltage	2.0		V
$V_{IL}$	Low-level Input voltage		0.8	V
$T_{amb}$	Operating free-air temperature range	-40	+85	°C

## DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			T <sub>amb</sub> = −40°C to +85°C			
			Min	Typ <sup>1</sup>	Max	
V <sub>IK</sub>	Input clamp voltage	V <sub>CC</sub> = 4.5V; I <sub>I</sub> = −18mA			−1.2	V
I <sub>I</sub>	Input leakage current	V <sub>CC</sub> = 5.5V; V <sub>I</sub> = GND or 5.5V			±5	μA
I <sub>CC</sub>	Quiescent supply current <sup>2</sup>	V <sub>CC</sub> = 5.5V; I <sub>O</sub> = 0, V <sub>I</sub> = V <sub>CC</sub> or GND			50	μA
ΔI <sub>CC</sub>	Additional supply current per input pin <sup>2</sup>	V <sub>CC</sub> = 5.5V, one input at 3.4V, other inputs at V <sub>CC</sub> or GND			3.5	mA
C <sub>I</sub>	Control pins	V <sub>I</sub> = 3V or 0, $\overline{OE}$ = V <sub>CC</sub>		3		pF
C <sub>IO(OFF)</sub>	Power-off leakage current	V <sub>O</sub> = 3V or 0		6		pF
r <sub>on</sub> <sup>3</sup>	On-resistance	V <sub>CC</sub> = 4.5V; V <sub>I</sub> = 0V; I <sub>I</sub> = 64mA		5	7	Ω
		V <sub>CC</sub> = 4.5V; V <sub>I</sub> = 0V; I <sub>I</sub> = 30mA		5	7	
		V <sub>CC</sub> = 4.5V; V <sub>I</sub> = 0V; I <sub>I</sub> = 15mA		10	15	

## NOTES:

1. All typical values are at  $V_{CC} = 5\text{V}$ ,  $T_A = 25^{\circ}\text{C}$
2. This is the increase in supply current for each input that is at the specified TTL voltage level rather than  $V_{CC}$  or GND
3. Measured by the voltage drop between the A and the B terminals at the indicated current through the switch.  
On-state resistance is determined by the lowest voltage of the two (A or B) terminals.

## AC CHARACTERISTICS

GND = 0V;  $t_R$ ;  $C_L = 50\text{pF}$ 

SYMBOL	PARAMETER	FROM (INPUT)	TO (OUTPUT)	74CBT3244		UNIT
				T <sub>amb</sub> = −40°C to +85 V <sub>CC</sub> = +5.0V ±0.5V		
				Min	Max	
t <sub>pd</sub>	Propagation delay <sup>1</sup>	A or B	B or A		.25	ns
t <sub>en</sub>	Output enable time to High and Low level	OE	A or B	1.0	8.9	ns
t <sub>dis</sub>	Output disable time from High and Low level	OE	A or B	1.0	7.4	ns

## NOTES:

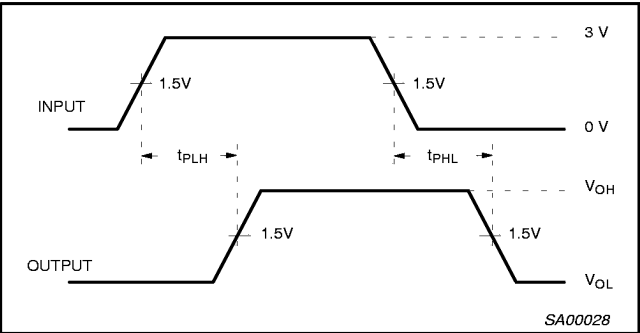
1. This parameter is warranted but not production tested. The propagation delay is based on the RC time constant of the typical on-state resistance of the switch and a load capacitance of 50 pF, when driven by an ideal voltage source (zero output impedance).

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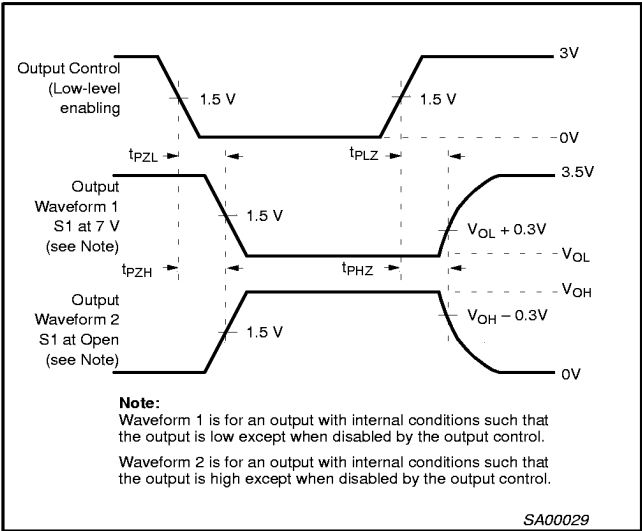
74CBT3244

AC WAVEFORMS

$V_M = 1.5\text{V}$ ,  $V_{IN} = \text{GND to } 3.0\text{V}$

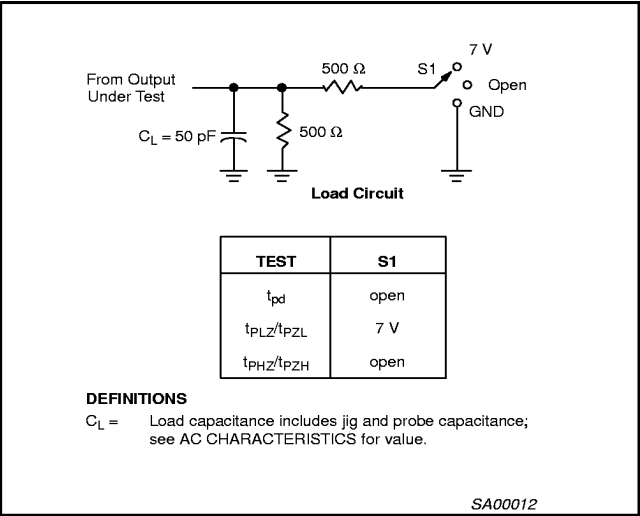


Waveform 1. Input to Output Propagation Delays



Waveform 2. 3-State Output Enable and Disable Times

TEST CIRCUIT AND WAVEFORMS



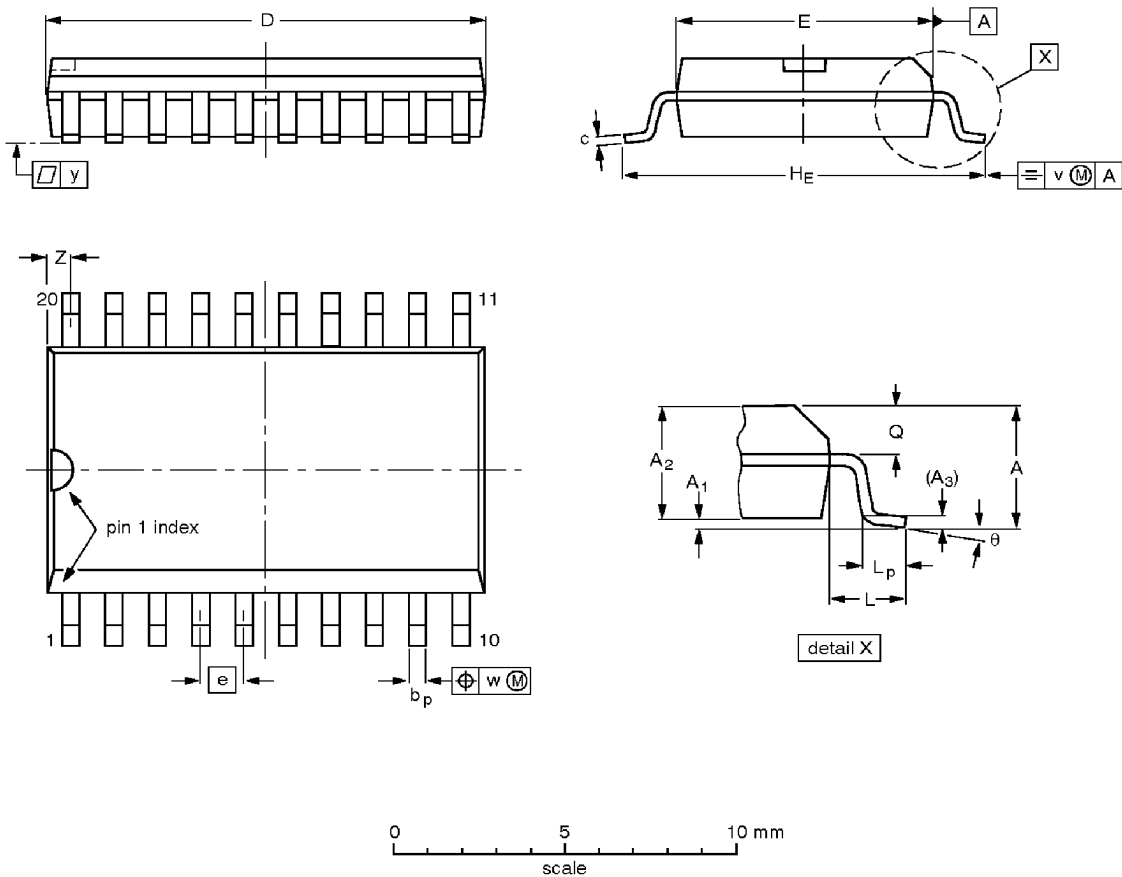
- NOTES:**
- All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 2.5\ \text{ns}$ ,  $t_f \leq 2.5\ \text{ns}$ .
  - The outputs are measured one at a time with one transition per measurement.

Octal bus switch with Quad Output Enables

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SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

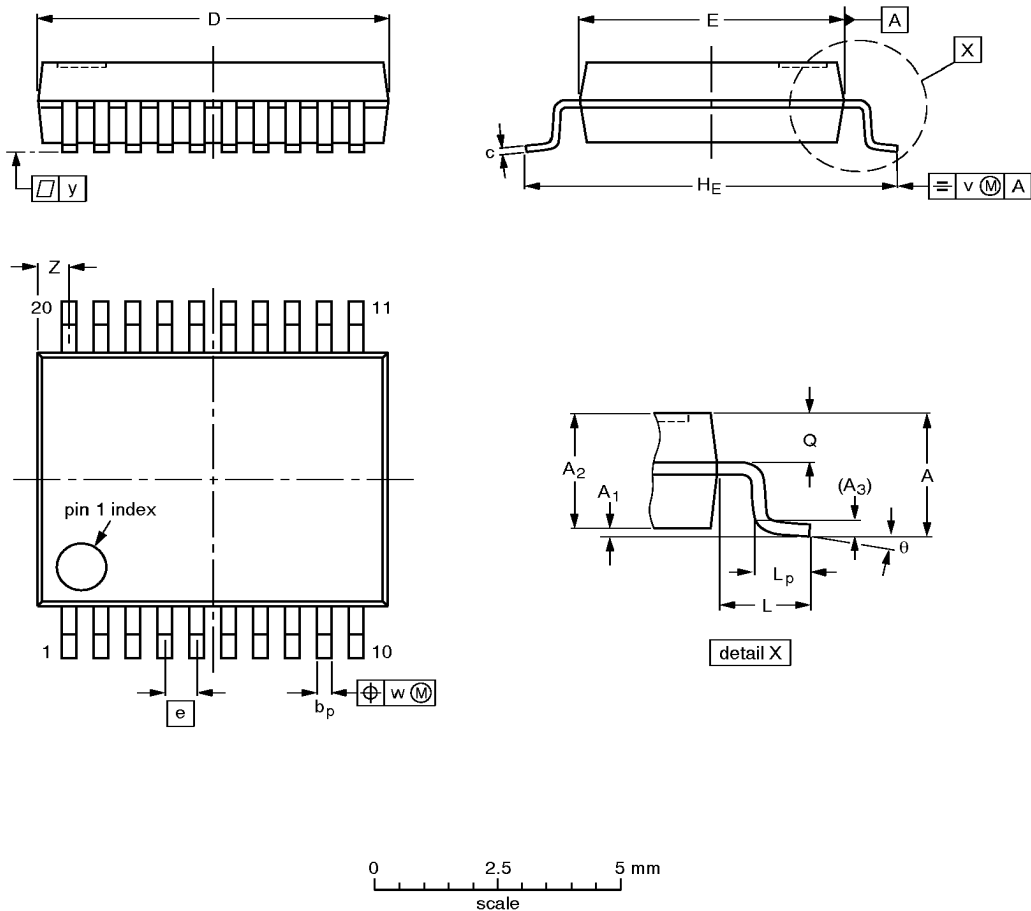
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT163-1	075E04	MS-013AC				95-01-24 97-05-22

Octal bus switch with Quad Output Enables

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SSOP20: plastic shrink small outline package; 20 leads; body width 5.3 mm

SOT339-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	7.4 7.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.9 0.5	8° 0°

Note
1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

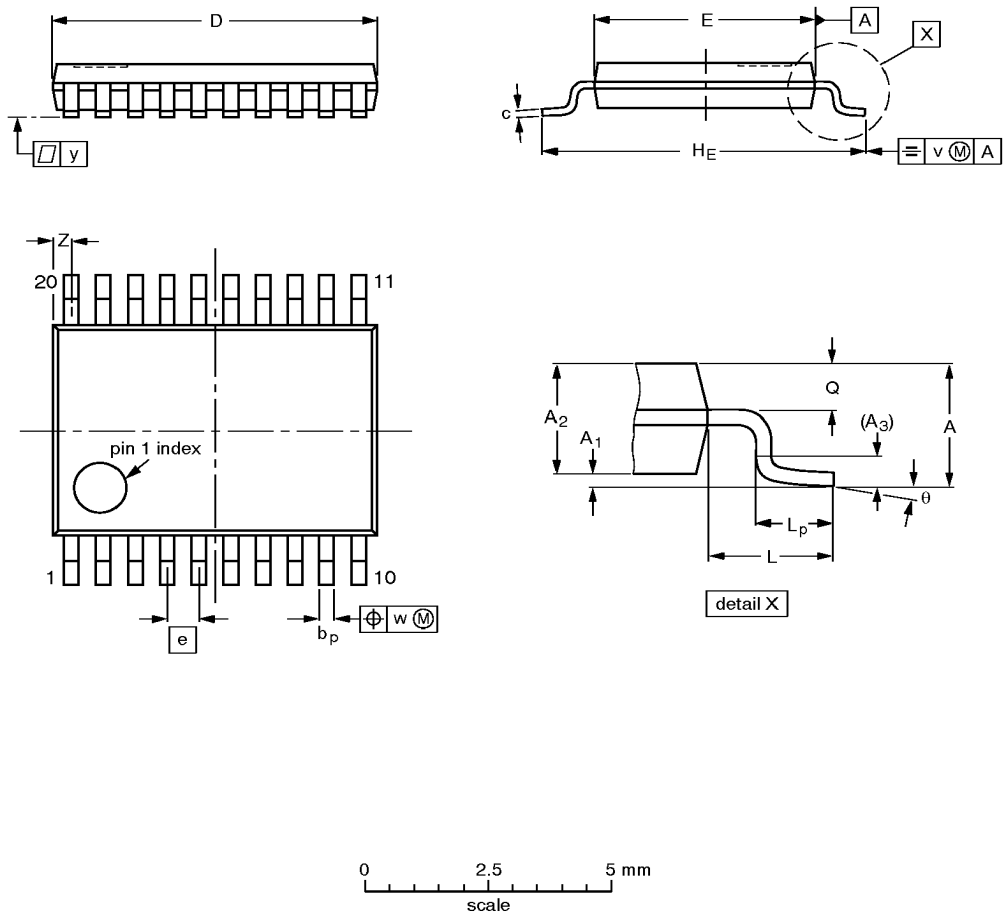
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT339-1		MO-150AE				93-09-08 95-02-04

Octal bus switch with Quad Output Enables

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TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1



DIMENSIONS (mm are the original dimensions)

UNIT	A <sub>max.</sub>	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(2)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8° 0°

Notes

- 1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
- 2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT360-1		MO-153AC				93-06-16 95-02-04