National Semiconductor

74FR240
Octal Buffer/Line Driver with TRI-STATE® Outputs

General Description

The 'FR240 is an inverting octal buffer and line driver designed to be employed as memory and address driver, clock driver and bus oriented transmitter or receiver.

Features

- TRI-STATE outputs drive bus lines or buffer memory address registers
- Outputs sink 64 mA and source 15 mA
- Guaranteed pin-to-pin skew
- Guaranteed 4000V minimum ESD protection

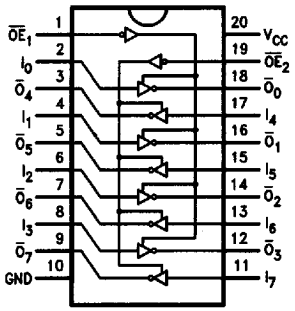
Ordering Code: See Section 11

Commercial	Package Number	Package Description
74FR240PC	N20A	20-Lead (0.300" Wide) Molded Dual-In-Line
74FR240SC (Note 1)	M20B	20-Lead (0.300" Wide) Molded Small Outline, JEDEC
74FR240SJ (Note 1)	M20D	20-Lead (0.300" Wide) Molded Small Outline, EIAJ

Note 1: Devices also available in 13" reel. Use suffix = SCX and SJX.

Connection Diagram

Pin Assignment for DIP and SOIC



TL/F/10901–1

Pin Description

Pin Names	Description
$\overline{OE}_1$, $\overline{OE}_2$	Output Enable Input (Active Low)
I_0–I_7	Inputs
$\overline{O}_0$–$\overline{O}_7$	Outputs

Truth Tables

Inputs		Outputs (Pins 12, 14, 16, 18)
$\overline{OE}_1$	I_n	
L	L	H
L	H	L
H	X	Z

Inputs		Outputs (Pins 3, 5, 7, 9)
$\overline{OE}_2$	I_n	
L	L	H
L	H	L
H	X	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

Absolute Maximum Ratings (Note 1)

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	
Plastic	−55°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output in High State (with V_{CC} = 0V)	
Standard Output	−0.5V to V_{CC}
TRI-STATE Output	−0.5V to +5.5V
Current Applied to Output in Low State (Max)	Twice the Rated I_{OL} (mA)
ESD Last Passing Voltage (Min)	4000V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature	
Commercial	0°C to +70°C
Supply Voltage	
Commercial	+4.5V to +5.5V

DC Electrical Characteristics

Symbol	Parameter	74FR			Units	V_{CC}	Conditions
		Min	Typ	Max			
V_{IH}	Input High Voltage	2.0			V		Recognized High Signal
V_{IL}	Input Low Voltage			0.8	V		Recognized Low Signal
V_{CD}	Input Clamp Diode Voltage			−1.2	V	Min	I_{IN} = −18 mA
V_{OH}	Output High Voltage	2.4			V	Min	I_{OH} = −3 mA
		2.0			V	Min	I_{OH} = −15 mA
V_{OL}	Output Low Voltage			0.55	V	Min	I_{OL} = 64 mA
I_{IH}	Input High Current			5	μA	Max	V_{IN} = 2.7V
I_{BVI}	Input High Current Breakdown Test			7	μA	Max	V_{IN} = 7.0V
I_{IL}	Input Low Currrent			−150	μA	Max	V_{IN} = 0.5V
V_{ID}	Input Leakage Test	4.75			V	0.0	I_{ID} = 1.9 μA, All Other Pins Grounded
I_{OD}	Output Circuit Leakage Current			3.75	μA	0.0	V_{IOD} = 150 mV, All Other Pins Grounded
I_{OZH}	Output Leakage Current			20	μA	Max	V_{OUT} = 2.7V
I_{OZL}	Output Leakage Current			−20	μA	Max	V_{OUT} = 0.5V
I_{OS}	Output Short-Circuit Current	−100		−225	mA	Max	V_{OUT} = 0.0V
I_{CEX}	Output High Leakage Current			50	μA	Max	V_{OUT} = V_{CC}
I_{ZZ}	Bus Drainage Test			100	μA	0.0	V_{OUT} = 5.25V
I_{CCH}	Power Supply Current		9	13	mA	Max	All Outputs High
I_{CCL}	Power Supply Current		37	45	mA	Max	All Outputs Low
I_{CCZ}	Power Supply Current		31	38	mA	Max	Outputs TRI-STATE
C_{IN}	Input Capacitance		8.0		pF	5.0	

AC Electrical Characteristics: See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74FR $T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50$ pF			74FR $T_A = Comm$, $V_{CC} = Comm$, $C_L = 50$ pF		Units	Fig. No.
		Min	Typ	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay A_n to B_n or B_n to A_n	1.0 1.0	3.3 2.9	4.7 4.7	1.0 1.0	4.7 4.7	ns	2–3
t_{PZH} t_{PZL}	Output Enable Time	2.6 2.6	4.0 6.3	7.0 7.0	2.6 2.6	7.0 7.0	ns	2–5
t_{PHZ} t_{PLZ}	Output Disable Time	1.7 1.7	3.3 2.9	6.6 6.6	1.7 1.7	6.6 6.6	ns	2–5

Extended AC Characteristics: See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74FR $T_A = Comm$, $V_{CC} = Comm$, $C_L = 50$ pF, Eight Outputs Switching (Note 2)		74FR $T_A = Comm$, $V_{CC} = Comm$, $C_L = 250$ pF (Note 3)		Units	Fig. No.
		Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay A_n to B_n or B_n to A_n	1.0 1.0	6.4 6.4	2.3 2.3	8.3 8.3	ns	2–3
t_{PZH} t_{PZL}	Output Enable Time	2.6 2.6	7.2 7.2			ns	2–5
t_{PHZ} t_{PLZ}	Output Disable Time	1.7 1.7	6.8 6.8			ns	2–5
t_{OSHL} (Note 1)	Pin to Pin Skew for HL Transitions		2.0			ns	
t_{OSLH} (Note 1)	Pin to Pin Skew for LH Transitions		1.1			ns	
t_{OST} (Note 1)	Pin to Pin Skew for HL/LH Transitions		3.1			ns	

Note 1: Skew is defined as the absolute value of the difference between the actual propagation delays for any two outputs of the same device. The specification applies to any outputs switching high to low, (t_{OSHL}), low to high, (t_{OSLH}), or high to low and/or low to high, (t_{OST}). Specifications guaranteed with all outputs switching in phase.

Note 2: This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase, i.e., all low-to-high, high-to-low, TRI-STATE-to-high, etc.

Note 3: These specifications guaranteed but not tested. The limits represent propagation delays with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load. This specification pertains to single output switching only.