National Semiconductor

74F538
1-of-8 Decoder with TRI-STATE® Outputs

General Description

The 'F538 decoder/demultiplexer accepts three Address (A_0–A_2) input signals and decodes them to select one of eight mutually exclusive outputs. A polarity control input (P) determines whether the outputs are active LOW or active HIGH. A HIGH Signal on either of the active LOW Output Enable ($\overline{OE}$) inputs forces all outputs to the high impedance state. Two active HIGH and two active LOW input enables are available for easy expansion to 1-of 32 decoding with four packages, or for data demultiplexing to 1-of-8 or 1-of-16 destinations.

Features

- Output polarity control
- Data demultiplexing capability
- Multiple enables for expansion
- TRI-STATE outputs

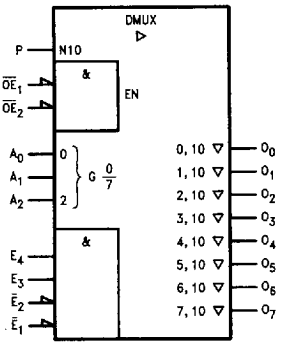
Ordering Code: See Section 11

Commercial	Package Number	Package Description
74F538PC	N20A	20-Lead (0.300" Wide) Molded Dual-In-Line
74F538SC (Note 1)	M20B	20-Lead (0.300" Wide) Molded Small Outline, JEDEC
74F538SJ (Note 1)	M20D	20-Lead (0.300" Wide) Molded Small Outline, EIAJ

Note 1: Devices also available in 13" reel. Use suffix = SCX and SJX.

Logic Symbols

IEEE/IEC



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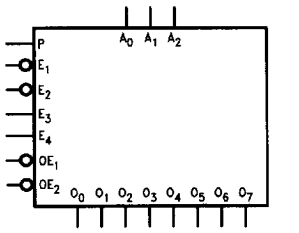

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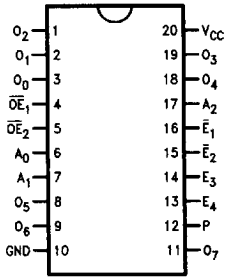
Connection Diagram

Pin Assignment for DIP and SOIC



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Unit Loading/Fan Out: See Section 2 for U.L. Definitions

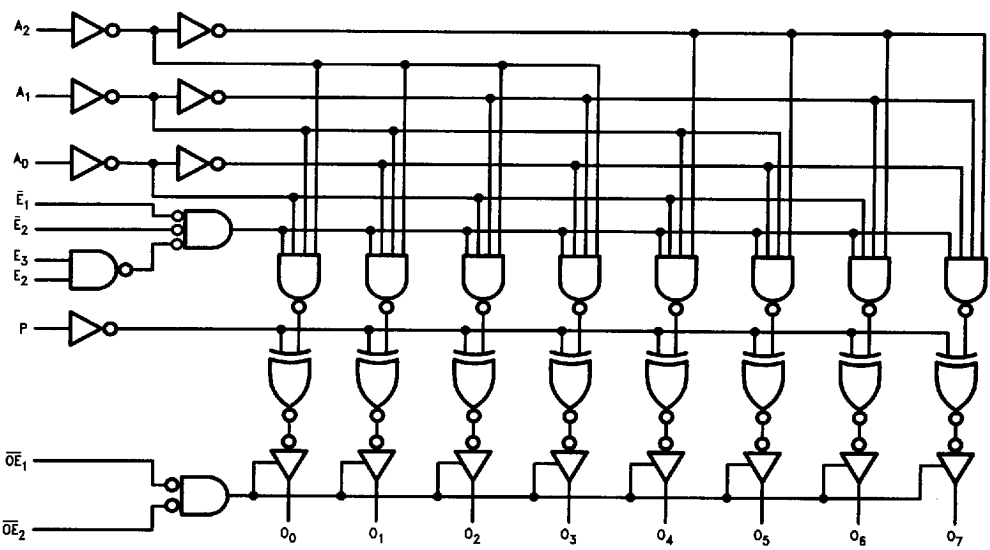
Pin Names	Description	74F	
		U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
A_0–A_2	Address Inputs	1.0/1.0	20 μA/−0.6 mA
$\overline{E}_1$, $\overline{E}_2$	Enable Inputs (Active LOW)	1.0/1.0	20 μA/−0.6 mA
E_3, E_4	Enable Inputs (Active HIGH)	1.0/1.0	20 μA/−0.6 mA
P	Polarity Control Input	1.0/1.0	20 μA/−0.6 mA
$\overline{OE}_1$, $\overline{OE}_2$	Output Enable Inputs (Active LOW)	1.0/1.0	20 μA/−0.6 mA
O_0–O_7	TRI-STATE Outputs	150/40 (33.3)	−3 mA/24 mA (20 mA)

Truth Table

Function	Inputs									Outputs							
	$\overline{OE}_1$	$\overline{OE}_2$	$\overline{E}_1$	E_2	E_3	E_4	A_2	A_1	A_0	O_0	O_1	O_2	O_3	O_4	O_5	O_6	O_7
High Impedance	H	X	X	X	X	X	X	X	X	Z	Z	Z	Z	Z	Z	Z	Z
	X	H	X	X	X	X	X	X	X	Z	Z	Z	Z	Z	Z	Z	Z
Disable	L	L	H	X	X	X	X	X	X	Outputs Equal P Input							
	L	L	X	H	X	X	X	X	X								
	L	L	X	X	L	X	X	X	X								
	L	L	X	X	X	L	X	X	X								
Active HIGH Output (P = L)	L	L	L	L	H	H	L	L	L	H	L	L	L	L	L	L	L
	L	L	L	L	H	H	L	L	H	L	H	L	L	L	L	L	L
	L	L	L	L	H	H	L	H	L	L	L	H	L	L	L	L	L
	L	L	L	L	H	H	L	H	H	L	L	L	H	L	L	L	L
	L	L	L	L	H	H	H	L	L	L	L	L	L	H	L	L	L
	L	L	L	L	H	H	H	L	H	L	L	L	L	L	H	L	L
	L	L	L	L	H	H	H	H	L	L	L	L	L	L	L	H	L
	L	L	L	L	H	H	H	H	H	L	L	L	L	L	L	L	H
Active LOW Output (P = H)	L	L	L	L	H	H	L	L	L	L	H	H	H	H	H	H	H
	L	L	L	L	H	H	L	L	H	H	L	H	H	H	H	H	H
	L	L	L	L	H	H	L	H	L	H	H	L	H	H	H	H	H
	L	L	L	L	H	H	L	H	H	H	H	H	L	H	H	H	H
	L	L	L	L	H	H	H	L	L	H	H	H	H	L	H	H	H
	L	L	L	L	H	H	H	L	H	H	H	H	H	H	L	H	H
	L	L	L	L	H	H	H	H	L	H	H	H	H	H	H	L	H
	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

Logic Diagram



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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +175°C
Plastic	−55°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V_{CC} = 0V)	
Standard Output	−0.5V to V_{CC}
TRI-STATE Output	−0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I_{OL} (mA)

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature	
Commercial	0°C to +70°C
Supply Voltage	
Commercial	+4.5V to +5.5V

DC Electrical Characteristics

Symbol	Parameter		74F Min	74F Typ	74F Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal
V_{IL}	Input LOW Voltage				0.8	V		Recognized as a LOW Signal
V_{CD}	Input Clamp Diode Voltage				−1.2	V	Min	I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage	74F 10% V_{CC}	2.5			V	Min	I_{OH} = −1 mA
		74F 10% V_{CC}	2.4					I_{OH} = −3 mA
		74F 5% V_{CC}	2.7					I_{OH} = −1 mA
		74F 5% V_{CC}	2.7					I_{OH} = −3 mA
V_{OL}	Output LOW Voltage	74F 10% V_{CC}			0.5	V	Min	I_{OL} = 20 mA
I_{IH}	Input HIGH Current	74F			5.0	μA	Max	V_{IN} = 2.7V
I_{BVI}	Input HIGH Current Breakdown Test	74F			7.0	μA	Max	V_{IN} = 7.0V
I_{CEX}	Output HIGH Leakage Current	74F			50	μA	Max	V_{OUT} = V_{CC}
V_{ID}	Input Leakage Test	74F	4.75			V	0.0	I_{ID} = 1.9 μA All Other Pins Grounded
I_{OD}	Output Leakage Circuit Current	74F			3.75	μA	0.0	V_{IOD} = 150 mV All Other Pins Grounded
I_{IL}	Input LOW Current				−0.6	mA	Max	V_{IN} = 0.5V
I_{OZH}	Output Leakage Current				50	μA	Max	V_{OUT} = 2.7V
I_{OZL}	Output Leakage Current				−50	μA	Max	V_{OUT} = 0.5V
I_{OS}	Output Short-Circuit Current		−60		−150	mA	Max	V_{OUT} = 0V
I_{ZZ}	Bus Drainage Test				500	μA	0.0V	V_{OUT} = 5.25V
I_{CCH}	Power Supply Current			31	45	mA	Max	V_O = HIGH
I_{CCL}	Power Supply Current			37	56	mA	Max	V_O = LOW
I_{CCZ}	Power Supply Current			37	56	mA	Max	V_O = HIGH Z

AC Electrical Characteristics: See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F $T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50$ pF			74F T_A, V_{CC} = Com, $C_L = 50$ pF		Units	Fig. No.
		Min	Typ	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay A_n to O_n	6.0 4.0	11.0 7.5	16.0 11.0	6.0 4.0	17.0 12.0	ns	2–3
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}_1$ or $\overline{E}_2$ to O_n	5.0 4.0	8.5 6.5	15.0 9.0	5.0 4.0	16.0 10.0		
t_{PLH} t_{PHL}	Propagation Delay E_3 or E_4 to O_n	6.0 5.0	11.0 10.0	16.0 14.0	6.0 5.0	17.0 15.0	ns	2–3
t_{PLH} t_{PHL}	Propagation Delay P to O_n	6.0 6.0	11.5 11.0	18.0 16.0	6.0 6.0	20.0 17.0		
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}_1$ or $\overline{OE}_2$ to O_n	3.0 5.0	5.5 9.0	10.0 13.0	3.0 5.0	11.0 14.0	ns	2–5
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}_1$ or $\overline{OE}_2$ to O_n	2.0 3.0	4.0 5.0	6.0 8.0	2.0 3.0	7.0 9.0		