National Semiconductor

74FR543
Octal Latched Transceiver with TRI-STATE® Outputs

General Description

The 'FR543 octal transceiver contains two sets of D-type latches for temporary storage of data flowing in either direction. Separate Latch Enable and Output Enable inputs are provided for each register to permit independent control of inputting and outputting in either direction of data flow. Both the A and B outputs will source 15 mA and sink 64 mA.

Features

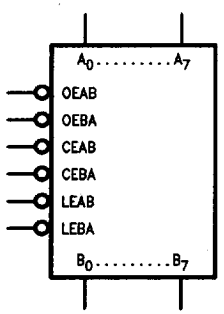
- Functionally equivalent to 'F543
- Back-to-back registers for storage
- Bidirectional data path
- A and B outputs have current sourcing capability of 15 mA and current sinking capability of 64 mA
- Separate controls for data flow in each direction
- Guaranteed pin-to-pin skew
- Guaranteed 4000V minimum ESD protection

Ordering Code: See Section 11

Commercial	Package Number	Package Description
74FR543SPC	N24C	24-Lead (0.300" Wide) Molded Dual-In-Line
74FR543SC (Note 1)	M24B	24-Lead (0.300" Wide) Molded Small Outline, JEDEC

Note 1: Devices also available in 13" reel. Use suffix = SCX.

Logic Symbol



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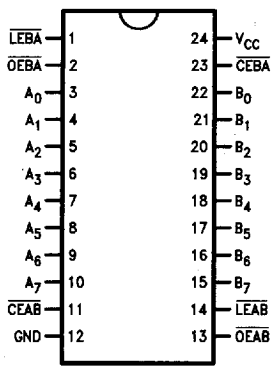
Connection Diagram

Pin Assignment for DIP and SOIC



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Pin Descriptions

Pin Names	Description
$\overline{OEAB}$, $\overline{OEBA}$	Output Enable Inputs
$\overline{LEAB}$, $\overline{LEBA}$	Latch Enable Inputs
$\overline{CEAB}$, $\overline{CEBA}$	Chip Enable Inputs
A_0–A_7	Side A Inputs or TRI-STATE Outputs
B_0–B_7	Side B Inputs or TRI-STATE Outputs

Functional Description

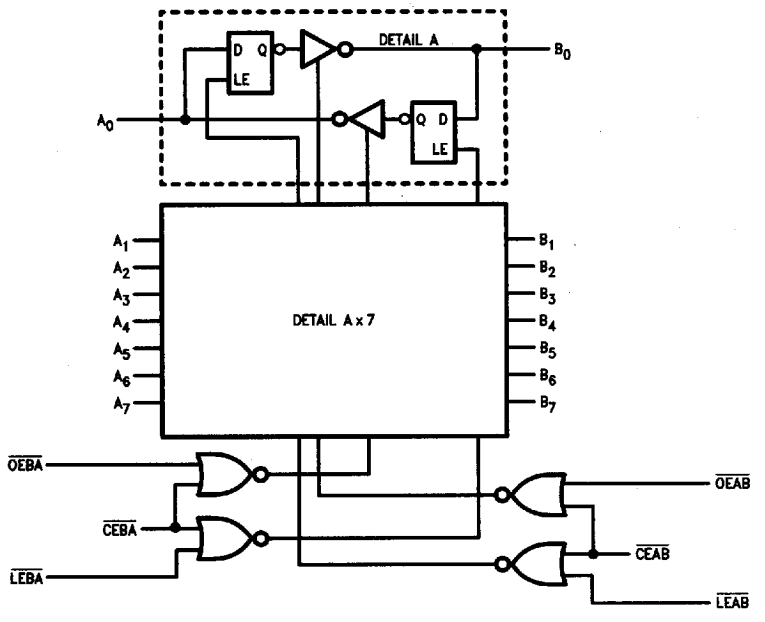
The 'FR543 contains two sets of D-type latches, with separate input and output controls for each. For data flow from A to B, for example, the A to B Enable ($\overline{CEAB}$) input must be low in order to enter data from the A port or take data from the B port as indicated in the Data I/O Control Table. With $\overline{CEAB}$ low, a low signal on ($\overline{LEAB}$) input makes the A to B latches transparent; a subsequent low to high transition of the $\overline{LEAB}$ line puts the A latches in the storage mode and their outputs no longer change with the A inputs. With $\overline{CEAB}$ and $\overline{OEAB}$ both low, the B output buffers are active and reflect the data present on the output of the A latches. Control of data flow from B to A is similar, but using the $\overline{CEBA}$, $\overline{LEBA}$ and $\overline{OEBA}$.

Data I/O Control Table

Inputs			Latch Status	Output Buffers
$\overline{CEAB}$	$\overline{LEAB}$	$\overline{OEAB}$		
H	X	X	Latched	High Z
X	H	X	Latched	—
L	L	X	Transparent	—
X	X	H	—	High Z
L	X	L	—	Driving

H = High Voltage Level
L = Low Voltage Level
X = Immaterial

Logic Diagram



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Absolute Maximum Ratings (Note 1)

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	
Plastic	−55°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output in High State (with V_{CC} = 0V)	
Standard Output	−0.5V to V_{CC}
TRI-STATE Output	−0.5V to +5.5V
Current Applied to Output in Low State (Max)	twice the rated I_{OL} (mA)
ESD Last Passing Voltage (Min)	4000V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature	
Commercial	0°C to +70°C
Supply Voltage	
Commercial	+4.5V to +5.5V

DC Electrical Characteristics

Symbol	Parameter	74FR			Units	V_{CC}	Conditions
		Min	Typ	Max			
V_{IH}	Input High Voltage	2.0			V		Recognized High Signal
V_{IL}	Input Low Voltage			0.8	V		Recognized Low Signal
V_{CD}	Input Clamp Diode Voltage			−1.2	V	Min	I_{IN} = −18 mA
V_{OH}	Output High Voltage	2.4			V	Min	I_{OH} = −3 mA (A_n, B_n)
		2.0			V	Min	I_{OH} = −15 mA (A_n, (B_n)
V_{OL}	Output Low Voltage			0.55	V	Min	I_{OL} = 64 mA (A_n, B_n)
I_{IH}	Input High Current			5	μA	Max	V_{IN} = 2.7V
I_{BVI}	Input High Current Breakdown Test			7	μA	Max	V_{IN} = 7.0V (Control Pins)
I_{BVIT}	Input High Current Breakdown Test (I/O)			100	μA	Max	V_{IN} = 5.5V (A_n, B_n)
I_{IL}	Input Low Current			−150	μA	Max	V_{IN} = 0.5 (CEAB, CEBA)
				−100	μA	Max	V_{IN} = 0.5 (LEAB, LEBA, OEAB, OEBA)
V_{ID}	Input Leakage Test	4.75			V	0.0	I_{ID} = 1.9 μA, All Other Pins Grounded
I_{OD}	Output Circuit Leakage Test			3.75	μA	0.0	V_{IOD} = 150 mV, All Other Pins Grounded
$I_{IH} + I_{OZH}$	Output Leakage Current			25	μA	Max	V_{OUT} = 2.7V (A_n, B_n)
$I_{IL} + I_{OZL}$	Output Leakage Current			−150	μA	Max	V_{OUT} = 0.5V (A_n, B_n)
I_{OS}	Output Short-Circuit Current	−100		−225	mA	Max	V_{OUT} = 0.0V (A_n, B_n)
I_{CEX}	Output High Leakage Current			50	μA	Max	V_{OUT} = V_{CC} (A_n, B_n)
I_{ZZ}	Bus Drainage Test			100	μA	0.0	V_{OUT} = 5.25V (A_n, B_n)
I_{CCH}	Power Supply Current		59	72	mA	Max	All Outputs High
I_{CCL}	Power Supply Current		87	102	mA	Max	All Outputs Low
I_{CCZ}	Power Supply Current		69	85	mA	Max	Outputs TRI-STATE
C_{IN}	Input Capacitance		8.0		pF	5.0	Control Pins
			17.0		pF	5.0	A_n, B_n

AC Electrical Characteristics: See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74FR $T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50$ pF			54FR $T_A = Comm$, $V_{CC} = Comm$, $C_L = 50$ pF		Units	Fig. No.
		Min	Typ	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay A_n to B_n or B_n to A_n	1.3 1.3	3.0 2.6	4.7 4.7	1.3 1.3	4.7 4.7	ns	2–3
t_{PLH} t_{PHL}	Propagation Delay LEAB to B, LEBA to A	2.3 2.3	5.7 4.0	8.5 8.5	2.3 2.3	8.5 8.5	ns	2–3
t_{PZH} t_{PZL}	Output Enable Time	2.3 2.3	4.3 4.9	7.4 7.4	2.3 2.3	7.4 7.4	ns	2–5
t_{PHZ} t_{PLZ}	Output Disable Time	1.6 1.6	3.9 3.5	7.0 7.0	1.6 1.6	7.0 7.0	ns	2–5

AC Operating Requirements: See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74FR $T_A = +25°C$, $V_{CC} = +5.0V$, $C_L = 50$ pF			54FR $T_A = Comm$, $V_{CC} = Comm$, $C_L = 50$ pF		Units	Fig. No.
		Min	Typ	Max	Min	Max		
$t_s(H)$ $t_s(L)$	Setup Time, High or Low D_n to LE	2.5 2.5	0.5 0.1		2.5 2.5		ns	2–6
$t_h(H)$ $t_h(L)$	Hold Time, High or Low D_n to LE	2.0 2.0	0.0 −0.6		2.0 2.0		ns	2–6
$t_w(H)$	LE Pulse Width High	6.0	3.6		6.0		ns	2–4

Extended AC Characteristics: See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74FR T_A = Comm, V_{CC} = Comm, C_L = 50 pF, Eight Outputs Switching (Note 2)		54FR T_A = Comm, V_{CC} = Comm, C_L = 250 pF (Note 3)		Units	Fig. No.
		Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay A_n to B_n or B_n to A_n	1.3 1.3	6.3 6.3	3.2 3.2	8.7 8.7	ns	2–3
t_{PLH} t_{PHL}	Propagation Delay LEAB to B, LEBA to A	2.3 2.3	10.2 10.2	4.2 4.2	12.8 12.8	ns	2–3
t_{PZH} t_{PZL}	Output Enable Time	2.3 2.3	11.1 11.1			ns	2–5
t_{PHZ} t_{PLZ}	Output Disable Time	1.6 1.6	7.2 7.2			ns	2–5
t_{OSHL} (Note 1)	Pin to Pin Skew for HL Transitions		1.2			ns	
t_{OSLH} (Note 1)	Pin to Pin Skew for LH Transitions		1.0			ns	
t_{OST} (Note 1)	Pin to Pin Skew for HL/LH Transitions		3.1			ns	

Note 1: Skew is defined as the absolute value of the difference between the actual propagation delays for any two outputs of the same device. The specification applies to any outputs switching high to low, (t_{OSHL}), low to high, (t_{OSLH}), or high to low and/or low to high, (t_{OST}). Specifications guaranteed with all outputs switching in phase.

Note 2: This specification is guaranteed but not tested. The limits apply to propagation delays for all paths described switching in phase, i.e., all low-to-high, high-to-low, TRI-STATE-to-high, etc.

Note 3: These specifications guaranteed but not tested. The limits represent propagation delays with 250 pF load capacitors in place of the 50 pF load capacitors in the standard AC load. This specification pertains to single output switching only.