

74F552

Octal Registered Transceiver with Parity and Flags

General Description

The 'F552 octal transceiver contains two 8-bit registers for temporary storage of data flowing in either direction. Each register has its own clock pulse and clock enable input as well as a flag flip-flop that is set automatically as the register is loaded. The flag output will be reset when the output enable returns to HIGH after reading the output port. Each register has a separate output enable control for its TRI-STATE® buffer. The separate Clocks, Flags, and Enables provide considerable flexibility as I/O ports for demand-response data transfer. When data is transferred from the A-port to the B-port, a parity bit is generated. On the

other hand, when data is transferred from the B-port to the A-port, the parity of input data on B₀–B₇ is checked.

Features

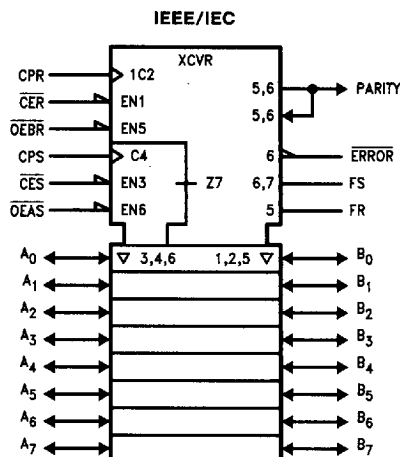
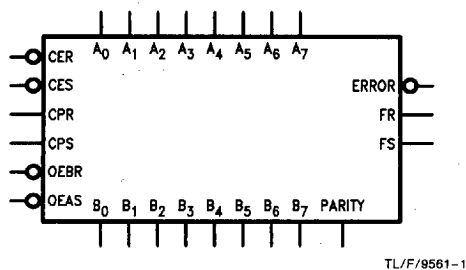
- 8-Bit bidirectional I/O Port with handshake
- Register status flag flip-flops
- Separate clock enable and output enable
- Parity generation and parity check
- B-outputs sink 64 mA
- TRI-STATE outputs

Ordering Code: See Section 11

Commercial	Package Number	Package Description
74F552QC (Note 1)	V28A	28-Lead Molded Plastic Leaded Chip Carrier
74F552SC (Note 1)	M28B	28-Lead (0.300" Wide) Molded Small Outline, JEDEC

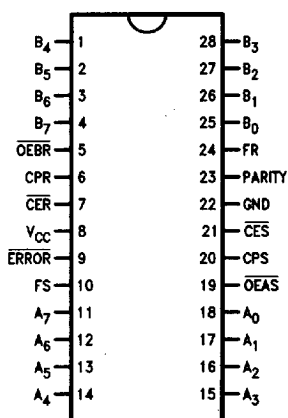
Note 1: Devices also available in 13" reel. Use suffix = SCX and QCX.

Logic Symbols

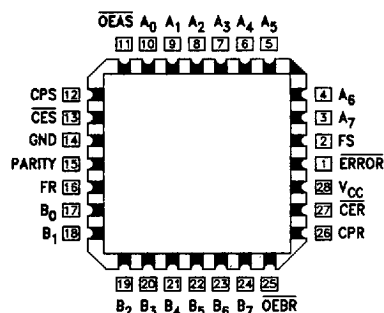


Connection Diagrams

Pin Assignment for SOIC



Pin Assignment for PCC



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Unit Loading/Fan Out: See Section 2 for U.L. definitions

Pin Names	Description	74F	
		U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
A ₀ –A ₇	A-to-B Port Data Inputs or B-to-A TRI-STATE	3.5/1.083 150/40 (33.3)	70 μ A/–0.65 mA –3 mA/24 mA (20 mA)
B ₀ –B ₇	B-to-A Transceiver Inputs or A-to-B TRI-STATE Output	3.5/1.083 600/106.6 (80)	70 μ A/–0.65 mA –12 mA/64 mA (48 mA)
FR	B Port Flag Output	50/33.3	–1 mA/20 mA
FS	A Port Flag Output	50/33.3	–1 mA/20 mA
PARITY	Parity Bit Transceiver Input or Output	3.5/1.083 600/106.6 (50)	70 μ A/–0.65 mA –12 mA/64 mA (48 mA)
ERROR	Parity Check Output (Active LOW)	50/33.3	–1 mA/20 mA
CER	R Registers Clock Enable Input (Active LOW)	1.0/1.0	20 μ A/–0.6 mA
CES	S Registers Clock Enable Input (Active LOW)	1.0/1.0	20 μ A/–0.6 mA
CPR	R Registers Clock Pulse Input (Active Rising Edge)	1.0/1.0	20 μ A/–0.6 mA
CPS	S Registers Clock Pulse Input (Active Rising Edge)	1.0/1.0	20 μ A/–0.6 mA
OEBR	B Port and PARITY Output Enable (Active LOW) and Clear FR Input (Active Rising Edge)	1.0/2.0	20 μ A/–1.2 mA
OEAS	A Port Output Enable (Active LOW) and Clear FS Input (Active Rising Edge)	1.0/2.0	20 μ A/–1.2 mA

Functional Description

Data applied to the A-inputs are entered and stored in the R register on the rising edge of the CPR Clock Pulse, provided that the Clock Enable ($\overline{CE}$) is LOW; simultaneously, the status flip-flop is set and the flag (FR) output goes HIGH. As the Clock Enable ($\overline{CE}$) returns to HIGH, the data will be held in the R register. These data entered from the A-inputs will appear at the B-port I/O pins after the Output Enable ($\overline{OE}$) has gone LOW. When $\overline{OE}$ is LOW, a parity bit appears at the PARITY pin, which will be set HIGH when there is an even number of 1s or all 0s at the Q outputs of the R register. After the data is assimilated, the receiving system clears the flag FR by changing the signal at the $\overline{OE}$ pin from LOW to HIGH.

Data flow from B-to-A proceeds in the same manner described for A-to-B flow. A LOW at the $\overline{CES}$ pin and a LOW-to-HIGH transition at CPS pin enters the B-input data and the parity-input data into the S registers and the parity register respectively and set the flag output FS to HIGH. A LOW signal at the $\overline{OEAS}$ pin enables the A-port I/O pins and a LOW-to-HIGH transition of the $\overline{OEAS}$ signal clears the FS flag. When $\overline{OEAS}$ is LOW, the parity check output ERROR will be HIGH if there is an odd number of 1s at the Q outputs of the S registers and the parity register. The flag FS can be cleared by a LOW-to-HIGH transition of the $\overline{OEAS}$ signal.

Register Function Table

(Applies to R or S Register)

Inputs			Internal Q	Function
D	CP	$\overline{CE}$		
X	X	H	NC	Hold Data
L		L	L	Load Data
H		L	H	Load Data
X	↑	L	NC	Keep Old Data

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Immaterial
 = LOW-to-HIGH Transition
 ↑ = Not LOW-to-HIGH Transition
 NC = No Change

Output Control

$\overline{OE}$	Internal Q	A or B Outputs	Function
H	X	Z	Disable Output
L	L	L	Enable Output
L	H	H	Enable Output

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Immaterial
 Z = High Impedance

Flag Flip-Flop Function Table

(Applies to R or S Flag Flip-Flop)

Inputs			Flag Output	Function
$\overline{CE}$	CP	$\overline{OE}$		
H	X	↑	NC	Hold Flag
L		↑	H	Set Flag
X	X		L	Clear Flag

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Immaterial
 = LOW-to-HIGH Transition
 = Not LOW-to-HIGH Transition
 NC = No Change

Parity Generation Function

$\overline{OE}$	Number of HIGHS in the Q Outputs of the R Register	Parity Output
H	X	Z
L	0, 2, 4, 6, 8	H
L	1, 3, 5, 7	L

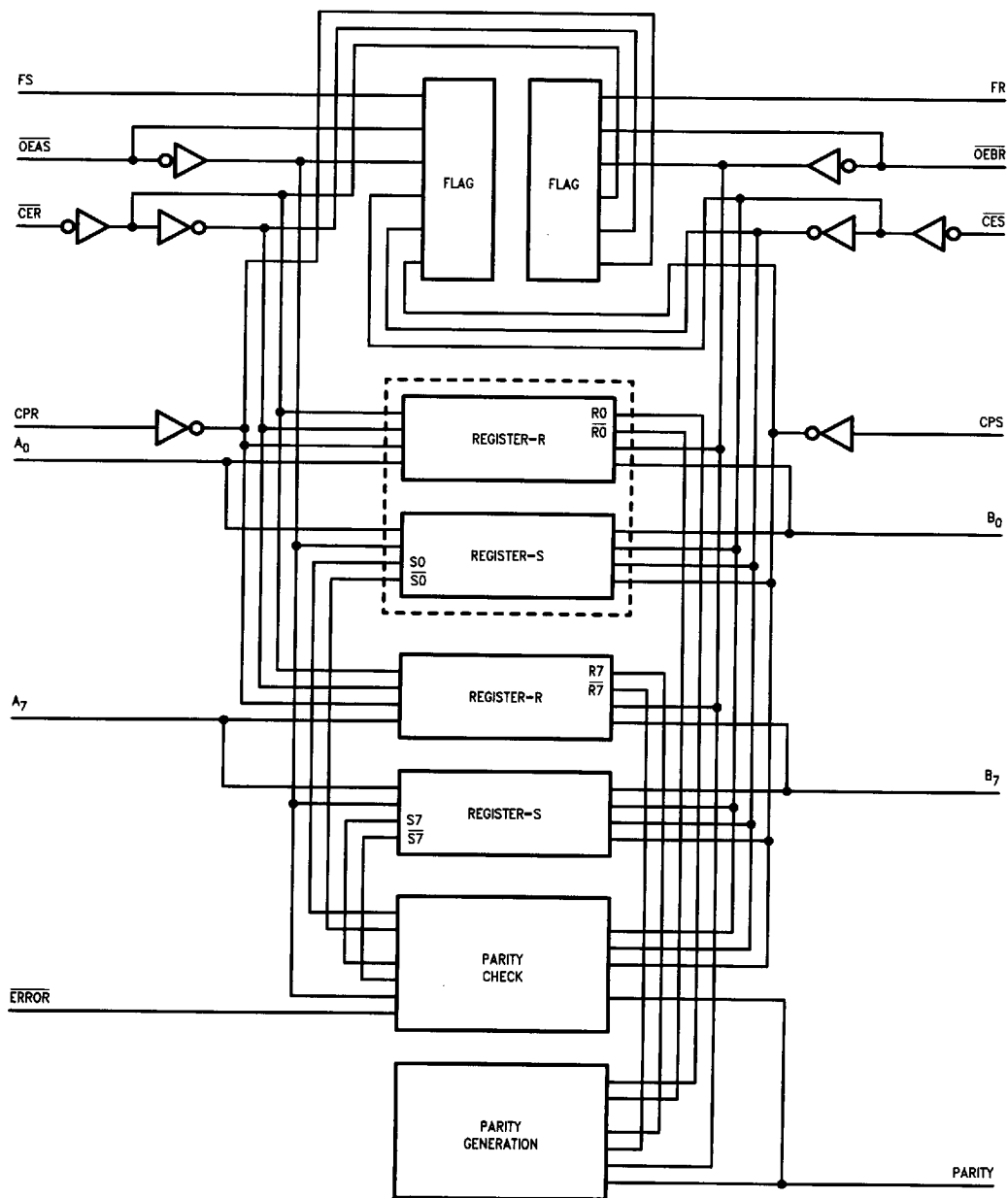
H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Immaterial
 Z = High Impedance

Parity Check Function

$\overline{OEAS}$	Number of HIGHS in the Q Outputs of the S Register	Parity Input	ERROR Output
H	X	X	H
L	0, 2, 4, 6, 8	L	L
L	1, 3, 5, 7	L	H
L	0, 2, 4, 6, 8	H	H
L	1, 3, 5, 7	H	L

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Immaterial

Block Diagram



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Absolute Maximum Ratings (Note 1)

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +175°C
V _{CC} Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V _{CC} = 0V)	
Standard Output	-0.5V to V _{CC}
TRI-STATE Output	-0.5V to +5.5V

Current Applied to Output in LOW State (Max)

twice the rated I_{OL} (mA)

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature	0°C to +70°C
Commercial	
Supply Voltage	+4.5V to +5.5V
Commercial	

DC Electrical Characteristics

Symbol	Parameter	74F			Units	V _{CC}	Conditions
		Min	Typ	Max			
V _{IH}	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V _{IL}	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V _{CD}	Input Clamp Diode Voltage			-1.2	V	Min	I _{IN} = -18 mA ($\overline{\text{CE}}\text{R}$, $\overline{\text{CE}}\text{S}$, CPR, CPS, $\overline{\text{OE}}\text{BR}$, $\overline{\text{OE}}\text{AS}$)
V _{OH}	Output HIGH Voltage	74F 10% V _{CC} 74F 10% V _{CC} 74F 10% V _{CC} 74F 5% V _{CC} 74F 5% V _{CC}	2.5 2.4 2.0 2.7 2.7		V	Min	I _{OH} = -1 mA (FR, FS, ERROR, A _n) I _{OH} = -3 mA (A _n , B _n PARITY) I _{OH} = -15 mA (B _n , PARITY) I _{OH} = -1 mA (FR, FS, ERROR, A _n) I _{OH} = -3 mA (A _n , B _n , PARITY)
V _{OL}	Output LOW Voltage	74F 10% V _{CC} 74F 10% V _{CC} 74F 10% V _{CC}		0.5 0.5 0.55	V	Min	I _{OL} = 20 mA (FR, FS, ERROR) I _{OL} = 24 mA (A _n) I _{OL} = 64 mA (B _n , PARITY)
I _{IH}	Input HIGH Current	74F		5.0	μA	Max	V _{IN} = 2.7V ($\overline{\text{CE}}\text{R}$, $\overline{\text{CE}}\text{S}$, CPR, CPS, $\overline{\text{OE}}\text{BR}$, $\overline{\text{OE}}\text{AS}$)
I _{BVI}	Input HIGH Current Breakdown Test	74F		7.0	μA	Max	V _{IN} = 7.0V ($\overline{\text{CE}}\text{R}$, $\overline{\text{CE}}\text{S}$, CPR, CPS, $\overline{\text{OE}}\text{BR}$, $\overline{\text{OE}}\text{AS}$)
I _{BVIT}	Input HIGH Current Breakdown (I/O)	74F		0.5	mA	Max	V _{IN} = 5.5V (A _n , B _n , PARITY)
I _{CEX}	Output HIGH Leakage Current	74F		50	μA	Max	V _{OUT} = V _{CC} (FR, FS, ERROR, A _n , B _n , PARITY)
V _{ID}	Input Leakage Test	74F	4.75		V	0.0	I _{ID} = 1.9 μA All other pins grounded
I _{OD}	Output Leakage Circuit Current	74F		3.75	μA	0.0	V _{ID} = 150 mV All other pins grounded
I _{IL}	Input LOW Current			-0.6 -1.2	mA	Max	V _{IN} = 0.5V ($\overline{\text{CE}}\text{R}$, $\overline{\text{CE}}\text{S}$, CPR, CPS) V _{IN} = 0.5V ($\overline{\text{OE}}\text{BR}$, $\overline{\text{OE}}\text{AS}$)
I _{IH} + I _{OZH}	Output Leakage Current			70	μA	Max	V _{OUT} = 2.7V (A _n , B _n , PARITY)
I _{IL} + I _{OZL}	Output Leakage Current			-650	μA	Max	V _{OUT} = 0.5V (A _n , B _n , PARITY)
I _{OS}	Output Short-Circuit Current		-60 -100	-175 -250	mA	Max	V _{OUT} = 0V (FR, FS, ERROR, A _n) V _{OUT} = 0V (B _n , PARITY)
I _{ZZ}	Bus Drainage Test			500	μA	0.0V	V _{OUT} = 5.25V (A _n , B _n , PARITY)
I _{CC} H	Power Supply Current		100	150	mA	Max	V _O = HIGH
I _{CC} L	Power Supply Current		100	150	mA	Max	V _O = LOW
I _{CC} Z	Power Supply Current		110	165	mA	Max	V _O = HIGH Z

AC Electrical Characteristics: See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F			74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A, V_{CC} = \text{Com}$ $C_L = 50\text{ pF}$			
		Min	Typ	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay CPS or CPR to A_n or B_n	3.5 4.0	6.0 7.0	8.0 9.5	3.0 3.5	9.0 10.5	ns	2-3
t_{PLH}	Propagation Delay CPS or CPR to FS or FR	3.0	5.5	7.5	2.5	8.5	ns	2-3
t_{PHL}	Propagation Delay $\overline{\text{OEAS}}$ to FS	3.5	6.0	8.0	3.0	9.0	ns	2-3
t_{PLH} t_{PHL}	Propagation Delay CPR to Parity	8.0 8.5	14.0 14.5	18.0 18.5	7.0 7.5	20.0 20.5	ns	2-3
t_{PLH} t_{PHL}	Propagation Delay CPS to ERROR	8.0 7.5	13.5 13.0	17.5 16.5	7.0 6.5	19.5 18.5	ns	2-3
t_{PLH} t_{PHL}	Propagation Delay $\overline{\text{OEAS}}$ to ERROR	3.5 3.0	6.0 5.0	8.0 7.0	3.0 2.5	9.0 8.0	ns	2-3
t_{PZH} t_{PZL}	Enable Time $\overline{\text{OEAS}}$ or $\overline{\text{OEBR}}$ to B_n or A_n	3.0 3.5	5.5 7.0	7.5 9.5	2.5 3.0	8.5 10.5	ns	2-5
t_{PHZ} t_{PLZ}	Disable Time $\overline{\text{OEAS}}$ or $\overline{\text{OEBR}}$ to B_n or A_n	3.0 3.0	6.5 5.5	8.5 7.5	2.5 2.5	9.5 8.5		
t_{PZH} t_{PZL}	Enable Time $\overline{\text{OEBR}}$ to Parity	3.0 3.5	4.5 6.0	7.5 9.5	2.5 3.0	8.5 10.5		
t_{PHZ} t_{PLZ}	Disable Time $\overline{\text{OEBR}}$ to Parity	3.0 3.0	5.5 6.5	8.5 7.5	2.5 2.5	9.5 8.5	ns	2-5

AC Operating Requirements: See Section 2 for Waveforms

Symbol	Parameter	74F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$		$T_A, V_{CC} = \text{Com}$			
		Min	Max	Min	Max		
$t_s(\text{H})$ $t_s(\text{L})$	Setup Time, HIGH or LOW A_n or B_n or Parity to CPS or CPR	7.5 4.5		8.5 5.0		ns	2-6
$t_h(\text{H})$ $t_h(\text{L})$	Hold Time, HIGH or LOW A_n or B_n or Parity to CPS or CPR	0 0		0 0			
$t_s(\text{H})$ $t_s(\text{L})$	Setup, Time HIGH or LOW CES or CER to CPS or CPR	6.0 10.0		7.0 11.5		ns	2-6
$t_h(\text{H})$ $t_h(\text{L})$	Hold Time, HIGH or LOW CES or CER to CPS or CPR	0 0		0 0			
$t_w(\text{H})$ $t_w(\text{L})$	Pulse Width, HIGH or LOW CPS or CPR	4.0 6.0		4.5 7.0		ns	2-4