

74F794 8-Bit Register with Readback

General Description

The 'F794 is an 8-bit register with readback capability designed to store data as well as read the register information back onto the data bus. The I/O bus (D bus) has TRI-STATE® outputs. Current sinking capability is 64 mA on both the D and Q busses.

Data is loaded into the registers on the low-to-high transition of the clock (CP). The output enable (\overline{OE}) is used to enable data on D_0 - D_7 . When \overline{OE} is low, the output of the registers is enabled on D_0 - D_7 , enabling D as an output bus. When

\overline{OE} is high, D_0 - D_7 are inputs to the registers configuring D as an input bus.

Features

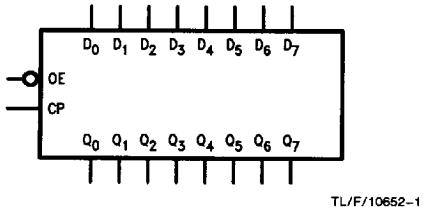
- TRI-STATE outputs on the I/O port
- D and Q output sink capability of 64 mA
- Guaranteed 4000V minimum ESD protection
- Functionally and pin equivalent to the 'LS794

Ordering Code: See Section 11

Commercial	Package Number	Package Description
74F794PC	N20A	20-Lead (0.300" Wide) Molded Dual-In-Line
74F794SC (Note 1)	M20B	20-Lead (0.300" Wide) Molded Small Outline, JEDEC

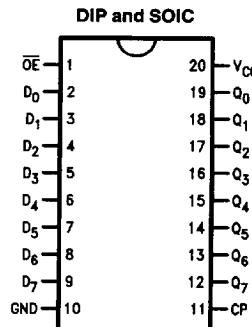
Note 1: Devices also available in 13" reel. Use suffix = SCX.

Logic Symbol



TL/F/10652-1

Connection Diagram



TL/F/10652-2

Input Loading/Fan-Out

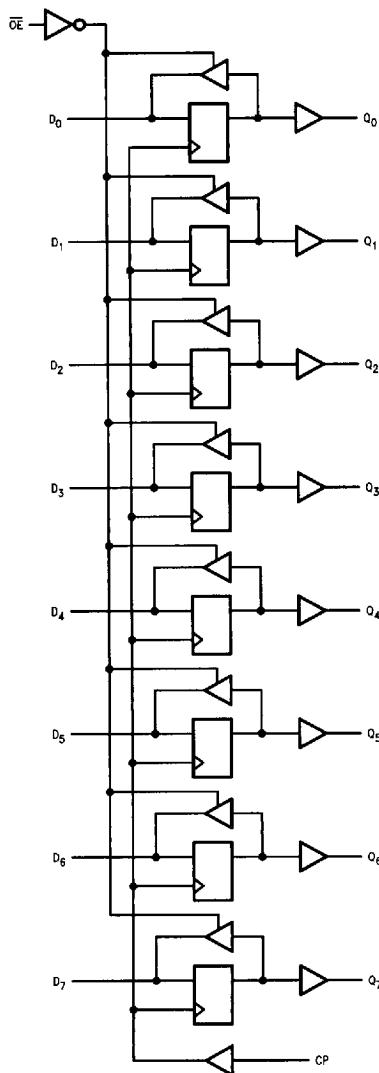
Pin Names	Description	74F High/Low	
		(U.L.)	Current
\overline{OE}	Output Enable Input	1.0/1.0	20 μ A/-0.6 mA
CP	Clock Pulse Inputs	1.0/1.0	20 μ A/-0.6 mA
D_0 - D_7	D Bus Inputs/ TRI-STATE Outputs	3.5/1.083	70 μ A/-650 μ A -15 mA/64 mA
Q_0 - Q_7	Q Bus Outputs	750/106.6	-15 mA/64 mA

Truth Table

Inputs		Outputs	
CP	\overline{OE}	Q	D
L or H or ↓	L	Q_n	Output, Q
L or H or ↓	H	Q_n	Input
↑	L	Q_n	Output, Q^*
↑	H	D	Input

*In this case the output of the register is clocked to the inputs and the overall Q output is unchanged at Q_n .

Logic Diagram



TL/F/10652-3

Absolute Maximum Ratings (Note 1)

Storage Temperature	−65°C to + 150°C			Voltage Applied to Output	
Ambient Temperature under Bias	−55° to + 125°C			In HIGH State (with $V_{CC} = 0V$)	
Junction Temperature under Bias Plastic	−55°C to + 175°C −55°C to + 150°C			Standard Output	−0.5V to V_{CC}
V_{CC} Pin Potential to Ground Pin	−0.5V to + 7.0V			TRI-STATE Output	−0.5V to + 5.5V
Input Voltage (Note 2)	−0.5V to + 7.0V			Current Applied to Output in LOW State (Max)	Twice the Rated I_{OL} (mA)
Input Current (Note 2)	−30 mA to + 5.0 mA			ESD Last Passing Voltage (Min)	4000V
ESD Last Passing Voltage (Min)	4000V				

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Voltage Applied to Output In HIGH State (with $V_{CC} = 0V$)	−0.5V to V_{CC}
Standard Output	−0.5V to + 5.5V
TRI-STATE Output	

Current Applied to Output in LOW State (Max)	Twice the Rated I_{OL} (mA)
ESD Last Passing Voltage (Min)	4000V

Recommended Operating Conditions

Free Air Ambient Temperature Commercial	0°C to 70°C
Supply Voltage Commercial	+ 4.5V to + 5.5V

DC Characteristics over Operating Temperature Range unless otherwise specified

Symbol	Parameter	74F			Units	V_{CC}	Conditions
		Min	Typ	Max			
V_{IH}	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V_{IL}	Input LOW Voltage		0.8		V		Recognized as a LOW Signal
V_{CD}	Input Clamp Diode Voltage			−1.2	V	Min	$I_{IN} = -18\text{ mA}$
V_{OH}	Output HIGH Voltage	2.4 2.0	2.8 2.44		V	Min	$I_{OH} = -3\text{ mA}$ $I_{OH} = -15\text{ mA}$
V_{OL}	Output LOW Voltage		0.45	0.55	V	Min	$I_{OL} = 64\text{ mA}$
I_{IH}	Input HIGH Current	74F		5.0	μA	Max	$V_{IN} = 2.7\text{ V}$
I_{BVI}	Input HIGH Current Breakdown Test	74F		7.0	μA	Max	$V_{IN} = 7.0\text{ V}$ (\overline{OE} , CP)
I_{BVIT}	Input HIGH Current Breakdown (I/O)	74F		0.5	mA	Max	$V_{IN} = 5.5\text{ V}$ (D_n)
I_{CEX}	Output HIGH Leakage Current	74F		50	μA	Max	$V_{OUT} = V_{CC}$
V_{ID}	Input Leakage Test	74F	4.75		V	0.0	$I_{ID} = 1.9\text{ }\mu\text{A}$ All Other Pins Grounded
I_{OD}	Output Leakage Circuit Current	74F		3.75	μA	0.0	$V_{IOD} = 150\text{ mV}$ All Other Pins Grounded
I_{IL}	Input LOW Current			−0.6	mA	Max	$V_{IN} = 0.5\text{ V}$ (\overline{OE} , CP)

DC Characteristics over Operating Temperature Range unless other specified (Continued)

Symbol	Parameter	74F			Units	V _{CC}	Conditions
		Min	Typ	Max			
I _{OS}	Output Short-Circuit Current	-100	-	-225	mA	Max	V _{OUT} = 0V
I _{IH} + I _{OZH}	Output Leakage Current			70	μA	Max	V _{OUT} = 2.7V (Dn)
I _{IL} + I _{OZL}	Output Leakage Current			-650	μA	Max	V _{OUT} = 0.5V (Dn)
V _{ID}	Input Leakage Test 74F	4.75			V	0.0	I _{ID} = 1.9 μA All Other Pins Grounded
I _{OD}	Output Circuit Leakage Current 74F		3.75		μA	0.0	V _{IOD} = 150 mV All Other Pins Grounded
I _{ZZ}	Bus Drainage Test		100		μA	0.0	V _{OUT} = 5.25V
I _{CCH}	Power Supply Current		65		mA	Max	V _O = HIGH
I _{CCL}	Power Supply Current		80		mA	Max	V _O = LOW
I _{CCZ}	Power Supply Current		80		mA	Max	V _O = HIGH Z

AC Characteristics: See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F			74F		Fig. No.	
		T _A = +25°C V _{CC} = +5.0V C _L = 50 pF			T _A , V _{CC} = Comm C _L = 50 pF			
		Min	Typ	Max	Min	Max		
f _{MAX}	Max. Clock Frequency	90			90		MHz 2-1	
t _{PLH} t _{PHL}	Propagation Delay CP to Qn	2.5 2.5	7.0 8.0		2.5 2.5	8.0 9.0	ns 2-3	
t _{PZH} t _{PZL}	Output Enable Time	2.3 2.0	8.5 10.0		2.0 2.0	9.0 10.5	ns 2-5	
t _{PHZ} t _{PLZ}	Output Disable Time	1.0 1.0	7.0 7.0		1.0 1.0	8.0 8.0	ns 2-5	
t _{S(H)} t _{S(L)}	Setup Time, HIGH or LOW Bus to Clock	4.0 4.0			4.0 4.0		ns 2-6	
t _{H(H)} t _{H(L)}	Hold Time, HIGH or LOW Bus to Clock	1.5 1.5			1.5 1.5		ns 2-6	
t _{w(H)}	Clock Pulse Width HIGH or LOW	5.8 5.8			5.8 5.8		ns 2-14	