

54F/74F827 • 74F828 10-Bit Buffers/Line Drivers

General Description

The 'F827 and 'F828 10-bit bus buffers provide high performance bus interface buffering for wide data/address paths or buses carrying parity. The 10-bit buffers have NOR output enables for maximum control flexibility.

The 'F827 and 'F828 are functionally- and pin-compatible to AMD's Am29827 and Am29828. The 'F828 is an inverting version of the 'F827.

Features

- TRI-STATE® output
- 'F828 is inverting
- Direct replacement for AMD's Am29827 and Am29828

Ordering Code: See Section 11

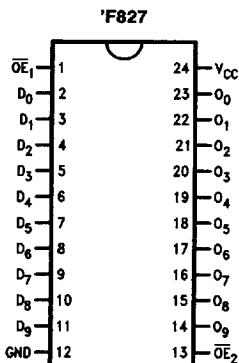
Commercial	Military	Package Number	Package Description
74F827SPC		N24C	24-Lead (0.300" Wide) Molded Dual-In-Line
	54F827SDM (Note 2)	J24F	24-Lead (0.300" Wide) Ceramic Dual-In-Line
74F827SC (Note 1)		M24B	24-Lead (0.300" Wide) Molded Small Outline, JEDEC
	54F827FM (Note 2)	W24C	24-Lead Cerpack
	54F827LM (Note 2)	E28A	24-Lead Ceramic Leadless Chip Carrier, Type C
74F828SPC		N24C	24-Lead (0.300" Wide) Molded Dual-In-Line
74F828SC (Note 1)		M24B	24-Lead (0.300" Wide) Molded Small Outline, JEDEC

Note 1: Devices also available in 13" reel. Use suffix = SCX.

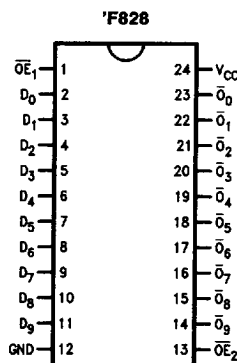
Note 2: Military grade device with environmental and burn-in processing. Use suffix = SDMQB, FMQB and LMQB.

Connection Diagrams

Pin Assignment for
DIP, Flatpak and SOIC

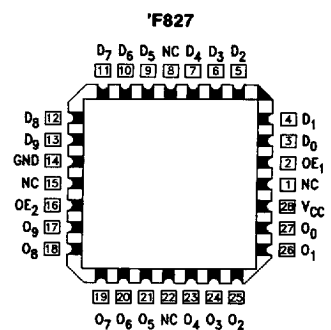


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Pin Assignment
for LCC

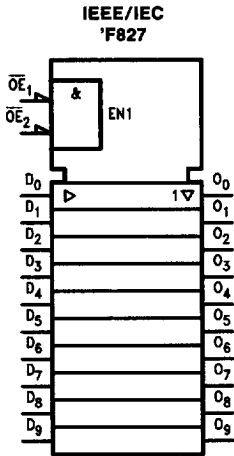


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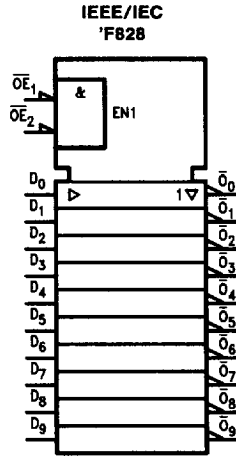
6501122 0082658 974

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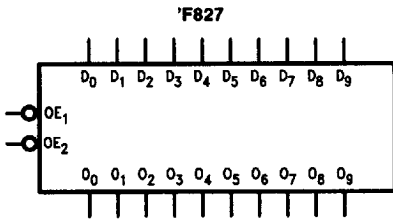
Logic Symbols



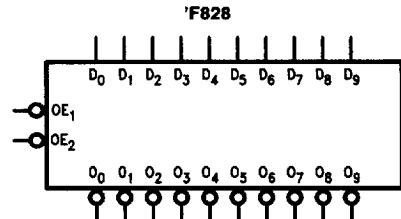
TL/F/9598-6



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TL/F/9598-3



TL/F/9598-10

Unit Loading/Fan Out: See Section 2 for U.L. definitions

Pin Names	Description	54F/74F	
		U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
$\overline{OE}_1, \overline{OE}_2$	Output Enable Input	1.0/1.0	20 μ A/ -0.6 mA
D_0-D_7	Data Inputs	1.0/1.0	20 μ A/ -0.6 mA
O_0-O_7	Data Outputs, TRI-STATE	600/106.6 (80)	-12 mA/64 mA (48 mA)

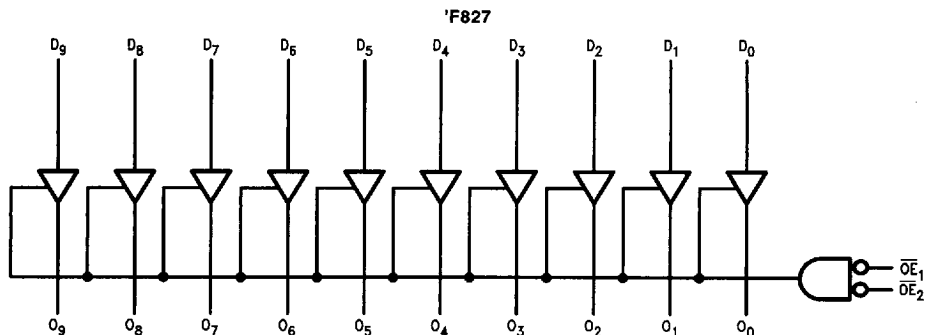
Functional Description

The 'F827 and 'F828 are line drivers designed to be employed as memory address drivers, clock drivers and bus-oriented transmitters/receivers which provide improved PC board density. The devices have TRI-STATE outputs controlled by the Output Enable ($\overline{OE}$) pins. The outputs can sink 64 mA (48 mA mil) and source 15 mA. Input clamp diodes limit high-speed termination effects.

Function Table

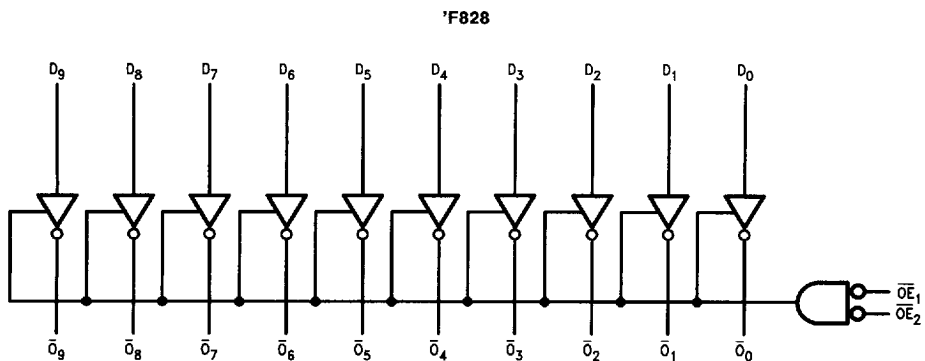
Inputs		Outputs		Function
$\overline{OE}$	D_n	O_n		
		'F827	'F828	
L	H	H	L	Transparent
L	L	L	H	Transparent
H	X	Z	Z	High Z

H = HIGH Voltage level
L = LOW Voltage level
Z = High Impedance
X = Immaterial

Logic Diagrams

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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.



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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +175°C
Plastic	−55°C to +150°C

V _{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
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Input Voltage (Note 2)	−0.5V to +7.0V
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Input Current (Note 2)	−30 mA to +5.0 mA
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Voltage Applied to Output in HIGH State (with V _{CC} = 0V)	
Standard Output	−0.5V to V _{CC}
TRI-STATE Output	−0.5V to +5.5V

Current Applied to Output in LOW State (Max)	twice the rated I _{OL} (mA)
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Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	−55°C to +125°C
Commercial	0°C to +70°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V

DC Electrical Characteristics

Symbol	Parameter		54F/74F			Units	V _{CC}	Conditions
			Min	Typ	Max			
V _{IH}	Input HIGH Voltage		2.0			V		Recognized as a HIGH Signal
V _{IL}	Input LOW Voltage				0.8	V		Recognized as a LOW Signal
V _{CD}	Input Clamp Diode Voltage				−1.2	V	Min	I _{IN} = −18 mA
V _{OH}	Output HIGH Voltage	54F 10% V _{CC} 54F 10% V _{CC} 74F 10% V _{CC} 74F 10% V _{CC} 74F 5% V _{CC}	2.4 2.0 2.4 2.0 2.7			V	Min	I _{OH} = −3 mA I _{OH} = −12 mA I _{OH} = −3 mA I _{OH} = −15 mA I _{OH} = −3 mA
V _{OL}	Output LOW Voltage	54F 10% V _{CC} 74F 10% V _{CC}		0.55 0.55		V	Min	I _{OL} = 48 mA I _{OL} = 64 mA
I _{IH}	Input HIGH Current	54F 74F		20.0 5.0		μA	Max	V _{IN} = 2.7V
I _{BVI}	Input HIGH Current Breakdown Test	54F 74F		100 7.0		μA	Max	V _{IN} = 7.0V
I _{CEX}	Output HIGH Leakage Current	54F 74F		250 50		μA	Max	V _{OUT} = V _{CC}
V _{ID}	Input Leakage Test	74F	4.75			V	0.0	I _{ID} = 1.9 μA All Other Pins Grounded
I _{OD}	Output Leakage Circuit Current	74F		3.75		μA	0.0	V _{IOD} = 150 mV All Other Pins Grounded
I _{IL}	Input LOW Current			−0.6		mA	Max	V _{IN} = 0.5V
I _{OZH}	Output Leakage Current			50		μA	Max	V _{OUT} = 2.7V
I _{OZL}	Output Leakage Current			−50		μA	Max	V _{OUT} = 0.5V
I _{OS}	Output Short-Circuit Current		−100	−225		mA	Max	V _{OUT} = 0V

DC Electrical Characteristics (Continued)

Symbol	Parameter	54F/74F			Units	V _{CC}	Conditions
		Min	Typ	Max			
I _{ZZ}	Bus Drainage Test			500	μA	0.0V	V _{OUT} = 5.25V
I _{CCH}	Power Supply Current ('F827)		30	45	mA	Max	V _O = HIGH
I _{CCL}	Power Supply Current ('F827)		60	90	mA	Max	V _O = LOW
I _{CCZ}	Power Supply Current ('F827)		40	60	mA	Max	V _O = HIGH Z
I _{CCH}	Power Supply Current ('F828)		14	20	mA	Max	V _O = HIGH
I _{CCL}	Power Supply Current ('F828)		56	85	mA	Max	V _O = LOW
I _{CCZ}	Power Supply Current ('F828)		35	50	mA	Max	V _O = HIGH Z

AC Electrical Characteristics: See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F			54F		74F		Units	Fig. No.
		T _A = +25°C V _{CC} = +5.0V C _L = 50 pF			T _A , V _{CC} = Mil C _L = 50 pF		T _A , V _{CC} = Com C _L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
t _{PLH}	Propagation Delay	1.0	3.0	5.5	1.0	7.5	1.0	6.5	ns	2-3
t _{PHL}	Data to Output ('F827)	1.5	3.3	5.5	1.5	7.0	1.5	6.0		
t _{PLH}	Propagation Delay	1.0	3.0	5.0			1.0	5.5	ns	2-3
t _{PHL}	Data to Output ('F828)	1.0	2.0	4.0			1.0	4.0		
t _{PZH}	Output Enable Time	3.0	5.7	9.0	2.5	10.0	2.5	9.5	ns	2-5
t _{PZL}	OE to O _n	3.5	6.8	11.5	3.0	12.5	3.0	12.0		
t _{PHZ}	Output Disable Time	1.5	3.3	8.0	1.5	9.0	1.5	8.5	ns	2-5
t _{PLZ}	OE to O _n	1.0	3.5	8.0	1.0	9.0	1.0	8.5		