

74F845

8-Bit Transparent Latch

General Description

The 'F845 bus interface latch is designed to eliminate the extra packages required to buffer existing latches and provide extra data width for wider address/data paths or buses carrying parity.

The 'F845 is functionally- and pin-compatible with AMD's Am29845.

Features

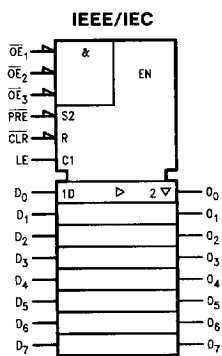
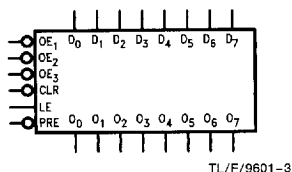
- TRI-STATE® outputs
- Direct replacement for AMD's Am29845

Ordering Code: See Section 11

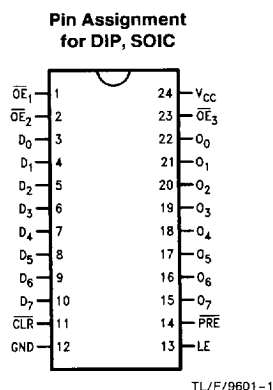
Commercial	Package Number	Package Description
74F845SPC	N24C	24-Lead (0.300" Wide) Molded Dual-In-Line
74F845SC (Note 1)	M24B	24-Lead (0.300" Wide) Molded Small Outline, JEDEC

Note 1: Devices also available in 13" reel. Use suffix = SCX.

Logic Symbols



Connection Diagram



Unit Loading/Fan Out: See Section 2 for U.L. Definitions

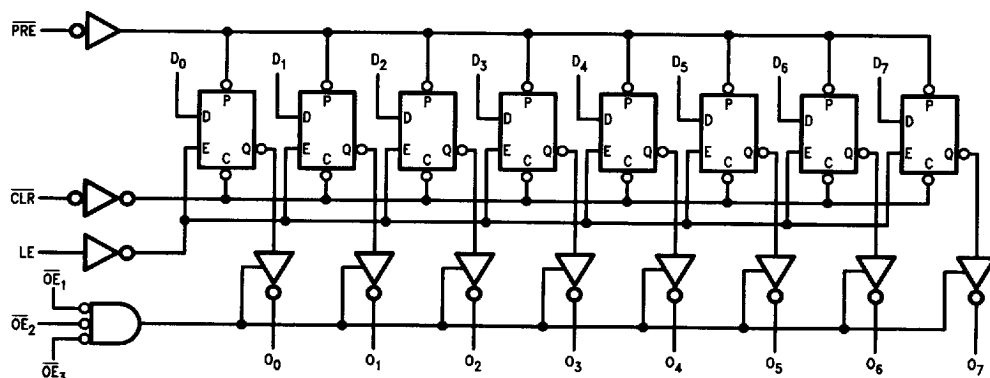
Pin Names	Description	74F	
		U.L. HIGH/LOW	Input I _{IH} /I _{IL} Output I _{OH} /I _{OL}
D ₀ -D ₇	Data Inputs	1.0/1.0	20 μ A/ -0.6 mA
O ₀ -O ₇	Data Outputs	150/40	-3.0 μ A/24 mA
$\overline{OE}_1$ - $\overline{OE}_3$	Output Enables	1.0/1.0	20 μ A/ -0.6 mA
LE	Latch Enable	1.0/1.0	20 μ A/ -0.6 mA
$\overline{CLR}$	Clear	1.0/1.0	20 μ A/ -0.6 mA
PRE	Preset	1.0/1.0	20 μ A/ -0.6 mA

Functional Description

The 'F845 consists of eight D-type latches with TRI-STATE outputs. The flip-flops appear transparent to the data when Latch Enable (LE) is HIGH. This allows asynchronous operation as the output transition follows the data in transition.

On the LE HIGH-to-LOW transition, the data that meets the setup times is latched. Data appears on the bus when the output Enable ($\overline{OE}$) is LOW. When $\overline{OE}$ is HIGH, the bus output is in the high impedance state.

Logic Diagram



TL/F/9601-4

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Function Table

Inputs					Internal	Output	Function
CLR	PRE	$\overline{OE}$	LE	D	Q	O	
H	H	H	X	X	X	Z	High Z
H	H	H	H	L	L	Z	High Z
H	H	H	H	H	H	Z	High Z
H	H	H	L	X	NC	Z	Latched
H	H	L	H	L	L	L	Transparent
H	H	L	H	H	H	H	Transparent
H	H	L	L	X	NC	NC	Latched
H	L	L	X	X	H	H	Preset
L	H	L	X	X	L	L	Clear
L	L	L	X	X	H	H	Preset
L	H	H	L	X	L	Z	Latched
H	L	H	L	X	H	Z	Latched

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Immaterial
 Z = High Impedance
 NC = No Change

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	−55°C to +175°C
Plastic	−55°C to +150°C
V _{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V _{CC} = 0V)	
Standard Output	−0.5V to V _{CC}
TRI-STATE Output	−0.5V to +5.5V

Current Applied to Output in LOW State (Max) twice the rated I_{OL} (mA)

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature	0°C to +70°C
Commercial	
Supply Voltage	+4.5V to +5.5V
Commercial	

DC Electrical Characteristics

Symbol	Parameter	74F			Units	V _{CC}	Conditions
		Min	Typ	Max			
V _{IH}	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V _{IL}	Input LOW Voltage		0.8		V		Recognized as a LOW Signal
V _{CD}	Input Clamp Diode Voltage		−1.2		V	Min	I _{IN} = −18 mA
V _{OH}	Output HIGH Voltage	74F 10% V _{CC}	2.5		V	Min	I _{OH} = −1 mA
		74F 10% V _{CC}	2.4				I _{OH} = −3 mA
		74F 5% V _{CC}	2.7				I _{OH} = −1 mA
		74F 5% V _{CC}	2.7				I _{OH} = −3 mA
V _{OL}	Output LOW Voltage	74F 10% V _{CC}		0.5	V	Min	I _{OL} = 24 mA
I _{IH}	Input HIGH Current	74F		5.0	μA	Max	V _{IN} = 2.7V
I _{BVI}	Input HIGH Current Breakdown Test	74F		7.0	μA	Max	V _{IN} = 7.0V
I _{CEX}	Output HIGH Leakage Current	74F		50	μA	Max	V _{OUT} = V _{CC}
V _{ID}	Input Leakage Test	74F	4.75		V	0.0	I _{ID} = 1.9 μA All Other Pins Grounded
I _{OD}	Output Leakage Circuit Current	74F		3.75	μA	0.0	V _{ID} = 150 mV All Other Pins Grounded
I _{IL}	Input LOW Current		−0.6		mA	Max	V _{IN} = 0.5V
I _{OZH}	Output Leakage Current		50		μA	Max	V _{OUT} = 2.7V
I _{OZL}	Output Leakage Current		−50		μA	Max	V _{OUT} = 0.5V
I _{OS}	Output Short-Circuit Current	−60	−150		mA	Max	V _{OUT} = 0V
I _{ZZ}	Bus Drainage Test		500		μA	0.0V	V _{OUT} = 5.25V
I _{CCZ}	Power Supply Current		63	85	mA	Max	V _O = HIGH Z

AC Electrical Characteristics: See Section 2 for Waveforms and Load Configurations

Symbol	Parameter	74F			74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$			$T_A, V_{CC} = \text{Com}$ $C_L = 50\text{ pF}$			
		Min	Typ	Max	Min	Max		
t_{PLH}	Propagation Delay	2.5	4.8	8.0	2.0	9.0	ns	2-3
t_{PHL}	D_n to O_n	1.5	3.6	6.5	1.5	7.0		
t_{PLH}	Propagation Delay	5.0	8.1	12.0	4.5	13.5	ns	2-3
t_{PHL}	LE to O_n	2.0	4.4	7.5	2.0	8.0		
t_{PLH}	Propagation Delay	3.0	5.9	10.0	2.5	11.0	ns	2-3
	PRE to O_n							
t_{PHL}	Propagation Delay	3.0	6.5	10.0	2.5	11.0	ns	2-3
	CLR to O_n							
t_{PZH}	Output Enable Time	2.5	5.8	9.5	2.0	10.5	ns	2-5
t_{PZL}	$\overline{OE}$ to O_n	2.5	7.6	12.0	2.0	13.0		
t_{PHZ}	Output Disable Time	1.0	3.1	7.5	1.0	8.5	ns	2-5
t_{PLZ}	$\overline{OE}$ to O_n	1.0	2.8	6.5	1.0	7.5		

AC Operating Requirements: See Section 2 for Waveforms

Symbol	Parameter	74F		74F		Units	Fig. No.
		$T_A = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$		$T_A, V_{CC} = \text{Com}$			
		Min	Max	Min	Max		
t_s (H) t_s (L)	Setup Time, HIGH or LOW D_n to LE	2.0 2.0		2.5 2.5		ns	2-6
t_h (H) t_h (L)	Hold Time, HIGH or LOW D_n to LE	2.5 3.0		3.0 3.5		ns	2-6
t_w (H)	LE Pulse Width, HIGH	4.0		4.0		ns	2-4
t_w (L)	$\overline{\text{PRE}}$ Pulse Width, LOW	5.0		5.0		ns	2-4
t_w (L)	$\overline{\text{CLR}}$ Pulse Width, LOW	5.0		5.0		ns	2-4
t_{rec}	$\overline{\text{PRE}}$ Recovery Time	10.0		10.0		ns	2-6
t_{rec}	$\overline{\text{CLR}}$ Recovery Time	12.0		13.0		ns	2-6