DUAL J$\overline{K}$ FLIP-FLOP WITH SET AND RESET; POSITIVE-EDGE TRIGGER

FEATURES

- J, $\overline{K}$ inputs for easy D-type flip-flop
- Toggle flip-flop or "do nothing" mode
- Output capability: standard
- I_{CC} category: flip-flops

GENERAL DESCRIPTION

The 74HC/HCT109 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT109 are dual positive-edge triggered, J$\overline{K}$ flip-flops with individual J, $\overline{K}$ inputs, clock (CP) inputs, set ($\overline{S}_D$) and reset ($\overline{R}_D$) inputs; also complementary Q and $\overline{Q}$ outputs.

The set and reset are asynchronous active LOW inputs and operate independently of the clock input.

The J and $\overline{K}$ inputs control the state changes of the flip-flops as described in the mode select function table.

The J and $\overline{K}$ inputs must be stable one set-up time prior to the LOW-to-HIGH clock transition for predictable operation.

The J$\overline{K}$ design allows operation as a D-type flip-flop by tying the J and $\overline{K}$ inputs together.

Schmitt-trigger action in the clock input makes the circuit highly tolerant to slower clock rise and fall times.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/t_{PLH}	propagation delay nCP to nQ, n$\overline{Q}$ n$\overline{S}_D$ to nQ, n$\overline{Q}$ n$\overline{R}_D$ to nQ, n$\overline{Q}$	C_L = 15 pF V_{CC} = 5 V	15 12 12	17 14 15	ns ns ns
f_{max}	maximum clock frequency		75	61	MHz
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per flip-flop	notes 1 and 2	20	22	pF

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where:
   f_i = input frequency in MHz
   f_o = output frequency in MHz
   $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs
   C_L = output load capacitance in pF
   V_{CC} = supply voltage in V
2. For HC the condition is V_I = GND to V_{CC}
   For HCT the condition is V_I = GND to V_{CC} − 1.5 V

PACKAGE OUTLINES

16-lead DIL; plastic (SOT38Z).
16-lead mini-pack; plastic (SO16; SOT109A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 15	$1\overline{R}_D$, $2\overline{R}_D$	asynchronous reset-direct input (active LOW)
2, 14, 3, 13	1J, 2J, 1$\overline{K}$, 2$\overline{K}$	synchronous inputs; flip-flops 1 and 2
4, 12	1CP, 2CP	clock input (LOW-to-HIGH, edge-triggered)
5, 11	$1\overline{S}_D$, $2\overline{S}_D$	asynchronous set-direct input (active LOW)
6, 10	1Q, 2Q	true flip-flop outputs
7, 9	1$\overline{Q}$, 2$\overline{Q}$	complement flip-flop outputs
8	GND	ground (0 V)
16	V_{CC}	positive supply voltage

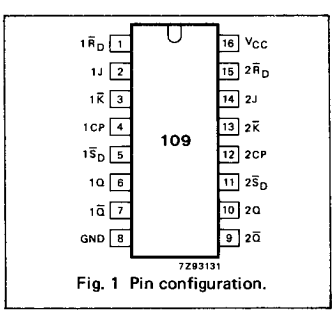

Fig. 1 Pin configuration.

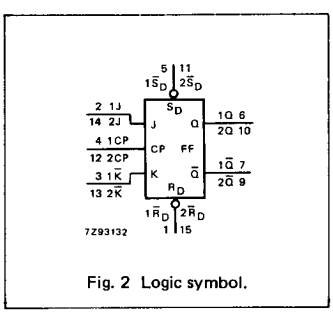

Fig. 2 Logic symbol.

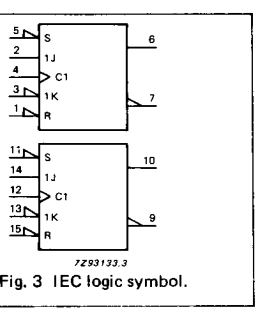

Fig. 3 IEC logic symbol.

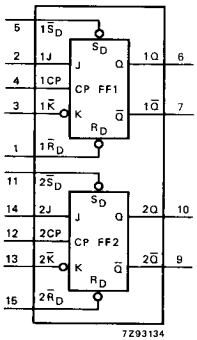

Fig. 4 Functional diagram.

FUNCTION TABLE

OPERATING MODE	INPUTS					OUTPUTS	
	$\overline{S}_D$	$\overline{R}_D$	CP	J	$\overline{K}$	Q	$\overline{Q}$
asynchronous set	L	H	X	X	X	H	L
asynchronous reset	H	L	X	X	X	L	H
undetermined	L	L	X	X	X	H	H
toggle	H	H	↑	h	l	$\overline{q}$	q
load "0" (reset)	H	H	↑	l	l	L	H
load "1" (set)	H	H	↑	h	h	H	$\underline{L}$
hold "no change"	H	H	↑	l	h	q	$\underline{\overline{q}}$

H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH CP transition
L = LOW voltage level
l = LOW voltage level one set-up time prior to the LOW-to-HIGH CP transition
q = lower case letters indicate the state of the referenced output one set-up time prior to the LOW-to-HIGH CP transition
X = don't care
↑ = LOW-to-HIGH CP transition

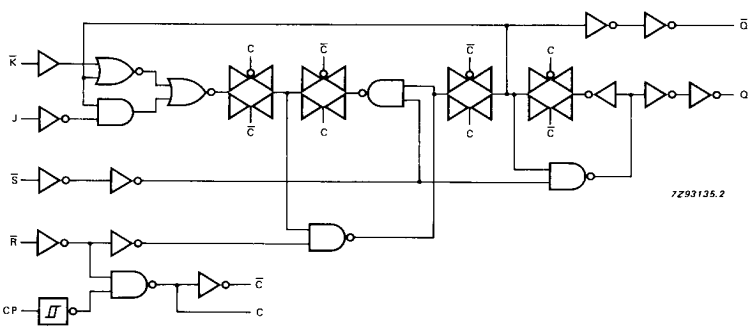

Fig. 5 Logic diagram (one flip-flop).

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: flip-flops

AC CHARACTERISTICS FOR 74HC

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay nCP to nQ, n$\overline{Q}$		50 18 14	175 35 30		220 44 37		265 53 45	ns	2.0 4.5 6.0	Fig. 6
t_{PLH}	propagation delay n$\overline{S}_D$ to nQ		30 11 9	120 24 20		150 30 26		180 36 31	ns	2.0 4.5 6.0	Fig. 7
t_{PHL}	propagation delay n$\overline{S}_D$ to n$\overline{Q}$		41 15 12	155 31 26		195 39 33		235 47 40	ns	2.0 4.5 6.0	Fig. 7
t_{PHL}	propagation delay n$\overline{R}_D$ to nQ		41 15 12	185 37 31		230 46 39		280 56 48	ns	2.0 4.5 6.0	Fig. 7
t_{PLH}	propagation delay n$\overline{R}_D$ to n$\overline{Q}$		39 14 11	170 34 29		215 43 37		255 51 43	ns	2.0 4.5 6.0	Fig. 7
t_{THL}/t_{TLH}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 6
t_W	clock pulse width HIGH or LOW	80 16 14	19 7 6		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 6
t_W	set or reset pulse width HIGH or LOW	80 16 14	14 5 4		100 20 17		120 24 20		ns	2.0 4.5 6.0	Fig. 7
t_{rem}	removal time n$\overline{S}_D$, n$\overline{R}_D$ to nCP	70 14 12	19 7 6		90 18 15		105 21 18		ns	2.0 4.5 6.0	Fig. 7
t_{su}	set-up time nJ, n$\overline{K}$ to nCP	70 14 12	17 6 5		90 18 15		105 21 18		ns	2.0 4.5 6.0	Fig. 6
t_h	hold time nJ, n$\overline{K}$ to nCP	5 5 5	0 0 0		5 5 5		5 5 5		ns	2.0 4.5 6.0	Fig. 6
f_{max}	maximum clock pulse frequency	6.0 30 35	22 68 81		5.0 24 28		4.0 20 24		MHz	2.0 4.5 6.0	Fig. 6

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: standard
I_{CC} category: flip-flops

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
nJ, $n\overline{K}$	0.35
$n\overline{R}_D$	0.35
$n\overline{S}_D$	0.35
nCP	0.35

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; $t_r = t_f$ = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay nCP to nQ, $n\overline{Q}$		20	35		44		53	ns	4.5	Fig. 6
t_{PLH}	propagation delay $n\overline{S}_D$ to nQ		13	26		33		39	ns	4.5	Fig. 7
t_{PHL}	propagation delay $n\overline{S}_D$ to $n\overline{Q}$		19	35		44		53	ns	4.5	Fig. 7
t_{PHL}	propagation delay $n\overline{R}_D$ to nQ		19	35		44		53	ns	4.5	Fig. 7
t_{PLH}	propagation delay $n\overline{R}_D$ to $n\overline{Q}$		16	32		40		48	ns	4.5	Fig. 7
t_{THL}/t_{TLH}	output transition time		7	15		19		22	ns	4.5	Fig. 6
t_W	clock pulse width HIGH or LOW	18	9		23		27		ns	4.5	Fig. 6
t_W	set or reset pulse width HIGH or LOW	16	8		20		24		ns	4.5	Fig. 7
t_{rem}	removal time $n\overline{S}_D$, $n\overline{R}_D$ to nCP	16	8		20		24		ns	4.5	Fig. 7
t_{su}	set-up time nJ, $n\overline{K}$ to nCP	18	8		23		27		ns	4.5	Fig. 6
t_h	hold time nJ, $n\overline{K}$ to nCP	3	−3		3		3		ns	4.5	Fig. 6
f_{max}	maximum clock pulse frequency	27	55		22		18		MHz	4.5	Fig. 6

AC WAVEFORMS

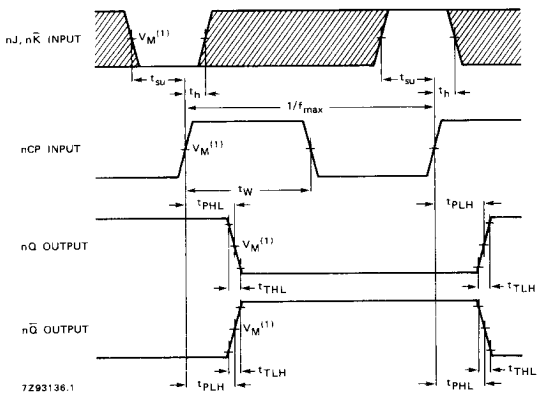

Fig. 6 Waveforms showing the clock (nCP) to output (nQ, nQ̄) propagation delays, the clock pulse width, the nJ, nK̄ to nCP set-up, the nCP to nJ, nK̄ hold times, the output transition times and the maximum clock pulse frequency.

Note to Fig. 6

The shaded areas indicate when the input is permitted to change for predictable output performance.

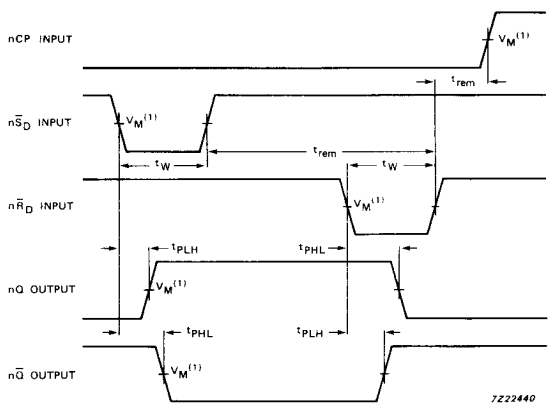

Fig. 7 Waveforms showing the set (n$\overline{S}_D$) and reset (n$\overline{R}_D$) input to output (nQ, nQ̄) propagation delays, the set and reset pulse widths and the n$\overline{R}_D$, n$\overline{S}_D$ to nCP removal time.

Note to AC waveforms

(1) HC : V_M = 50%; V_I = GND to V_{CC}.
HCT: V_M = 1.3 V; V_I = GND to 3 V.