

SUPERSEDES DATA OF MARCH 1988

NINE WIDE SCHMITT TRIGGER BUFFER; OPEN DRAIN OUTPUTS

FEATURES

- Schmitt trigger action on all data inputs
- Output capability: standard (open drain)
- I^{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT9115 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT9115 are nine wide Schmitt trigger buffer with open drain outputs and Schmitt trigger inputs.

The Schmitt trigger action in the data inputs transform slowly changing input signals into sharply defined jitter-free output signals.

The 74HC/HCT9115 have open-drain N-transistor outputs, which are not clamped by a diode connected to V_{CC}. In the OFF-state, i.e. when one input is HIGH, the output may be pulled to any voltage between GND and V_{OMax}. This allows the device to be used as a LOW-to-HIGH or HIGH-to-LOW level shifter. For digital operation and OR-tied output applications, these devices must have a pull-up resistor to establish a logic HIGH level.

The "9115" is identical to the "9114" but has non-inverting outputs.

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t _{PHL} / t _{PLZ}	propagation delay A _n to Y _n	C _L = 15 pF V _{CC} = 5 V	12	13	ns
C _I	input capacitance		3.5	3.5	pF
C _{PD}	power dissipation capacitance per buffer	notes 1 and 2	5	5	pF

GND = 0 V; T_{amb} = 25 °C; t_r = t_f = 6 ns

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz C_L = output load capacitance in pF
f_o = output frequency in MHz V_{CC} = supply voltage in V
Σ (C_L × V_{CC}² × f_o) = sum of outputs

2. For HC the condition is V_I = GND to V_{CC}
For HCT the condition is V_I = GND to V_{CC} - 1.5 V

PACKAGE OUTLINES

20-lead DIL; plastic (SOT146).

20-lead mini-pack; plastic (SO20; SOT163A).

PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 2, 3, 4, 5, 6, 7, 8, 9 10	A ₀ to A ₈ GND	data inputs ground (0 V)
19, 18, 17, 16, 15, 14, 13, 12, 11	Y ₀ to Y ₈	data outputs
20	V _{CC}	positive supply voltage

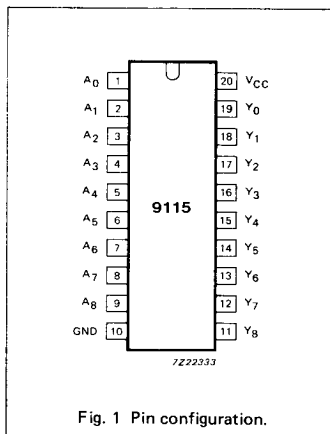


Fig. 1 Pin configuration.

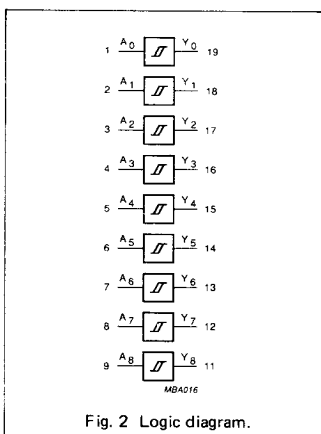


Fig. 2 Logic diagram.

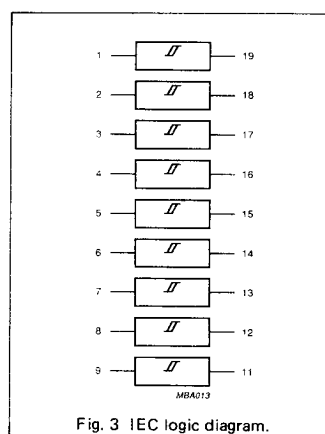
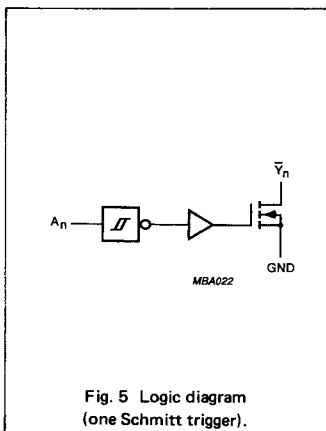
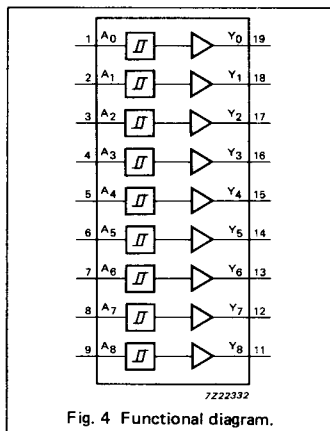


Fig. 3 IEC logic diagram.



FUNCTION TABLE

INPUTS	OUTPUTS
A_n	Y_n
L	L
H	Z

H = HIGH voltage level
 L = LOW voltage level
 Z = high impedance OFF-state

DC CHARACTERISTICS FOR 74HC

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".
Transfer characteristics are given below.

Output capability: standard
I_{CC} category: MSI

TRANSFER CHARACTERISTICS FOR 74HC

Voltages are referred to GND (ground = 0 V)

SYMBOL	PARAMETER	T _{amb} (°C)								UNIT	TEST CONDITIONS	
		74HC									V _{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V _{T+}	positive-going threshold	0.70 1.75 2.30	1.13 2.37 3.11	1.50 3.15 4.20	0.70 1.75 2.30	1.50 3.15 4.20	0.70 1.75 2.30	1.50 3.15 4.20	V	2.0 4.5 6.0	Fig. 6	
V _{T−}	negative-going threshold	0.30 1.35 1.80	0.70 1.80 2.43	1.10 2.40 3.30	0.30 1.35 1.80	1.10 2.40 3.30	0.30 1.35 1.80	1.10 2.40 3.30	V	2.0 4.5 6.0	Fig. 6	
V _H	hysteresis (V _{T+} − V _{T−})	0.2 0.4 0.5	0.43 0.57 0.68	0.80 1.00 1.10	0.18 0.40 0.50	0.80 1.00 1.10	0.15 0.40 0.50	0.80 1.00 1.10	V	2.0 4.5 6.0	Fig. 6	

AC CHARACTERISTICS FOR 74HC

GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T _{amb} (°C)								UNIT	TEST CONDITIONS	
		74HC									V _{CC} V	WAVEFORMS
		+25			−40 to +85		−40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
t _{PHL} / t _{PLZ}	propagation delay A _n to Y _n		36 13 10	115 22 19		140 28 24		165 33 28	ns	2.0 4.5 6.0	Fig. 7	
t _{THL}	output transition time		19 7 6	75 15 13		95 19 16		110 22 19	ns	2.0 4.5 6.0	Fig. 7	

DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications". Transfer characteristics are given below.

Output capability: standard

I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
A _n	0.3

TRANSFER CHARACTERISTICS FOR 74HCT

Voltages are referred to GND (ground = 0 V)

SYMBOL	PARAMETER	T _{amb} (°C)								UNIT	TEST CONDITIONS	
		74HCT									V _{CC} V	WAVEFORMS
		+25			—40 to +85		—40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
V _{T+}	positive-going threshold	0.9 1.2	1.50 1.70	2.0 2.1	0.9 1.2	2.0 2.1	0.9 1.2	2.0 2.1	V	4.5 5.5	Fig. 6	
V _{T—}	negative-going threshold	0.7 0.8	1.06 1.27	1.4 1.7	0.7 0.8	1.4 1.7	0.7 0.8	1.4 2.7	V	4.5 5.5	Fig. 6	
V _H	hysteresis (V _{T+} — V _{T—})	0.2 0.2	0.44 0.44	0.8 0.8	0.2 0.2	0.8 0.8	0.2 0.2	0.8 0.8	V	4.5 5.5	Fig. 6	

AC CHARACTERISTICS FOR 74HCT

GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T _{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V _{CC} V	WAVEFORMS
		+25			—40 to +85		—40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t _{PHL} / t _{PLZ}	propagation delay A _n to Y _n		18	31		39		47	ns	4.5	Fig. 7
t _{THL}	output transition time		7	15		19		22	ns	4.5	Fig. 7

TRANSFER CHARACTERISTIC WAVEFORMS

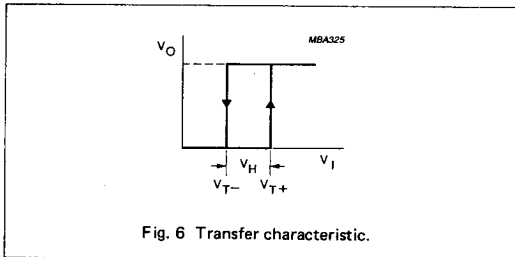


Fig. 6 Transfer characteristic.

AC WAVEFORMS

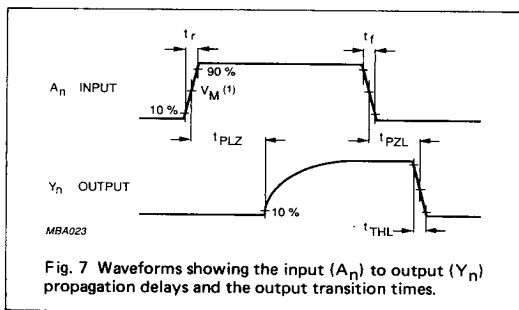


Fig. 7 Waveforms showing the input (A_n) to output (Y_n) propagation delays and the output transition times.

Note to AC waveforms

- (1) HC : $V_M = 50\%$; $V_I = \text{GND to } V_{CC}$.
HCT: $V_M = 1.3 \text{ V}$; $V_I = \text{GND to } 3 \text{ V}$.